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1/f Noise Sources in Dual-Gated Indium Arsenide Nanowire Transistors

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1/f Noise Sources in Dual-Gated Indium Arsenide Nanowire Transistors

Collin J. Delker, *Member, IEEE*, Seongmin Kim, Mattias Borg, Lars-Erik Wernersson, and David B. Janes, *Member, IEEE*

***Abstract*—1/f noise is studied in dual-gated InAs nanowire transistors consisting of an omega top gate with high-k atomic layer deposited dielectric and silicon dioxide to substrate back gate. Noise spectra at varying gate bias combinations are compared from devices with differing top-gate lengths to separate the noise contributions of the top-gated channel from the ungated access portion, including the metal–nanowire contacts. For a given device geometry, it is possible to bias the device into four different regimes where the resistance and the noise amplitude can each be independently dominated by either the channel or the access/contact regions. When the device is fully in the on state, the access/contact regions dominate both resistance and noise. When the device is operating near or below threshold, the channel dominates resistance and noise. For the lowest amount of overall 1/f noise, most of the nanowire should be covered by the top gate, minimizing the access region length.**

***Index Terms*—Indium Arsenide, low-frequency noise, nanowire FETs.**

I. Introduction

SEMICONDUCTOR nanowires show promise in future nanoelectronic applications such as high-speed electronics [1], chemical sensors [2], and transparent/flexible electronics [3]. However, one obstacle in realizing applications of nanowire devices has been the high levels of low-frequency noise, exacerbated in nanowires due to the high surface-to-volume ratio that increases the effects of surface defect interactions, particularly in III–V semiconductors such as indium arsenide (InAs) [4], [5]. The noise levels may be significant enough to mask the true electrical characteristics of nanowire devices such as 1-D transport. In nanowire devices, 1/f noise may arise from two sources: (1) carrier interaction with the nanowire–oxide interface through the channel; and (2) the current fluctuation through the source/drain contacts. Interface passivation would be expected to impact the former but not necessarily the latter.

Hooge's relationship

$$S_I = \frac{\alpha_H I^2}{f N_{\rm tot}} \tag{1}$$

has been often used to relate current noise spectral power density S_I to the current I, frequency f, and number of charge carriers $N_{\rm tot}$ in a device, where α_H is the Hooge parameter dependent on device materials and geometry [6]. This relationship assumes that charge carriers behave independently and that the current is uniform. It does not make any statements about the sources of noise in a device or if individual portions of a device (i.e., channel, contacts, and access regions) have unique influences over noise generation.

While Hooge's relationship (1) was originally empirical, physically based models have been developed. In MOSFETs, 1/f noise is attributed to tunneling of electrons into and out of traps in the surface oxide interface. Under this assumption, the Hooge parameter can be estimated based on the physical properties of the device, including dimensions, interface trap density, and a trap tunneling parameter [7]. This model has been also used to extract the trap density from noise measurements [8]. MOSFET models typically consider fluctuations in either carrier number or mobility within the channel but ignore contact contributions.

In other types of devices, contact effects also contribute to noise. It has been shown that 1/f noise in carbon nanotube transistors tends to stem from trapping and detrapping in the oxide layer or from excess noise in Schottky barrier metal–nanowire contacts [9]. Schottky barriers contribute 1/f noise through mobility and diffusivity fluctuations and current limiting in the metal–semiconductor barrier [10]. In [11], the influence of the gate on 1/f noise was studied in silicon nanowire transistors. Other studies have pointed to the contacts as being a possible contributor to noise in nanowire devices [12], and trapping and detrapping due to surface states and dangling bonds in the exposed wire can contribute to noise [13]–[15]. Hooge parameters as low as 4.2×10^{-3} have been demonstrated in vertical wrap-gate InAs nanowire transistors at room temperature [16] and as low as 5×10^{-4} in InAs nanowires at low temperatures [17]. However, few nanowire studies have quantitatively distinguished between the different noise sources. Understanding these noise contributions can provide a pathway toward improved device performance and also provide a means to differentiate channel effects from contact effects in overall device operation.

In this paper, we present an experimental study and associated models for InAs nanowire FETs with both back and top gates, with a variable fraction of the source–drain gap covered by the top gate. We observe various regimes where the noise and resistance are dominated either by the channel or by the access regions. It is also shown that the lowest noise levels can

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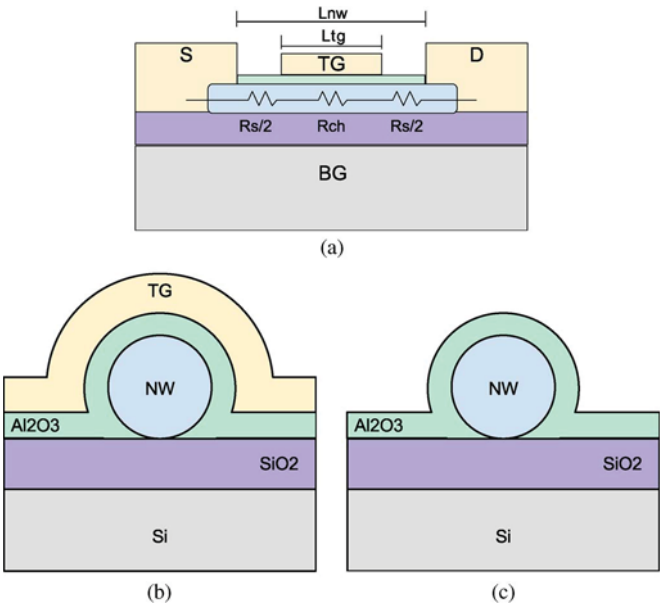

Fig. 1. Structure of dual-gate nanowire transistor. (a) Side view of the device from source to drain showing the resistance from the channel and from the access regions. (b) Cross section of the device in channel region covered by top gate. (c) Cross section of the device in access region with no top gate.

be achieved by covering the largest fraction of the nanowire between source and drain contacts with a top gate, minimizing the noise contribution from the access regions.

II. Fabrication and Device Structure

In order to study sources of noise contributions in InAs nanowire transistors, dual-gated nanowire transistors were fabricated. The devices consist of an omega-shaped top gate and a back gate, both controlling the same wire. InAs(111)B substrates were decorated with Au aerosol nanoparticles with a nominal diameter of 20 nm. These substrates were used to grow InAs nanowires in a metal–organic vapor-phase epitaxy reactor [18]. After an initial annealing step at 550 °C, the reactor temperature was ramped down to 450 °C after which trimethylindium (TMIn) and arsine (AsH_3) were introduced with molar fractions of 4.2×10^{-6} and 3.9×10^{-4}, respectively. The Au particles promote the growth of epitaxial nanowires in the (111)B direction, oriented vertically out from the substrate. The total growth time was 7.5 min after which the TMIn supply was terminated and the sample was cooled down under continued AsH_3 flow. The resulting nanowires are not intentionally doped and exhibit a uniform diameter without measurable tapering. The average length and diameter of the nanowires on the sample were measured to be 2.1 μm $(+/-0.14)$ and 26.5 nm $(+/-1)$, respectively.

The wires were then removed from the growth substrate by sonication in isopropanol. Three to four drops of nanowire solution were dispersed and allowed to dry on Si substrates with 20-nm thermal SiO_2, prepatterned with an array of alignment markers. The wires were optically imaged in relation to the alignment markers so that source and drain contacts could be aligned to individual wires and patterned by e-beam lithography, ensuring that each device contains a single nanowire. After a 5-s dip in buffered HF to remove any native oxide from the wires, nickel source and drain contacts were deposited by e-beam evaporation and liftoff. A 10-nm Al_2O_3 top-gate dielectric was deposited by atomic layer deposition using a Cambridge NanoTech F200 deposition system. Finally, a Ti/Au metal top gate was patterned and deposited within each source–drain gap. The device structure is shown in Fig. 1, including cross sections in the top-gated and access regions. The channel is defined as the portion of the nanowire covered by the top gate and has length $l_{\rm tg}$. The entire source–drain gap has a length of $l_{\rm nw}$, leaving access regions on either side of the channel. While the back gate modulates these access regions in addition to the channel, the top gate only modulates the channel. Several devices were fabricated with varying $l_{\rm tg}$ to $l_{\rm nw}$ ratios in order to study the influence of each gate on electrical and noise characteristics. Back-gate lengths $l_{\rm nw}$ ranged from 250 to 1000 nm, with top gates from 100 to 750 nm. The ratio of $l_{\rm tg}$ to $l_{\rm nw}$ varied from 0.1 to 0.75. The entire nanowire from source to drain, including the area not covered by the top gate, is passivated by the Al_2O_3 layer.

III. Modeling

The channel, controlled by the top gate, will have some resistance $R_{\rm ch}$. The remaining nanowire is controlled only by the back gate and will contribute additional resistance R_s so that the total resistance between the source and drain is

$$R_{\rm tot} = R_s + R_{\rm ch} \tag{2}$$

when biased in the linear region.

The number of free charge carriers in the nanowire is controlled by both top and back gates and can be calculated using gate capacitance values. The back gate has a cylinder-on-plate capacitance per unit length found from

$$C_{\rm bg} = \frac{2\pi\epsilon_o\epsilon_{\rm bg}}{\cosh^{-1}(1 + t_{\rm bg}/r_{\rm nw})} \tag{3}$$

where $t_{\rm bg}$ is the back-gate oxide thickness and $r_{\rm nw}$ is the nanowire radius. The top gate can be modeled using a partial coaxial capacitance value

$$C_{\rm tg} = \frac{0.6 \cdot 2\pi\epsilon_o\epsilon_{\rm tg}}{\ln\left((r_{\rm nw} + t_{\rm tg})/r_{\rm nw}\right)} \tag{4}$$

where the 0.6 factor accounts for the portion of the nanowire that is wrapped by the gate, and the top-gate oxide has thickness $t_{\rm tg}$. Assuming that the top and back gates have unique and independent threshold voltages, i.e., $V_{\rm TH_{top}}$ and $V_{\rm TH_{back}}$, respectively, the total number of carriers in the nanowire can be calculated using both gates

$$N_{\rm tot} = \frac{l_{\rm tg}C_{\rm tg}}{q}(V_{\rm tg} - V_{\rm TH_{top}}) + \frac{l_{\rm nw}C_{\rm bg}}{q}(V_{\rm bg} - V_{\rm TH_{back}}). \tag{5}$$

The number of carriers in the access regions can be found from

$$N_s = (l_{\rm nw} - l_{\rm tg})\frac{C_{\rm bg}}{q}(V_{\rm bg} - V_{\rm TH_{back}}) \tag{6}$$

and the channel has charge contributions from both gates such that

$$N_{\rm ch} = \frac{l_{\rm tg}}{q}\left[C_{\rm tg}(V_{\rm tg} - V_{\rm TH_{top}}) + C_{\rm bg}(V_{\rm bg} - V_{\rm TH_{back}})\right]. \tag{7}$$

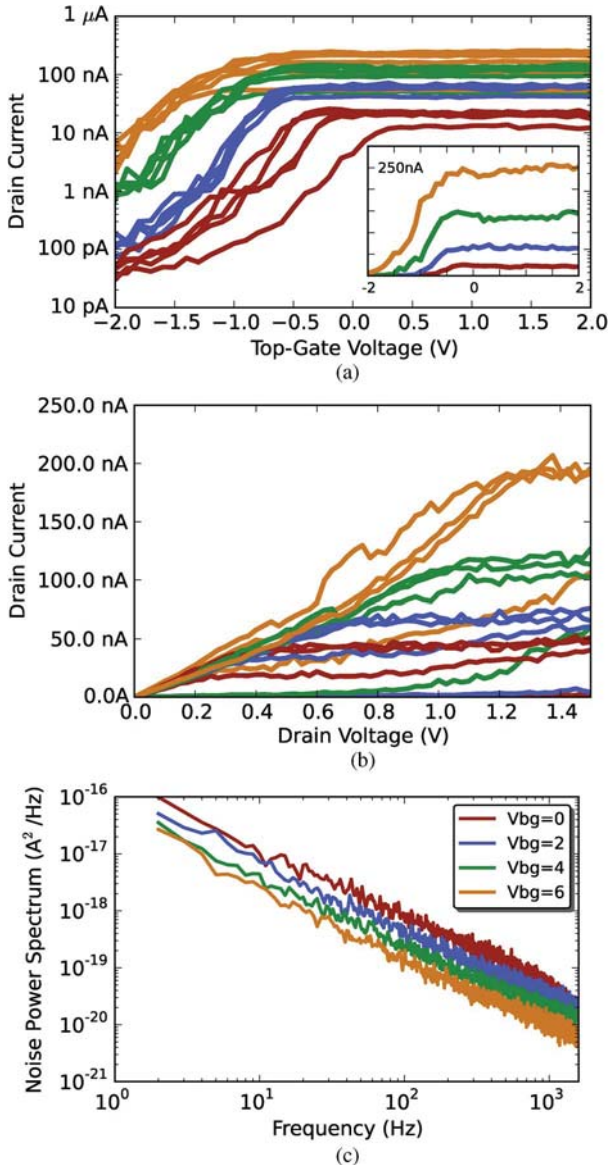

Fig. 2. Typical I–V characteristics for dual-gated device. (a) Transfer characteristics with drain voltages ranging from 0.2 to 1 V. (Inset) Same data at Vds $= 1$ only on a linear scale. (b) Output characteristics with top-gate voltages ranging from -2 to 2 V. (c) Measured 1/f noise spectrum for InAs device with varying back-gate voltages. Legend in (c) also applies to other figures.

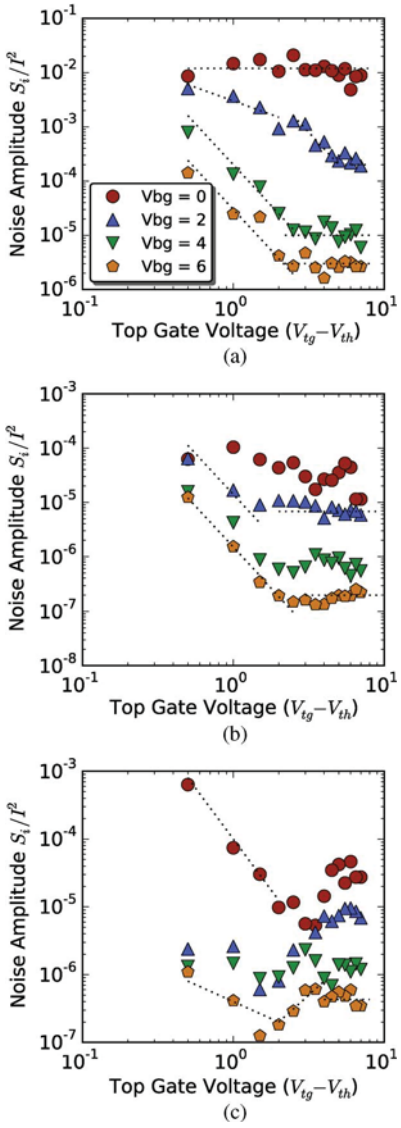

Fig. 3. Noise versus top-gate voltage for three devices with $l_{\rm tg}/l_{\rm nw}$ of (a) 0.1, (b) 0.5, and (c) 0.75. Dotted lines indicate reference slopes of 0 and -3, $+2$ and -1. Legend shown in (a) also applies to the other plots.

IV. Electrical Characterization

The current–voltage (I–V) characteristics of the devices were measured at room temperature using an Agilent 4516C semiconductor parameter analyzer. Typical I–V curves are shown in Fig. 2(a) and (b). The back gate turns on the contacts and access regions, enabling higher currents, whereas the top gate helps in fully shutting off the device. High noise levels are already apparent from the fluctuations in the I–V curves.

The 1/f noise in the devices was characterized at room temperature using an Agilent 35670A spectrum analyzer at varying top- and back-gate voltages both above and below threshold. Example noise spectra at various back-gate voltages are shown in Fig. 2(c). Drain bias was held constant in the linear region for all measurements so that channel resistance is not affected by saturation to ensure that (2) (5)–(7) apply. Noise levels tend to increase as the back gate is turned off, indicating a contact-dominated noise characteristic [19]. Several devices of varying gate length ratios were measured.

The noise amplitude at 100 Hz is normalized by the current squared, and the resulting S_I/I^2 is plotted against top-gate voltage, as shown in Fig. 3, for various $l_{\rm tg}/l_{\rm nw}$ ratios. The three devices featured in the figure have $l_{\rm tg}/l_{\rm nw}$ ratios of 0.1, 0.5, and 0.75, respectively, corresponding to $l_{\rm tg}$ and $l_{\rm nw}$ lengths of 100 nm/1000 nm, 250 nm/500 nm, and 750 nm/1000 nm, respectively. Several distinct regions emerge from these plots as indicated by the different slopes of each top-gate sweep on the log–log scale. At low top-gate voltages, the data show a negative slope, but as top-gate voltage increases, the slope levels out to zero.

These slopes are described in [20], which considered how noise in MODFETs with series access regions can exhibit various gate voltage dependency values, i.e., $S_I/I^2 \propto V_{\rm tg}^m$ with $m = -1$, -3, 0, or $+2$, depending on whether the channel

TABLE I
PROPORTIONALITY CONSTANT m OF NOISE-TO-GATE VOLTAGE

m	$R_s > R_{ch}$	$R_{ch} > R_s$
$S_{Rch} > S_{Rs}$	-3	-1
$S_{Rs} > S_{Rch}$	0	+2

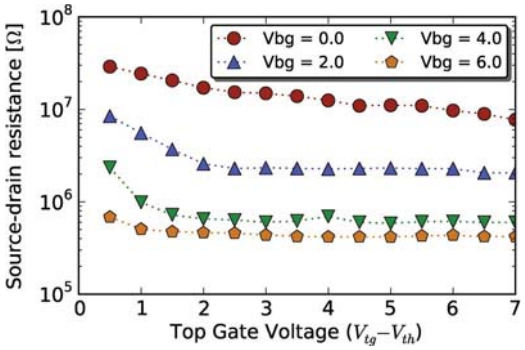

Fig. 4. Resistance versus top-gate voltage at different back-gate voltages.

or access regions are dominating the resistance and noise, as shown in Table I. When the access regions and contacts dominate both noise and resistance, $m = 0$, but when the channel dominates both noise and resistance, $m = -1$. In our measurements, all four possibilities can be seen among the nanowire devices tested in their different operating regimes.

A similar model can be applied to our nanowire devices to separate the noise contributions from the channel and access regions, but the effects of the back gate also need to be considered. From the measured I–V data, total source–drain resistance $R_{\rm tot}$ is found at each bias point, as shown in Fig. 4. Each gate serves to lower the total resistance between the source and drain. An access region resistance R_s is found for each back-gate voltage by extrapolating a plot of $R_{\rm tot}$ versus $1/V_{\rm tg}$ to the point where $1/V_{\rm tg} \to 0$. The channel resistance $R_{\rm ch}$ at each given bias point is then determined from (2).

After the resistance associated with each bias point is calculated, the Hooge parameter within each regime can be found. By examining the noise amplitudes in the channel- or access-dominated regions, separate Hooge parameters can be extracted for the access region α_s and for the channel $\alpha_{\rm ch}$. Taking noise to be a fluctuation in resistance S_R, then in general, $S_R/R^2 = S_I/I^2 = \alpha/fN$. Assuming two independent 1/f noise contributions, the total noise can be written as [21]

$$S_{R_{\rm tot}} = S_{R_{\rm ch}} + S_{R_s} \tag{8}$$

where the noise from the channel region is

$$S_{R_{\rm ch}} = \frac{\alpha_{\rm ch} R_{\rm ch}^2}{f N_{\rm ch}} \tag{9}$$

and the noise from the access region is

$$S_{R_s} = \frac{\alpha_s R_s^2}{f N_s}. \tag{10}$$

To extract the Hooge parameters for each nanowire region, the dominant regimes in Table I are used. When biased in the $m = -1$ regime, the channel is dominating both noise and resistance; hence, the measured $S_I/I^2 \simeq S_{R_{\rm ch}}/R_{\rm ch}^2$. Using this data point, the channel Hooge parameter can be calculated from

$$\alpha_{\rm ch} = \frac{S_I}{I^2} f N_{\rm ch} \tag{11}$$

with $N_{\rm ch}$ calculated from (7).

When biased in the $m = 0$ regime, the access regions dominate both noise and resistance; hence, $S_I/I^2 \simeq S_{R_s}/R_s^2$. Using this data point, the access region Hooge parameter can be extracted using

$$\alpha_s = \frac{S_I}{I^2} f N_s \tag{12}$$

with N_s calculated from (6).

Since the data follow a Hooge relationship within each regime, Hooge parameters that are independent of gate voltage are obtained as long as the device remains in the same dominant regime. The extracted Hooge parameter components for several devices of varying top-gate lengths are shown in Fig. 5(a). The

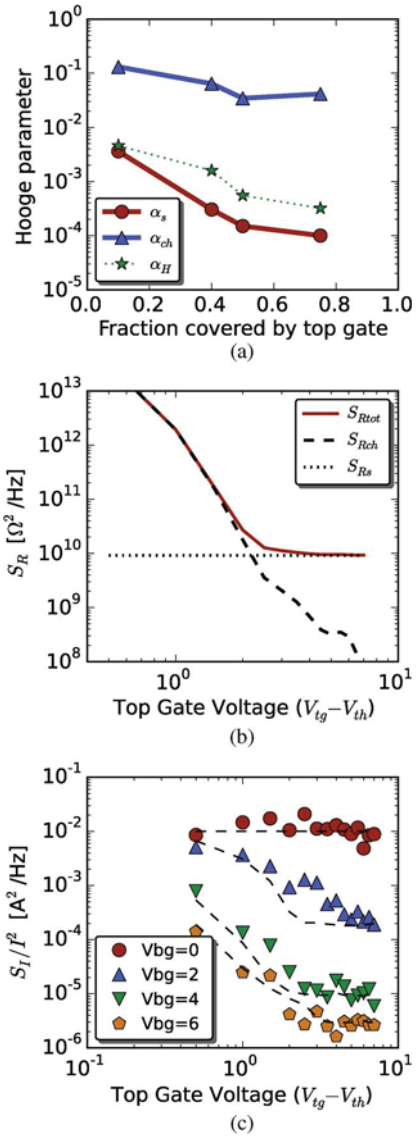

Fig. 5. (a) Hooge parameter components extracted from noise spectra of devices of different channel lengths. (b) Noise contribution from the contacts and access regions for the 10% top-gated device at Vbg = 6 V. (c) Measured noise amplitude with dashed lines showing model considering sum of channel and access region noise contributions at same bias points.

channel Hooge parameter is higher than the access Hooge parameter for all devices tested. Although the Hooge parameter for the channel is higher, the actual noise amplitude still depends on bias of both gates, and under certain operating regimes, channel noise may be smaller than access region noise, as discussed later. If a single Hooge parameter is computed using the traditional method of lumping together the effects of the channel and access regions using (1), the dotted line in Fig. 5(a) is obtained, showing α_H values near 10^{-3}. It is clear that the lowest α_H in this type of device can be obtained by covering the entire nanowire with the top gate, thereby minimizing the access region noise contribution.

With the Hooge parameters determined, the noise contributions from each region can be calculated at various bias points from (9) and (10). The two noise components are shown in Fig. 5(b) as a function of top-gate voltage for the 10% top-gated device with the back gate turned on to 6 V. Because the access regions are independent of top-gate voltage, access region noise S_{R_s} is constant for the fixed back-gate bias. However, channel noise $S_{R_{\rm ch}}$ is controlled by the top gate. A clear transition is seen between access region-dominated behavior at higher top-gate bias and channel-dominated behavior at lower top-gate bias. When the sum of the two calculated noise components is normalized by resistance and plotted with the original measured data [see Fig. 5(c)], the total extracted noise follows the trends observed in the measured data. The calculations were done at other back-gate voltages, as also shown in Fig. 5(c), illustrating that this model also captures the back-gate dependence of noise with higher back-gate voltages exhibiting less noise amplitude.

To illustrate the effect of access region noise behavior and channel noise behavior, the ratio of channel noise to access region noise $S_{R_{\rm ch}}/S_{R_s}$ is plotted against the channel-to-access resistance ratio $R_{\rm ch}/R_s$ from each of the measured data points, as shown in Fig. 6. Each quadrant represents the dominance of either channel or access region and corresponds to one of the previously mentioned m values. These plots show strong correlation between the slopes of the noise plots in Fig. 3, with lower top-gate voltages appearing further to the right in the $m = -1$ and $m = -3$ quadrants, where higher top-gate voltages appear in the $m = 0$ quadrant.

When comparing the devices with differing top-gate lengths, the $S_{R_{\rm ch}}/S_{R_s}$ ratio decreases, and the $R_{\rm ch}/R_s$ ratio increases when a higher percentage of the channel is covered by the gate. This can be seen in the Fig. 6 plots as the lines shifting down and to the right as the top-gate length increases. This behavior is consistent with the model because in the channel region, resistance is directly proportional to and noise is inversely proportional to $l_{\rm tg}$, but in the access regions, resistance is directly proportional to and noise is inversely proportional to $(l_{\rm nw} - l_{\rm tg})$.

In the longest top-gate device, there are signs of entering the $m = +2$ region, which is an indication of very noisy contacts/access regions sometimes seen in contact-dominated devices. In this device, under certain bias regimes, the channel is long enough to contribute significant resistance, yet the noise from the contacts is much higher due to the small number of carriers available in the contact area. Further work should be done to improve the interface between metal and nanowire.

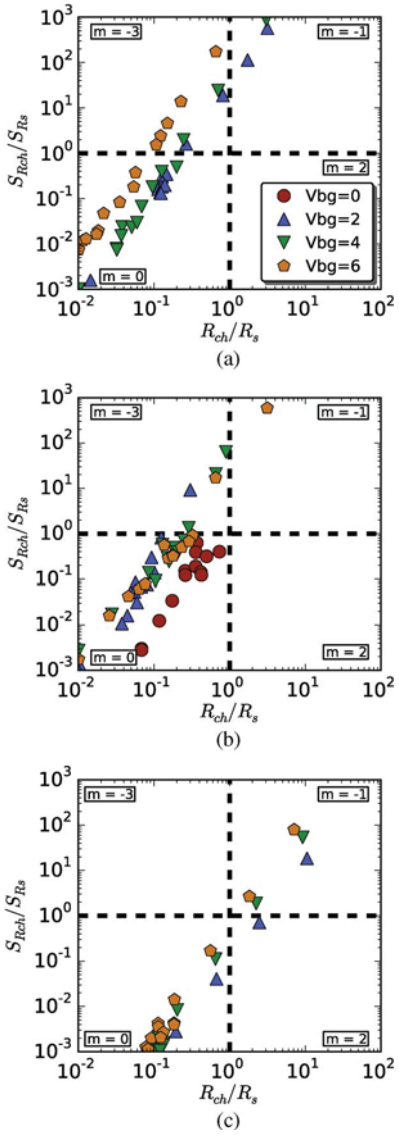

Fig. 6. $S_{R_{\rm ch}}/S_{R_s}$ plotted against $R_{\rm ch}/R_s$ for the same devices in Fig. 3 with $l_{\rm tg}/l_{\rm nw}$ of (a) 0.1; (b) 0.5; and (c) 0.75. Legend shown in (a) also applies to the other plots.

V. Discussion

The model described above accounts for a top gate and a back gate that control the resistance of the channel and access regions. It does not explicitly include effects of the metal–semiconductor contacts, which may add to the resistance and noise. Because the back gate forms its channel near the bottom of the nanowire and the metal contact interface with the top of the wire, there will be some resistance between the contact and the back-gate channel, which remains nearly independent of back-gate voltage, particularly for higher gate bias. However, in all but the highest top- and back-gate biases, this additional contact resistance will be minimal compared with the channel and access resistances. The contact contribution is also minimized in devices with long access regions. This allows fair comparison of devices by the $l_{\rm tg}/l_{\rm nw}$ ratio instead of requiring absolute lengths. When extracting Hooge parameters from measured noise levels, it was ensured from the corresponding I–V curves [see Fig. 2(a) for example] that the device was operating under bias conditions where contact resistance is not a limiting factor.

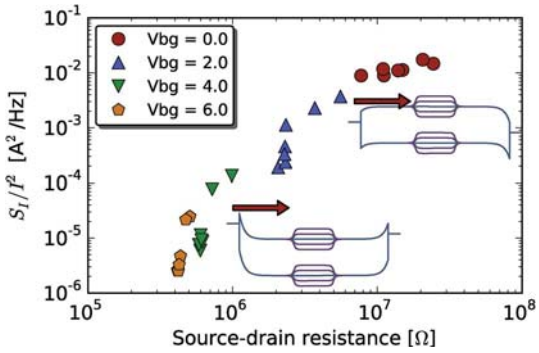

Fig. 7. Normalized noise amplitude versus source-to-drain resistance at same bias points. Inset band diagrams show effect of top gate with back gate above and below threshold.

Evidence of contact resistance can be seen from the output characteristics in Fig. 2(b). If the contact resistance were minimal, turning on the back gate would decrease the resistance in both access regions and channel, whereas the top gate would only decrease the resistance of the channel. However, at low drain and high top- and back-gate voltages, the back gate does not appear to drastically reduce the resistance (by increasing the slope in the linear region of the output characteristics); therefore, the resistance in this regime is not determined by the portions of the nanowire modulated by the back gate but by the metal–nanowire contacts.

Further insight into the contact/access resistance operation of these devices can be gained by plotting the noise amplitude (normalized by current squared) versus source–drain resistance at different gate bias combinations, as shown in Fig. 7, and considering the respective band diagrams. When the back gate is well above threshold (low resistance), the top gate modulates the noise levels but has little effect on resistance because the current is determined by thermionic emission from the contacts into the channel, as illustrated by the lower inset band diagram. When the back gate is near or below threshold (high resistance), the top gate can modulate the resistance but has less effect on noise, as illustrated by the upper inset band diagram. Applying higher back-gate voltages will decrease noise levels by lowering the contact resistance and increasing charge carriers in the access regions. This is also apparent from the top-gate transfer characteristics on a linear scale, as shown in the inset in Fig. 2(a). As the top gate turns on, the current starts to increase, but after a certain point, it flattens out due to the contacts and access regions. The flat portion of the transfer characteristics corresponds to the $m = 0$ regions of the noise data where the access regions dominate resistance. As the top gate decreases enough to begin to shut off the current, the $m = -3$ region is entered and eventually becomes low enough to enter the $m = -1$ region where the channel dominates resistance.

The physically-based noise model, which assumes that noise is generated by electron trapping in the oxide interface, predicts that the Hooge parameter should remain constant with channel length. However, if an overall Hooge parameter is naively extracted without considering the separate effects of the contacts and access regions, strong length dependence is seen [see α_H in Fig. 5(a)] due to contacts and access regions being neglected in the calculation. When the access regions and channel are separated, the channel noise component correctly shows a length-independent Hooge parameter $\alpha_{\rm ch}$. The access region noise, however, still exhibits a downward trend in Hooge parameter α_s as the length of the channel increases. This trend can be explained by considering both the ungated nanowire region and the metal–nanowire contact. Although α_s is assumed to be only from the access regions, the metal contact will add some noise due to barrier fluctuations that were not included in the calculations. In devices with large access regions (small fraction covered by the top gate), the large number of carriers available will lead to a low access region noise, which allows the contact noise to become significant. For fixed contact noise, the relative contribution to α_s will be largest for shortest $l_{\rm tg}$ values (longest access regions). Overestimation is mostly apparent in the $l_{\rm tg}/l_{\rm nw} = 0.1$ device, but the increase in α_s with decreasing $l_{\rm tg}/l_{\rm nw}$ ratio indicates some contact contribution even for other contact lengths. Quantitatively accounting for this extra contact noise is left for future work.

To apply this noise model to a device with metal–semiconductor contacts, it should be ensured that fringing fields from the top gate do not modulate the contacts. The characteristic band-bending length of the contacts is [22]

$$\lambda = \sqrt{\frac{\epsilon_{\rm nw}}{\epsilon_{\rm ox}} d_{\rm nw} d_{\rm ox}} \tag{13}$$

where $d_{\rm nw}$ and $d_{\rm ox}$ are diameters of nanowire and oxide, respectively, and $\epsilon_{\rm nw}$ and $\epsilon_{\rm ox}$ are the relative dielectric constants. For these devices, λ is 48 nm. In all the devices tested, the spacing between contact and top gate is at least 125 nm; hence, the top gate will not affect the contacts.

In this model, the number of charge carriers was calculated assuming a constant gate capacitance value. The experimental devices, however, are approaching small diameters where the quantum capacitance of the nanowire can become small and therefore significant [23]. However, because these devices are not fully quantum-capacitance limited, ignoring the effects of quantum capacitance in this analysis does not qualitatively change the results and only overestimates the channel charge by about 30% (or less, depending on bias point).

VI. Conclusion

In summary, 1/f noise in top-gated nanowire devices comes from two sources, i.e., the top-gated channel region and the back-gated access regions/metal contacts. In this paper, a basic model for noise amplitude and resistance of the two regions has been developed based on calculations of carrier numbers, Hooge parameters, and resistances extracted from experimental data. This model was used to analyze the relative contributions of the two regions at various bias points and the overall noise/resistance properties as a function of top-gate length and bias point. For a given device geometry, it is possible to bias the device into four different regimes where the resistance and the noise amplitude can each be independently dominated by either the channel or the access/contact regions. Signatures of the four possible regimes were observed in various devices, and transition points between regimes were observed to shift as the channel length was changed.

When the device is operating far above threshold, the channel has low resistance and low noise contribution; thus, the contacts dominate the observable noise. When the device is operating near or below threshold, the channel has high resistance and it dominates the noise. For the lowest amount of noise, most of the nanowire should be covered by the top gate, minimizing the access region length. Passivation and surface treatments may reduce the noise levels by removing interface traps but should be focused on the metal–nanowire contact and the ungated region to reduce noise in the on state of the device. Reducing the series resistance of the ungated region through selective doping or other methods is key to optimizing the noise in nanowire devices.

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