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Student Paper

Study of Ultra-scaled SiGe/Si Core/Shell Nanowire FETs for CMOS Applications

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Introduction: SiGe/Si core/shell nanowire (NW) devices are promising candidates for the future generation MOSFETs providing better channel control and hole mobility [1-4]. These core-shell devices can be exploited both as p- and n-type devices [3]. The Si shell improves the semiconductor-oxide interface and enhances the device performances [1, 3]. The Germanium condensation technique [4] is able to provide high Ge content (>50%) channel with Si as capping layer. In this work we investigate the viability of using these core/shell NWFETs for CMOS application.

Approach: We have developed an atomistic Tight-Binding[5] based Virtual Crystal Approximation (VCA) model for the electronic structure calculation of SiGe alloys[6], which is coupled to a 2D FEM Poisson solver for charge-potential self-consistency[7]. Transfer characteristics are obtained using a ballistic top-of-the-barrier model [8]. Different gate configurations (double, tri, all around) can be considered in the model.

Device details: We investigate circular gate all around (GAA), <100> oriented channel, NWFETs with constant semiconductor diameter (W) of 9nm. The NW body is made of a SiGe core, with 90, 70 and 50% Ge concentration, wrapped in a Si capping layer (Fig. 1a). The core diameter (CD) varies from 0, 3, 4, 6 ,8, to 9nm. Both SiO_2 ($\varepsilon_r = 3.9$) and high-K ($\varepsilon_r = 20$; like ZrO_2, HfO_2) gate dielectrics are used in p- and n-type MOSFETs, with doped source/drain and undoped channel.

Results and Discussion: The I_{ON}, C_{gON} and gate delay (τ) are chosen as metrics for the performance comparison of n/p FETs [9]. These metrics are obtained at V_{DD} =0.55V and I_{OFF}=1e-9Amp. A small C_{gON} (desired) represents a fast switching device. A high Ge% (~90%) and a thin core (~25% of W) reduce C_{gON} ~3 times as compared to a pure Si pFET (Fig.2a). C_{gON} is insensitive to the variation in Ge% and core thickness in nFETs (Fig.2b).

With increasing Ge% and increasing CD, I_{ON} improvement is very small(~1.05X) in pFETs (Fig.3a). A small benefit can be attributed to the buried channel in pFETs (hole cloud is inside the core as seen in Fig. 5), leading furthermore to a poor gate control. nFETs show an improvement of ~1.1X for CD:W ~ 1:2 (Fig.3b) since the inversion charge is pushed towards the surface (Fig.6). This improvement increases with the Ge% since the energy barrier height (ΔEc) between the core and the shell increases, thereby pushing the inversion charge to the high mobility Si shell (Fig.6).

Gate delay ($\tau = C_{gON}V_{DD}/I_{ON}$) is determined by the interplay of C_{gON} and I_{ON}. In pFETs, the minimum τ is obtained for the devices with CD/W ~50% (Fig.4a). A maximum improvement of ~1.32X is obtained for 90% Ge core since it has the maximum I_{ON} and minimum C_{gON}. For nFETs, an improvement of ~1.1X is observed for 90% Ge core with a shell width close to the core width (CD ~70%).Thus, the SiGe/Si core/shell structure speeds up both pFETs and nFETs compared to their pure Si counterparts.

Optimization of pFETs: From Fig.4 it is clear that pFETs are ~3 times slower as compared to nFETs. pFETs can be improved if the gate control on the channel is improved[4]. This can be achieved in two ways, (a) the reduction of the Si shell thickness and (b) the use of a high-K gate dielectric material for better electrostatic control. We have performed Ids-Vgs simulation for all Ge % channels with no Si cap and 1.5 nm HfO_2 dielectric (ε_{ox} ~20). The I_{ON} improves as much as ~2.5X times bringing the pFETs performances close to nFETs (Fig.7). However, this increases the fabrication complexity and need for better NW/oxide interface quality (Table I)[4].

Conclusions and Outlook: We have investigated SiGe/Si core/shell NWFET for CMOS technology. A high Ge% and a thick Si cap improve nFETs. However, pFETs along with a high Ge% require a thin Si shell and a high-K gate dielectric to make them comparable to nFETs for high performance logic applications. Alloy and interface scattering has been neglected in this study. This can reduce the channel current. However, we expect the trends to remain the same since they are dominated by bandstructure effects in ultra-scaled devices. All these points have been summarized in Table I.

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TABLE 1. Performance, Structure and Optimization comparison of SiGe/Si Core/Shell n/p NWFETs.

Device Type →	**pFET**	**nFET**
C_{gON} reduction	Higher Ge, thinner core	Insensitive to Ge% & core width
I_{ON} improvement	Higher Ge, thicker core	Higher Ge, core/shell width ~1:1
Gate delay	~1.3X faster compared to Si	~1.1X faster compared to Si
Channel type/ Gate control	Buried/Bad gate control	Surface / Good gate control
Process Complexity	More steps, high-K integration [4]	Fits into standard CMOS [4]
Optimization	High-K gate dielectric, thin shell	Shell/Core width ~ 1:1

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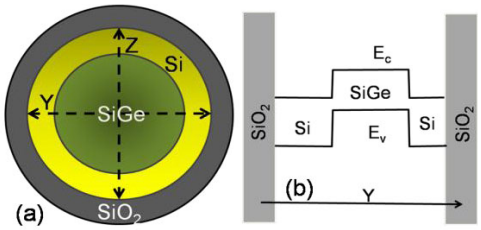

Fig.1. (a) Schematic of a circular GAA SiGe/Si core/shell NWFET. (b) Band-edge diagram showing Ec and Ev in the device in the plane of the FET channel.

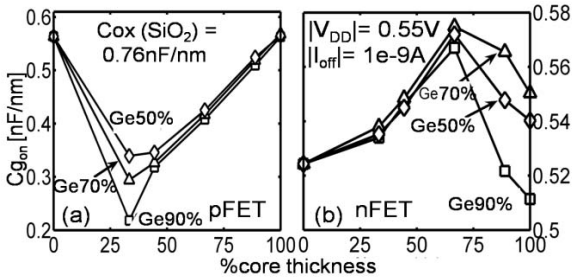

Fig. 2. On state gate capacitance (Cg_{ON}) for **(a)** pFETs and **(b)** nFETs at V_{DD} = 0.5V.

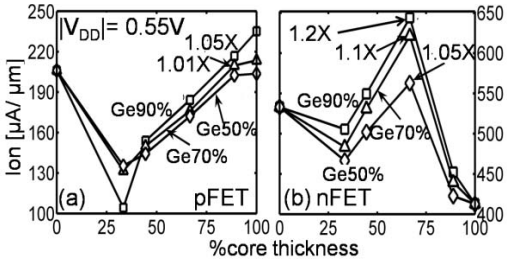

Fig.3. Ion for **(a)** pFET and **(b)** nFET at VDD = 0.55V (normalized to perimeter). Ion increase is monotonic for pFETs. nFETs show highest I_{ON} at 75% core thickness.

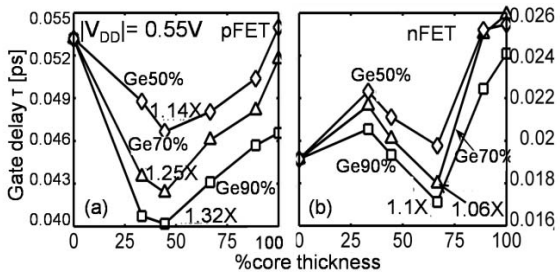

Fig.4. Gate delay(τ) for **(a)** pFET and **(b)** nFET. SiGe core improves pFETs more (~1.3X) compared to nFETs (~1.1X) over conventional SiNW p/nFETs respectively.

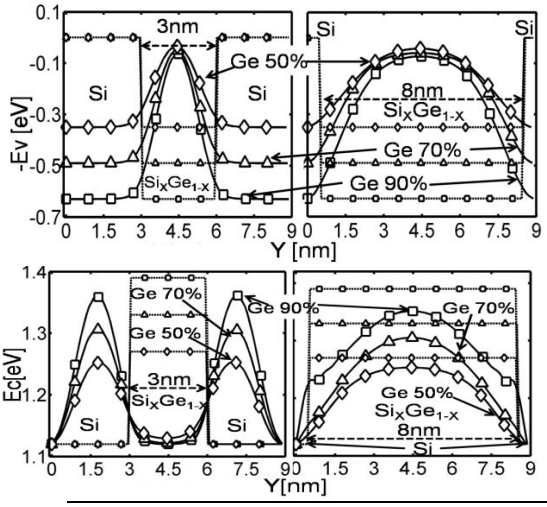

Fig.5. Hole cloud under inversion for 3nm and 8nm core for 3 different Ge%. Larger core (thinner shell) brings charge closer to the wire surface thereby improving the pFET.

Fig.6. Electron cloud under inversion for 3nm and 8nm core for 3 different Ge% core. Smaller core pushes the charge closer to wire surface resulting in better nFET performance.

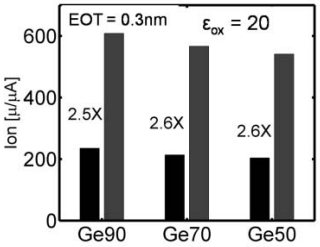

Fig. 7 pFET improvement (core/shell = 9nm/0nm, tox=1.5nm) using a high-K (HfO) gate dielectric. A 2.5X improvement in Ion is obtained for all Ge%. Thinner EOT brings the charge closer to gate resulting in better transistor action and making I_{ON} comparable to nFETs.