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Silicon Nanowire Tunneling Field-Effect Transistor Arrays: Improving Subthreshold Performance Using Excimer Laser Annealing

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Silicon Nanowire Tunneling Field-Effect Transistor Arrays: Improving Subthreshold Performance Using Excimer Laser Annealing

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***Abstract*—We have experimentally established that the inverse subthreshold slope S of a Si nanowire tunneling field-effect transistor (NW-TFET) array can be within 9% of the theoretical limit when the doping profile along the channel is properly engineered. In particular, we have demonstrated that combining excimer laser annealing with a low-temperature rapid thermal anneal results in an abrupt doping profile at the source/channel interface as evidenced by the electrical characteristics. Gate-controlled tunneling has been confirmed by evaluating S as a function of temperature. The good agreement between our experimental data and simulation allows performance predictions for more aggressively scaled TFETs. We find that Si NW-TFETs can be indeed expected to deliver S-values below 60 mV/dec for optimized device structures.**

***Index Terms*—Excimer laser annealing (ELA), nanowire tunneling field-effect transistor (NW-TFET), steep-slope transistors, ultrathin-body silicon-on-insulator (SOI).**

I. Introduction

SINCE the first experimental demonstration of sub-60 mV/dec operation [1], tunneling field-effect transistors (TFETs) have been extensively studied on a variety of material systems to address the demand for low-power device operation not achievable with conventional metal–oxide–semiconductor field-effect transistors (MOSFETs) [2]–[6]. For this purpose, detailed studies have been dedicated to the importance of using a 1-D geometry, such as a nanotube and nanowire (NW), to access the so-called quantum capacitance limit (QCL) [7]–[9], wherein proper drain voltage dependence is ensured in the device's ON-state [10]—a feat that is not easily achievable in 2- and 3-D systems. Despite this fact, a relatively small number of studies exist on Si NW TFETs (NW-TFETs) at present [11]–[14]. Those that do typically employ vapor–liquid–solid (VLS) grown NWs that use Au catalyst materials not compatible with current manufacturing processes and have the added challenge of NW placement [11]–[13]. Ideally, Si NW-TFET arrays would be created in a top–down approach to combine the inherent scaling advantages of NWs and their capability to operate in the QCL with a complementary metal–oxide–semiconductor (CMOS) compatible process flow.

The only critical component missing then is the ability to maintain the abruptness of the doping profile at the source/channel interface for these NW-TFET arrays. A major problem that the semiconductor industry at large is facing today is precisely this issue of maintaining the abruptness of channel doping profiles in MOSFETs as dimension scale [15]. Traditional rapid thermal anneal (RTA) processing used to activate implanted dopants can lead to unacceptable diffusion in ultrathin body semiconductors, which is a problem that is exacerbated in a NW geometry [16]. To overcome this limitation, researchers have explored alternate doping techniques and diffusionless activation processes such as plasma doping (PLAD) and excimer laser annealing (ELA), respectively [17], [18]. Whereas abrupt source/drain doping profiles are important for conventional MOSFETs, they are *crucial* in achieving optimized band-to-band tunneling (BTBT) devices such as TFETs, whose ON-state currents $I_{\rm ON}$ and inverse subthreshold slopes are ultrasensitive to the abruptness of this junction. To our knowledge, the use of ELA for enhanced BTBT devices has not been explored yet.

Herein, we present the first systematic study on top–down Si NW-TFET arrays comparing RTA, ELA, and low-temperature RTA (LT-RTA) activation and recrystallization processes to realize significantly improved BTBT behavior as measured by $I_{\rm ON}$ and $S_{\rm avg}$, which is the average extracted inverse subthreshold slope over three orders of magnitude change in drain current I_D. Simulations using the Wenzel–Kramer–Brillouin (WKB) approximation are used to compare the results with ideally expected $S_{\rm avg}$-values, showing good agreement with the ELA + LT-RTA process and allowing the prediction of performance for aggressively scaled TFETs.

II. Experiment

NW-TFET arrays consisting of 400 NWs in parallel were fabricated on silicon-on-insulator (SOI) substrates

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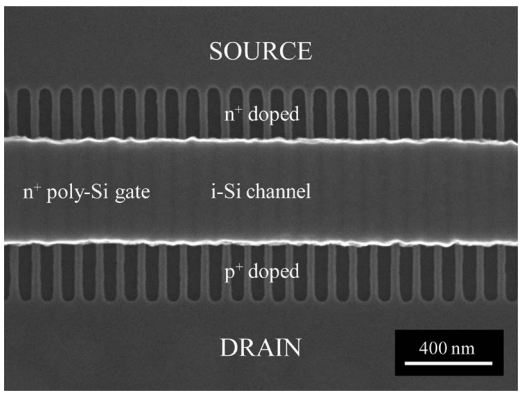

Fig. 1. Scanning electron microscope image of a NW-TFET array with a nominal wire pitch of 100 nm and wire width of ∼20 nm. An intrinsic Si channel region is preserved under the 500-nm-wide poly-Si gate and n^+- and p^+-regions were formed through ion implantation and RTA, ELA, and LT-RTA activation processes.

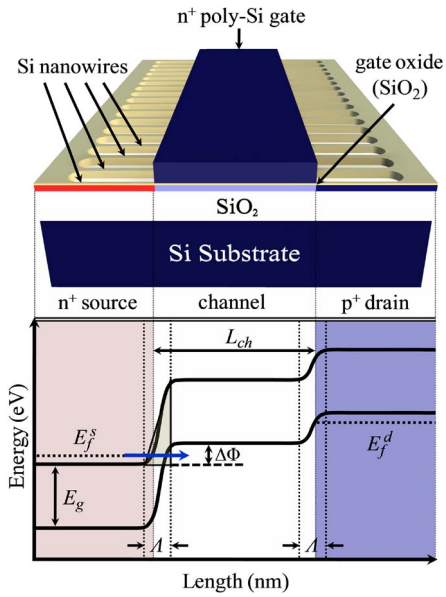

Fig. 2. Schematic representation of (top) the fabricated Si NW-TFET arrays with a cross-sectional slice of one of the NWs, showing the n^+ source, i-Si channel, and p^+ drain segments. (Bottom) The band diagram projection illustrates the hole current flow responsible for the p-branch tunneling characteristics when the valance band in the channel is above the conduction band edge in the source.

with a Si body thickness of 20 nm and a 100-nm-thick buried oxide (BOX) layer. Wire arrays were defined using electron-beam lithography to achieve a nominal pitch and wire width of 100 and 20 nm, respectively (see Fig. 1). Dry oxidation was used to form a gate oxide thickness of ∼6 nm, as confirmed by cross-sectional transmission electron microscope imaging (not shown). The n^+ poly-Si gated channel region was patterned to occupy 500 nm of the 1 μm total wire length, leaving ∼250 nm for the n^+-source and p^+-drain extension regions. The source and drain regions were implanted at energies of 5 (As) and 1.5 keV (B) with a 0° implant angle and dose of 1×10^{15} cm^{-2}. The implant energies were carefully chosen with simulation to ensure the presence of a sufficient seed crystal at the bottom of the NWs. A detailed description of the NW-TFET array fabrication process used in this paper was recently reported by Sandow *et al.* [14].

To evaluate the impact of different activation processes on TFET performance, three techniques were investigated: RTA, ELA, and ELA + LT-RTA. For RTA, a standard spike anneal at 1000 °C was used to activate the dopants and repair the damage induced by implantation. The ramp-up rate for the RTA process was 100 °C/s, and the ramp-down rate was 80 °C/s. Submelt ELA processing was performed using a KrF excimer laser ($\lambda_{\text{ex}} = 248$ nm) with a top-flat beam profile of 7×7 mm^2. The pulse duration and number of pulses was held constant at 28 ns and 100, respectively. The energy fluence was tuned in the range of 45–75 mJ/cm^2 to optimize tunneling performance. The best results were obtained at 60 mJ/cm^2; therefore, we restrict our discussion in this paper to this energy fluence. It is important to note that using an energy fluence level corresponding to the *submelt process regime* is the key to maintaining the abruptness of the as-implanted profile. Previous studies that focus on the application of ELA to NWs grown via the VLS method reported that Si NW melting occurred in the range of 60–70 mJ/cm^2 in the form of beaded periodic chains of nanoparticles due to morphological instabilities [19]. Similar melting effects were not observed in our NW arrays formed on SOI at these energy levels, possibly due to the absence of Au and other morphological defects found in grown NWs that lower the melting threshold. Finally, this ELA process was combined with a 5-min 650 °C LT-RTA treatment to further improve doping abruptness at the tunnel junction. The temperature was chosen in an attempt to reduce the depth of the amorphized region and enhance the crystalline quality while minimizing both diffusion into the unimplanted Si regions (i.e., in-diffusion) and dopant deactivation [20], [21].

Electrical characterization of the TFET arrays was carried out by negatively biasing the p^+-drain with respect to the n^+-source to permit the staircase p-i-n structure depicted in Fig. 2. In this arrangement at a sufficiently high negative gate voltage V_{gs}, the valence band in the channel is lifted above the conduction band in the source, and interband tunneling occurs at the source/channel junction, giving rise to p-type transistor behavior.

III. Results and Discussion

A. Components of TFET Operation

To gain a qualitative understanding of the impact of the various geometry and material-related parameters on tunneling performance, we invoke the Landauer expression for a 1-D ballistic device, given by [22]

$$I_D = 2 \cdot \frac{q}{h} \int_0^{\Phi_f^0} dE \cdot T(E) \left(f_s(E) - f_d(E) \right). \qquad (1)$$

To achieve reasonably high I_{ON} currents, $T(E)$ *should then be as close to unity as possible*. For TFETs, the transmission can be estimated using the WKB approximation for a triangular

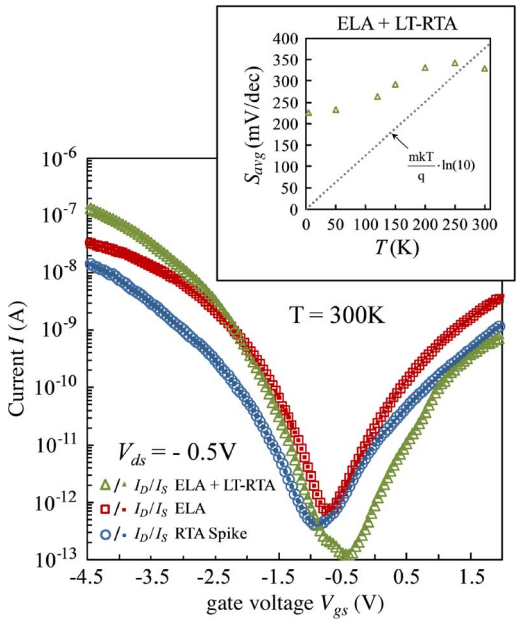

Fig. 3. Transfer characteristics showing tunneling currents in the p- and n-branches for three annealing conditions: (circles) 1000 °C RTA spike anneal, (squares) ELA at an energy fluence of 60 mJ/cm^2, and (triangles) ELA at the same conditions followed by a 650 °C LT-RTA step for 5 min. Overlapping I_D and I_S currents indicate the absence of gate leakage. (*Inset*) Extracted $S_{\rm avg}$ vs. T values over 3 orders magnitude change in I_D, which demonstrate $<$ factor of 2 variation from 4 to 300 K and much larger $S_{\rm avg}$ values than for the kT/q behavior (dotted line) expected for thermal emission at lower temperatures.

barrier, as shown in Fig. 2 band diagram, and is expressed as [23]

$$T_{\rm WKB} \approx \exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3q\hbar(\Delta\Phi + E_g)}\right). \quad (2)$$

Here, q, $\hbar$, E_g, and m^* represent the charge of an electron, the reduced Planck's constant, the band gap of the material, and the transverse effective mass, respectively. The energy window $\Delta\Phi$ is the difference between the surface potential in the channel and the conduction band edge in the source, as depicted in Fig. 2, and is directly related to V_{gs}. Furthermore, $\Delta\Phi$ is the only operation-dependent parameter in (2). Since the remaining parameters are material dependent or physical constants, the screening length Λ or the region over which the potential varies spatially, offers the only option in which $T_{\rm WKB}$ can be modified for a given material choice. A decrease in Λ leads to a larger tunneling probability, which in turn results in an effectively reduced $S_{\rm avg}$-value. It is this link between $S_{\rm avg}$ and Λ that will be explored in greater detail in this paper.

B. Role of Doping Abruptness in TFETS

Given that maintaining a minimum Λ is crucial for optimized tunneling in a particular material, a closer look at the factors that contribute to this parameter is instructive. Ideally, Λ has two major components, namely, the screening length that arises from the depletion of the doped source region at the source/channel interface $\lambda_{\rm dop}$ and screening from the intrinsic channel region $\lambda_{\rm ch}$, which results from the selection of device dimensions and geometry. More specifically, Λ is *ideally* defined with the following analytic expression:

$$\Lambda = \lambda_{\rm dop} + \lambda_{\rm ch} = \sqrt{\frac{\varepsilon_o\varepsilon_{\rm body}\cdot kT}{q^2N_D}} + \sqrt{\frac{\varepsilon_{\rm body}}{\varepsilon_{\rm ox}}\cdot\frac{d_{\rm body}^2}{8}\cdot\ln\left(1+\frac{2d_{\rm ox}}{d_{\rm body}}\right)}, \quad (3)$$

for a coaxial gate geometry, where ε_0, $\varepsilon_{\rm body}$, $\varepsilon_{\rm ox}$, $d_{\rm body}$, $d_{\rm ox}$, N_D, k, and T represent the permittivity of free space, relative permittivity of the semiconductor and oxide, body thickness, oxide thickness, doping concentration in the source, Boltzmann's constant, and operating temperature, respectively. To avoid degradation of $S_{\rm avg}$, the Fermi level in the source should be kept between 50–100 meV above the conduction band [24], corresponding to a doping level in Si of $N_D \approx 8\times10^{19} - 2\times10^{20}$ cm^{-3}. Thus, at room temperature, $\lambda_{\rm dop} \approx 0.5$ nm and $\lambda_{\rm dop} \ll \lambda_{\rm ch}$ even for aggressively scaled devices.

Simply using (3) then gives the impression that the only components necessary for achieving a minimum Λ are aggressive scaling and high-κ dielectrics. Although these are indeed necessary ingredients, these modifications alone *do not* necessarily sufficiently minimize Λ. The primary reason for this is that (3) assumes an infinitely abrupt doping profile at the source/channel interface. In reality, even an as-implanted doping profile for a given implant energy produces a finite "smearing" of the lateral dopant profile into the channel region, or $\Delta\lambda_{\rm dop}$, that inhibits the grip of the channel potential over this region, effectively increasing the tunneling distance. Simulations have shown that even in planar structures, the steepness of the lateral doping profile falls off at ~3 nm/dec for As and ~5 nm/dec for B when a standard RTA 1000 °C spike anneal is used for activation [25]. Given that there is ~10-dec difference in doping at the source/channel junction for an ideal Si TFET, the degradation of Λ and, ultimately, $S_{\rm avg}$ may be significant if junction abruptness cannot be reasonably maintained. For this reason, alternative activation processes are explored in this paper to improve junction steepness and, consequently, $S_{\rm avg}$.

C. Characterization of Disparately Activated NW-TFETS

The transfer characteristics for the RTA spike, ELA, and ELA + LT-RTA-annealed NW-TFETs are displayed in Fig. 3 at $V_{ds} = -0.5$ V. We briefly note that all of the devices were tested in the range of $V_{ds} = -0.05$ to -3 V and displayed the same general trends between different activation conditions over this entire voltage range. Furthermore, noting that the purpose of a steep-slope device is to allow the transition between the ON- and OFF-states to occur over a smaller gate voltage window and that $I_{\rm ON}$ for an optimized device is defined at $V_{gs} = V_{ds} =$ supply voltage V_{dd} [26], the choice of $|V_{ds}| = 0.5$ V was made to achieve the best possible device performance at a V_{ds} value actually suitable for low-power applications. I_D and I_S are both included in Fig. 3 to indicate the absence of any appreciable gate leakage, which is a necessary component to ensure that the extracted subthreshold slope is, in fact, accurately represented and not artificially low as a result of I_D leaking from the channel to the gate in the OFF-state. This is particularly

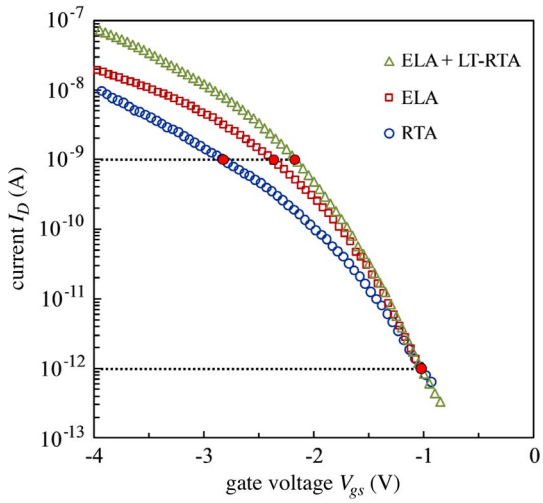

Fig. 4. Transfer characteristics shifted in V_{gs} to align the p-branches of RTA, ELA, and ELA + LT-RTA annealed NW-TFET devices at $I_{\mathrm{OFF}} = 10^{-12}$ A. (Dotted lines and large dots) The extraction points for S_{avg} over three orders magnitude change in I_D.

important deep into the OFF-state where gate leakage can be significant and where local subthreshold slopes are often reported. Whereas a threshold voltage V_{th} shift occurs between the devices that use different means of activation, device-to-device variation of V_{th} for a given activation technique was found to be negligible.

Tunneling occurs in both the p- and n-branches; however, we restrict our analysis to the p-branch since, in principle, higher activation and steeper doping profiles are possible with As, compared with B doping. The inset in Fig. 3 shows the observed S_{avg} vs. temperature T over 3 orders of magnitude change in I_D for the ELA + LT-RTA device. Always the same trend was observed—a relatively temperature independent S_{avg} from 4–50 K and 150–300 K with some temperature dependence showing up in the range of 50–150 K. A number of factors can potentially contribute to this temperature-dependent range, even in a tunneling device, such as freeze out of trap-assisted tunneling centers or quenching of phonons required for tunneling through the indirect Si band gap [27], [28]. Clearly, however, the S_{avg} variation is far below the predicted value for thermal emission over a gate-controlled barrier that tends toward zero, as indicated by the dotted line. In our experiment, S_{avg} only changes by a factor of 1.45 to 1.65, regardless of the number of decades change in I_D considered, over the entire temperature range from 4 to 300 K.

The key performance-related features to note are I_{ON} and S_{avg}, where we define I_{ON} at 1 V above threshold and S_{avg} over 3 orders of magnitude change in I_D from 10^{-12} to 10^{-9} A to provide a reasonable $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio for digital applications. To more clearly illustrate the comparison of S_{avg} for the different activation processes, the p-branch current in Fig. 3 is re-plotted in Fig. 4, with the characteristics shifted in V_{gs} to align at $I_{\mathrm{OFF}} = 10^{-12}$ A. I_{ON} and S_{avg} both demonstrate a clear and significant trend of improvement, depending on the activation process used. Here, ELA + LT-RTA shows the greatest enhancement followed by ELA and, finally, the RTA spike anneal. The extracted values are summarized in Table I.

TABLE I
COMPARISON OF THE NW-TFET DEVICE PERFORMANCE

Process	S_{avg} (mV/dec)[a]	V_{th} (V)	I_{ON} (nA)[b]
RTA	601	-3.5	15.2
ELA	452	-2.9	21.5
ELA + LT-RTA	382	-3.0	77.0

[a] S_{avg} values are extracted over three orders of magnitude current from $I_{OFF} = 10^{-12}$ A to $I_D = 10^{-9}$ A. [b] $I_{ON} = I_D$ at $|V_{gs} - V_{th}| = 1$V

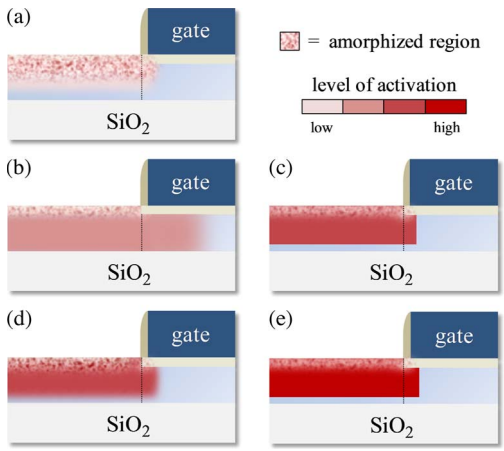

Fig. 5. Cross-sectional schematics depicting the expected relative levels of activation and dopant profile smearing at the source/channel junction under the gate for the activation conditions described in this paper, including: (a) as-implanted; (b) 1000 °C spike RTA; (c) 650 °C SPER only; (d) ELA only; and (e) ELA + 650 °C LT-RTA.

D. Performance Dependence on the Activation Process

To gain a better understanding of the trends for the extracted figures of merit, namely I_{ON} and S_{avg}, a qualitative description of the expected doping behavior, in terms of activation and junction steepness, during the various processes is necessary. Typically, the degree of activation and cross-sectional area of current flow are considered as key ingredients for achieving high I_{ON} values in conventional MOSFETs. This logic alone, however, is not sufficient to explain the current in tunneling devices since a 1000 °C RTA spike anneal should, in principle, favorably compare in terms of I_{ON} from this perspective. By contrast, TFETs are electrically very sensitive to Λ, as evidenced by the results presented in Fig. 4 and discussed in Sections III-A–C; therefore, over and above the level of activation and cross-sectional area of current flow, *lateral doping abruptness at the source/channel junction is paramount in tunneling devices*. Ultimately, it is the competition and interplay between these physical manifestations that results in the observed characteristics.

Fig. 5 provides a simplified picture of the expected activation levels and doping steepness for the different processes. Certain features have been exaggerated for clarity in the foregoing arguments. The as-implanted profile shown in Fig. 5(a) is expected to exhibit a large degree of amorphized Si with a very

low level of activation [20]. The existence of a seed crystal at the bottom of the NW is crucial in avoiding higher defect densities that arise from complete amorphization [29]. Fig. 5(b) depicts the situation for the RTA spike anneal, where significant diffusion toward the unimplanted Si regions at the bottom of the NW and laterally into the channel region is expected [30]. This has the effect of increasing the cross-sectional area of current flow through the NW while achieving reasonably high levels of activation *but* at the expense of a significant "smearing" of the dopant profile at the source/channel interface, which effectively increases Λ by reducing the abruptness of the transition between the source and the gated channel region, as discussed in Section III-B. By contrast, it is known that a single 650 °C solid-phase epitaxial regrowth (SPER) anneal, which is akin to the LT-RTA process, results only in dopant diffusion toward the implanted surface [20]. During this process, a fraction of the As dopants are "snow ploughed" toward the Si/gate SiO_2 interface, while many of the As dopants at the same time relocate onto Si lattice sites within the implanted region and become electrically active during the recrystallization process. Importantly, this diffusion of dopants toward the Si/gate SiO_2 interface and negligible in-diffusion act to sharpen the borders of the doping profile *beyond* the as-implanted profile, as pictured in Fig. 5(c), creating a box-like dopant profile at the border of the implanted/unimplanted region. This process then effectively minimizes Λ, enhancing the probability of tunneling transmission at the source/channel interface. Additionally, SPER is a nonequilibrium process that has demonstrated the ability to overcome the solid-solubility limit imposed on the conventional RTA process [31]. Activation using submelt ELA is also capable of achieving activation levels in excess of the solid-solubility limit and doping profiles with only subtle variations in steepness from the as-implanted profile, as displayed in Fig. 5(d) [18]. At first, this process alone may appear to provide an adequate option; however, similar to the SPER case, this nonequilibrium method leads to a metastable state where deactivation can occur with subsequent thermal treatments between 500 °C–800 °C common in CMOS processing [32], [33]. Furthermore, laser activation treatments, such ELA, are known to suffer from poorer local atomic order [30]. This combined with the smaller activated cross section can potentially lead to a relatively large series resistance in a NW geometry, which may be responsible for the comparatively pronounced saturation of I_D deeper into the ON-state of the ELA only device.

By combining ELA *and* LT-RTA [see Fig. 5(e)], an optimal balance between lateral profile steepness, activation, and cross-sectional current flow may be realized, promoting optimized tunneling through the source/channel barrier. Several detailed studies have been dedicated to the benefits of using laser annealing (LA) in conjunction with RTA processing, compared with an RTA spike anneal or LA alone [21], [30], [34]. Submelt ELA promotes high activation with minimal diffusion. In this way, many As dopants are already active on substitutional sites prior to LT-RTA. The subsequent LT-RTA treatment, which clearly improves $I_{\rm ON}$ and $S_{\rm avg}$ in the TFET arrays, may enhance tunneling through a number of mechanisms, including a sharpened dopant profile, improved crystallinity, minimization of the depth of the amorphous region, and/or higher activation. Further investigation is needed to quantify and isolate the effects of each of these potential contributing factors. In any case, the selection of 650 °C for LT-RTA should provide access to the "sweet spot" where deactivation is minimized and in-diffusion is negligible [20], [21]. The outcome is a highly activated source doping with a sharp source/channel junction, as electrically verified by the results presented in Fig. 4 and Table I. Further optimization of the LT-RTA process may be possible by using smaller time durations, although there is still some debate as to whether deactivation occurs during recrystallization of the amorphous layer or in succession to this process for SPER [35], [36]. In the present case, where ELA has already recrystallized much of the NW, even smaller times than are typically used in SPER processing may be sufficient. Regardless, if the LT-RTA time duration can be properly tuned, further optimization of TFET performance is possible.

IV. Simulation and Scaling

The evolution in device performance for the activation techniques presented herein demonstrates an unambiguous trend of improvement in moving from the standard RTA process to a combination of ELA and LT-RTA; however, this raises the broader question of whether this process enhancement is sufficient enough to ultimately achieve a sub-60 mV/dec $S_{\rm avg}$ with aggressive scaling.

In order to answer this question, a model that adequately captures the key contributing factors to device operation over a wide range of $d_{\rm body}$ and $d_{\rm ox}$ is essential. To accomplish this task, we employ a more encompassing version of the Landauer formalism presented in (1), wherein, for a given channel potential Φ_f^0, the number of contributing modes $M(E)$, is analytically determined by considering the mode spacing that arises due to size quantization in the NW, rather than simply assuming a single mode, as in (1). In this way, the appropriate number of modes is assigned for a given NW diameter at a given value of Φ_f^0. In addition to size quantization effects, our model also considers the influence of V_{gs} on Φ_f^0 to capture the transition from the classical limit into the QCL. In a well-behaved fully depleted device, the total gate capacitance C_g is given by $C_g = C_{\rm ox}C_q/(C_{\rm ox}+C_q)$, where C_q is the quantum capacitance or change in channel charge with changing surface potential [9]. The relationship between V_{gs} and Φ_f^0 is given by

$$\delta\Phi_f^0 = \frac{C_{\rm ox}}{C_{\rm ox}+C_q}\cdot q\delta V_{gs}. \tag{4}$$

In 1-D systems, the QCL can be reached, where $C_q < C_{\rm ox}$, and the gate capacitance is dominated by C_q. Consequently, $\delta\Phi_f^0/q\delta V_{gs}$ approaches unity even in the devices ON-state. In our model, the actual band movement is accounted for by determining C_q for each V_{gs} using the expression

$$C_q = q^2\frac{\delta}{\delta\Phi_f^0}\int_0^\infty D(E)\cdot T_{\rm WKB}(E) \times(f_S(E,T)+f_d(E-qV_{ds},T)dE. \tag{5}$$

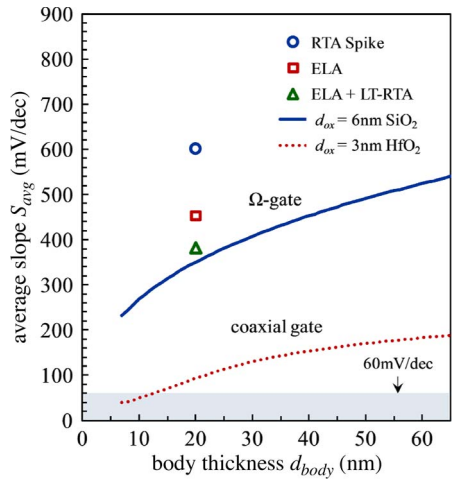

Fig. 6. Simulation curves, showing how $S_{\rm avg}$ over 3 orders magnitude change in I_D scales with $d_{\rm body}$, are plotted together with experimentally extracted values of $S_{\rm avg}$ for RTA, ELA, and ELA + LT-RTA. Aggressively scaled NW-TFETs with $d_{\rm ox} = 3$ nm (HfO_2) show the potential for sub-60 mV/dec operation for $d_{\rm body} < 13$ nm.

Importantly, the transmission probability that appears in (5) involves BTBT. This is in contrast to the conventional MOSFET case where transmission is only a function of scattering. The result is that the QCL can be more easily accessed in a device that employs tunneling since the smaller tunneling probability lowers C_q, compared with $C_{\rm ox}$ for a given set of $d_{\rm ox}$ and $d_{\rm body}$. Using (2) and (3), we calculated C_q given by (5) followed by the modified Landauer expression in an iterative fashion to generate I_D–V_{gs} curves. Since the gating arrangement of the top–down TFETs is more accurately described by an Ω-gate structure rather than a fully coaxial gate geometry, λ_{ch} in (3) was adjusted by a factor of $\sqrt{4/3}$ to account for the fact that only 75% of the channel circumference is covered by the gate. Using this approach, $S_{\rm avg}$ was determined by averaging the slope of these curves over 3-dec change in I_D from 10^{-12} to 10^{-9} A to match the experimental data for comparison.

The results are represented by the solid line in Fig. 6. At $d_{\rm body} = 20$ nm, the simulated curve has a value of 350 mV/dec, compared with 382 mV/dec for the dual process ELA + LT-RTA device, a ∼9% deviation in contrast to the ∼72% variation for the RTA spike annealed sample. By adding $\Delta\lambda_{\rm dop}$ to (3), the effective physical smearing of the dopant profile at the source/channel interface was estimated for each of the activation processes by adjusting $\Delta\lambda_{\rm dop}$ until a match was obtained between the simulated and experimentally extracted $S_{\rm avg}$ values shown in Table I. The outcome was $\Delta\lambda_{\rm dop-RTA} \approx 9.2$ nm $> \Delta\lambda_{\rm dop-ELA} \approx 3.7$nm $> \Delta\lambda_{\rm dop-ELA+LT-RTA} \approx 1.1$ nm. These values assume that the degradation of the subthreshold slopes is primarily due to the dopant profile smearing problem. In reality, a number of other factors can potentially contribute to the deviation in $S_{\rm avg}$ as well, including interface trap and parasitic fringe capacitance contributions. Given that similarly fabricated NW MOSFETs demonstrated an $S \sim 64$ mV/dec (close to the thermal limit), we rule out any significant capacitance contributions and attribute the majority of the departure of $S_{\rm avg}$ from the ideal expected values to dopant smearing due to the activation and implant processes. One fortunate outcome is that, contrary to most scaling processes, *the smearing of the source/channel doping profile will improve as NW dimensions scale*, and smaller implant energies are required, resulting in a tighter lateral distribution that yields a smaller Λ. In other words, $S_{\rm avg}$ is expected to get closer to the ideal theoretical limit as the NW diameter scales.

Based on the fact that the choice of $d_{\rm body}$ and $d_{\rm ox}$ used in this paper are not sufficient to reach the sub-60 mV/dec range, further scaling measures are obviously required. It was found that a combination of aggressively scaled high-k dielectrics and small NW diameters are required to access sub-60 mV/dec inverse subthreshold slopes (see dotted curve in Fig. 6). To simulate this curve, the following assumptions were made: 1) 3-dec change in I_D with $I_{\rm OFF}$ adjusted from 10^{-12} to 3.3×10^{-13} A (reliable data is available for the ELA + LT-RTA device at this current level, as shown in Figs. 3 and 4); 2) a gate-all-around (GAA) geometry; and 3) a 3-nm-thick HfO_2 gate dielectric with a conservatively estimated dielectric constant of ∼15. This curve was only extended to 7 nm to reflect the fact that below this diameter, E_g increases in a $1/d_{\rm body}$ fashion due to quantization effects [37]. Here, *a projection of* $S_{\rm avg} \approx 39$ mV/dec *is possible* at $d_{\rm body} = 7$ nm, a substantial improvement over the thermal limit, with sub-60 mV/dec operation possible for $d_{\rm body} < 13$ nm. This result is encouraging in the sense that the feasibility of creating such Si NW arrays has already been experimentally demonstrated [38] and suggests in combination with our findings a route toward Si-based steep-slope devices.

V. Conclusion

$S_{\rm avg}$ has been experimentally extracted from top–down NW-TFET arrays that were fabricated employing processing methods that are compatible with state-of-the-art CMOS techniques. By using ELA in conjunction with an LT-RTA activation process to preserve doping abruptness at the source/channel tunneling interface, a significant improvement in $S_{\rm avg}$ and $I_{\rm ON}$ were achieved. $S_{\rm avg}$ for ELA + LT-RTA was shown to be within ∼9% of the theoretical limit for a perfectly abrupt doping profile. Furthermore, our simulations have shown that future work using this activation process in conjunction with NW-TFETs that have a smaller diameter, GAA architecture, and HfO_2 gate dielectric will enable the realization of sub-60 mV/dec operation on a Si platform.

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