2-26-2010

Sub-threshold study of undoped trigate nFinFET

G C. Tettamanzi
Delft Univ Technol

G P. Lansbergen
Delft Univ Technol

A Paul
Purdue University - Main Campus

Sunhee Lee
Purdue University - Main Campus, sunnyleekr@purdue.edu

P A. Deosarran
Delft Univ Technol

See next page for additional authors

Authors

G C. Tettamanzi, G P. Lansbergen, A Paul, Sunhee Lee, P A. Deosarran, N Collaert, Gerhard Klimeck, S Biesemans, and S Rogge

Sub-threshold study of undoped trigate nFinFET

G.C. Tettamanzi [a,*], G.P. Lansbergen [a], A. Paul [b], S. Lee [b], P.A. Deosarran [a], N. Collaert [c], G. Klimeck [b], S. Biesemans [c], S. Rogge [a]

[a] Kavli Institute of Nanoscience, Delft University of Technology, Lorentzweg 1, 2628 CJ Delft, The Netherlands
[b] Network for Computational Nanotechnology, Purdue University, West Lafayette, Indiana 47907, USA
[c] InterUniversity Microelectronics Center (IMEC), Kapeldreef 75, 3001 Leuven, Belgium

ARTICLE INFO

ABSTRACT

Modern MOSFET devices with *undoped* channel have a non-trivial current distribution, which is gate voltage dependent. In our work we have studied the sub-threshold behavior of *undoped* triple gate MOSFETs (FinFETs) using a thermionic transport model. We have analyzed the conductance data of such devices, and from this, we have been able to determine the evolution of both the active cross-section area of the channel and the barrier height as a function of the gate voltage. The result of our experiments shows good agreement with tight binding simulations and with analytical results. This confirms the validity of the use of our thermionic approach to study transport in sub-micrometer size FinFET devices and not only in micrometer size samples specially made for characterizations.

© 2009 Elsevier B.V. All rights reserved.

1. Introduction

The continuous request of miniaturization in modern MOSFETs needs to be followed by constant effort towards the understanding of the mechanisms of transport in such devices. In *undoped* triple gate MOSFETs (FinFETs), a novel geometry that has been introduced to overcome short channel effects (SCE's) [1], the details of transport have been studied so far only using computational [2–6] or theoretical [7] tools. There is therefore a great need of the implementation of innovative experimental techniques that could allow a better understanding of transport in these devices. Our work in the field has been driven by this necessity and in this paper we describe what is, to the best of our knowledge, the first ever developed experimental technique that can be used to map the location of area of transport in sub-micrometer size FinFETs.

2. Experimental

Our FinFET devices consist of a nanowire channel connected to large contacts (source and drain) etched in a 65 nm Si intrinsic film with a wrap-around metallic gate on covering three faces of the channel [1,8]. Conductance versus temperature data for undoped FinFETs of channel length, $L = 40$ nm, and channel height, $H = 65$ nm, but different channel width, W, from 25 nm to 125 nm have been taken [8]. Richardson fits ($ln(G/T)$ versus $1000/T$ at fixed gate voltage, V_g), obtained from the rearrangement of the conductance versus V_g data taken at different temperatures have been analyzed using a thermionic fitting procedure [9].

This fitting procedure is implemented using the model of the thermionic emission through a barrier [9]:

$$G = SA^*T \frac{e}{k_B} \exp\left(-\frac{E_b}{k_B T}\right) \qquad (1)$$

where S is the portion of the physical cross-section that participates to transport, E_b is the source (drain)–channel barrier height, and $A^* = 2.1 \times 120 \text{ A cm}^{-2}\text{K}^{-2}$ is the effective Richardson constant for Si [5,9]. By mean of this fitting procedure, E_b versus V_g and S versus V_g curves have been then determined and studied as our final goal has been to gain information about the extend and the location of transport in our devices. In our investigations we could exclude tunneling [10], due to its different temperatures dependence.
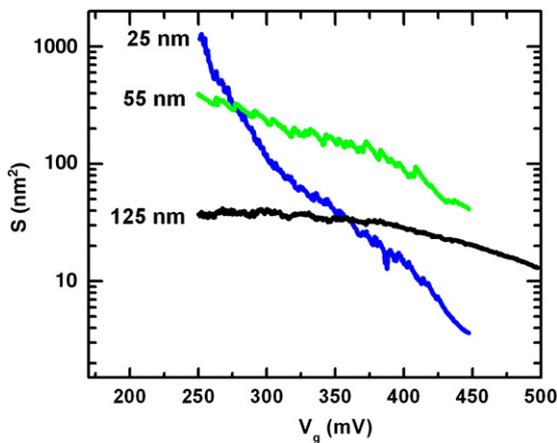
3. Results

By analyzing the data of our devices, we have been able to determine the evolution of both the barrier height, E_b, and the active cross-section area of the channel, S, as a function of V_g (see Figs. 1 and 2). The active cross-section area is an important parameter as it provides a direct indication on the portion of the physical cross-section that carries the bulk of the current. In Fig. 1, we readily observe a decrease of E_b for increasing V_g for all devices. Another visible trend is reflected in the data of Table 1, where the coupling factors $\alpha_1 = \frac{\partial E_b}{\partial V_g}$, that is obtained from our thermionic fits of Fig. 1 and give an indication of the coupling between the gate and the whole channel, shows a decrease for increasing width. Alternatively, the coupling factors α_2, obtained from Coulomb blockade measurements (as in Fig. 3) do not show the same decrease. This because the Coulomb blockade transport that we observe originates from interface
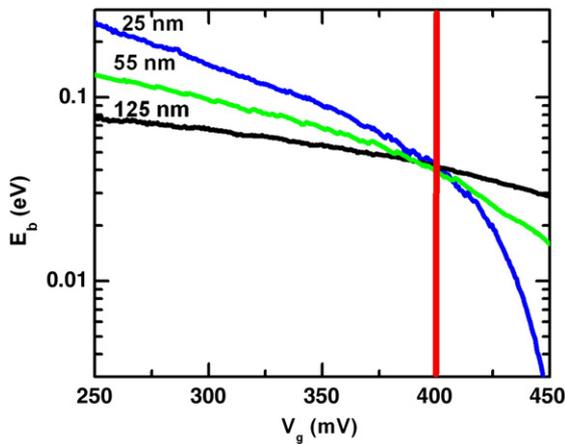
Fig. 1. Barrier height versus gate voltage data of having the same channel height and length, 65 nm and 40 nm respectively, but different values for the channel width, W; 25 nm (blue line), 55 nm (green line) and 125 nm (black line). The red line indicates the position of the common crossover. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)


Fig. 2. Active cross-section area versus gate voltage for the same three different devices of Fig. 1. Results here presented are replicated for different devices having the same channel dimensions but not shown for clarity.

states, and therefore from the region of the channel that is always strongly coupled to the gate, in contrary to the center of the channel that is affected by SCEs and influences negatively the behavior of α_1 when the width is increased. More importantly, we find a common crossing point between different E_b–V_g traces corresponding to different device widths, as it is shown in Fig. 1. This crossing point is located at $V_g = 0.4$ V, as indicted by the red line in Fig. 1, and corresponds to the expected work function difference between the metallic gate and the Si channel [3]. We associate this result to a correct choice of the thermionic model used to analyze our data, e.g.: this proves that in our devices and in the region of interest for us, transport arise in a thermionic fashion through a barrier that is artificially engineered by mean of mismatch between the work function of the metallic gate and the electron affinity of the Si channel and this is independent from the width of the devices.

Table 1
Summary of the characteristics of the gate channel capacitive coupling of devices reported in this study obtained from the results of the fit of Fig. 1 and from Coulomb blockade measurements at 1.6 K.

Width (nm)	25	55	125
α_1	1	0.7	0.14
α_2	0.7	0.8	0.8
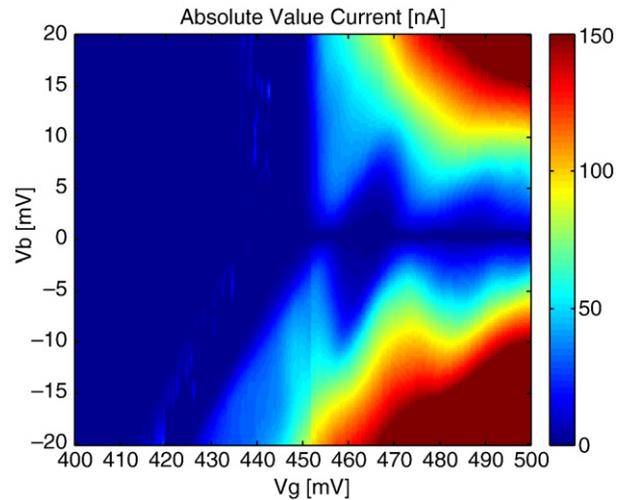
Fig. 3. Stability conductance data obtained for a 25 nm width device at 1.6 K. The observed Coulomb blockade diamonds are probably attributable to confined-trapped states in the interface Si channel-metallic gate [9]. Similar measurements are obtained for all devices independently from the width of the channel.

From another side, and this is particularly evident for the device with the smallest width, $W = 25$ nm, as it is shown in the blue line of Fig. 2, from the data of S we see that at $V_g = 0$ we measure an active cross-sectional area comparable to the physical cross-section of the channel, but this area decreases dramatically with increasing V_g. In order to benchmark our experimental method, we have used state-of-the-art-simulations, done under an atomistic 10 band sp3d5s* tight binding (TB) model, to perform electronic structure calculation (coupled self-consistently with a 2D Poisson solver [11]) and we obtained terminal characteristics using a ballistic top of the barrier model [12]. The results of such simulations done for a device having very similar characteristics of our ($W = 25$ nm and $H = 65$ nm) show a behavior similar to the one observed in our experiments. In fact, we use these simulations to calculate the potential distribution in the cross-section of the channel below the gate (Fig. 4). The potential distribution gives a direct indication of the portion of the transverse cross-section that is
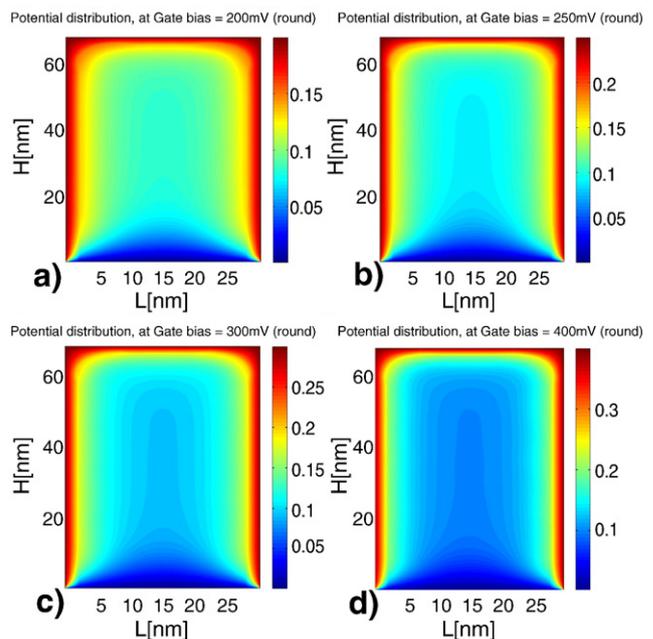
Fig. 4. Results obtained from our tight binding (TB) model with spin orbit coupling for the charge distribution under the gate. Results are obtained for a device of $W = 25$ nm and $H = 65$ nm, and for V_g of a) 200 mV b) 250 mV c) 300 mV and d) 400 mV respectively.

electrically active, as only the portions of the channel for which the potential distribution is very close to the value applied with the gate (red and yellow in Fig. 4) represent volumes of the channel contributing to the electrical transport.

4. Discussion

In Fig. 4 we see that for increasing of V_g, we observe a gradual reduction of the transport in the center of the channel, while in the regions of the channel close to the interface channel–gate, electrical transport remain very consistent for every V_g. In fact, for $V_g >> 0$ as in Fig. 4d, the induced electrical potential is much higher (and therefore E_b is much lower) at the gate–channel interface. Henceforth, we can conclude by saying that the results of our experiments show a good agreement with our quantum simulations. Furthermore, our experimental and simulation results confirm the validity of the use of the thermionic approach to investigate transport in FET devices and are in line with what has been theoretically shown by Taur [1,7]: in undoped channel FETs, due to screening of the carriers, for a certain value of the gate voltage, transport is concentrated only in the regions close to the gate–channel interface.

5. Conclusion

By comparing our experimental results with the results of the TB simulations and with the Taur model, we have a clear demonstration of the reliability of the method, based on the thermionic fitting procedure, that we have developed in order to study transport in our FinFET devices.

This opens the way of its systematic use to obtain information about the magnitude and the position of carrier in FET devices in general. Hencefore, by the mean of our results, we have demonstrated what, to the best of our knowledge, is the first experimental implementation of a method to be used to localize and quantify the area of transport in field effect transistors. By doing this we have given some answers to the fundamental technological question on how to obtain the best FET geometry for electronic functionalities.

References

[1] H.-S.P. Wong, IBM J. Res. Develop. 46 (2002) 133.
[2] M. Nawaz, P.H., W. Molzer, Int. J. Electron. 94 (2007) 821.
[3] J. Fossum, J.-W. Yang, V.P. Trivedi, IEEE Electron. Device Lett. 24 (2003) 745.
[4] A. Burenkov, J. Lorenz, Proc. ESSDERC 2003 (2003) 135.
[5] M. Stadele, R.J. Luyken, M. Roosz, M. Specht, W. Rosner, L. Dreeskornfeld, J. Hartwich, F. Hofmann, J. Kretz, E. Landgraf, et al., Proc. ESSDERC 2004 (2004) 165.
[6] F.J.G. Ruiz, A. Godoy, F. Gamiz, C. Sampedro, L. Donetti, IEEE Trans. Electron. Devices. 54 (2007) 3369.
[7] Y. Taur, IEEE Elect. Dev. Lett. 21 (2000) 24.
[8] N. Collaert, M. Demand, I. Ferain, J. Lisoni, Singanamalla, P. Zimmerman, Y.-S. Yim, T. Schram, G. Mannaert, M. Goodwin, et al., Symp VLSI Tech. (2005) 108.
[9] H. Sellier, G.P. Lansbergen, J. Caro, S. Rogge, N. Collaert, I. Ferain, M. Jurczak, S. Biesemans, Appl. Phys. Lett. 90 (2007) 073502.
[10] J. Appenzeller, J. Radosavljevic, J. Knoc, P. Avouris, Phys. Rev. Lett. 92 (2004) 048301.
[11] N. Neophytou, A. Paul, M. Lundstrom, G. Klimeck, IEEE Trans. on Elec. Dev. 55 (2008) 1286.
[12] A. Paul, S. Mehrotra, M. Luisier, G. Klimeck, On the validity of the top of the barrier quantum transport model for ballistic nanowire MOSFETs, 13th International Workshop on Computational Electronics (IWCE) (2009), 2009, doi:10.1103/WCE.2009.5091134.