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On the validity of the top of the barrier quantum transport model for ballistic nanowire MOSFETs

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***Abstract*— This work focuses on the determination of the valid device domain for the use of the Top of the barrier (ToB) model to simulate quantum transport in nanowire MOSFETs in the ballistic regime. The presence of a proper Source/Drain barrier in the device is an important criterion for the applicability of the model. Long channel devices can be accurately modeled under low and high drain bias with DIBL adjustment.**

Keywords-component; nanowires; top of the barrier; MOSFET; ballistic transport model; DIBL; tunneling current; top-of-the-barrier; subthreshold- slope; Tight-Binding;Short channel effects .

I. INTRODUCTION

Continuous shrinking of channel length (Lc) in silicon CMOS devices to increase performance has led to the development of non-planar devices. Nanowire based Field-Effect-Transistors (FET) are an attractive candidate in this area due to better electrostatic gate control. Recently many experimental groups have demonstrated fabrication of silicon nanowire (SiNW) transistors of diameters even down to 3nm [1, 2, 3, 4, 5].

To understand the working of such small devices it is important to have proper theoretical model which encapsulates quantum transport mechanisms. A critical element in the model is the representation of the device in an atomistic Tight-Binding (TB) model [6], which understands the finite number of atoms in the structure, their local arrangement with details such as strain distribution and disorder [7, 8]. A full 3D atomistic quantum transport model [9, 10, 11] can provide the device characteristics, however, this model is computationally time consuming [12]. Recently, a 2D top of the barrier (ToB) atomistic quantum transport model [13, 14, 15] has been used for speedy simulation and analysis of SiNW FET device characteristics, which provides significant insight. However, to use the ToB model reliably, it is essential to understand the device regime where this model is valid.

In this work, the range of validity of 2D Top of the barrier atomistic quantum transport model is evaluated with a full 3D and atomistic model. Figure 1 shows that ToB inherently misses the channel length dependence; however, it can fetch accurate and fast results for long channel ballistic transistors. We observe a deviation in ToB vs. full 3D results as channel length is reduced. This difference is mostly attributed to the source/drain tunnelling current due to shrinking of the barrier

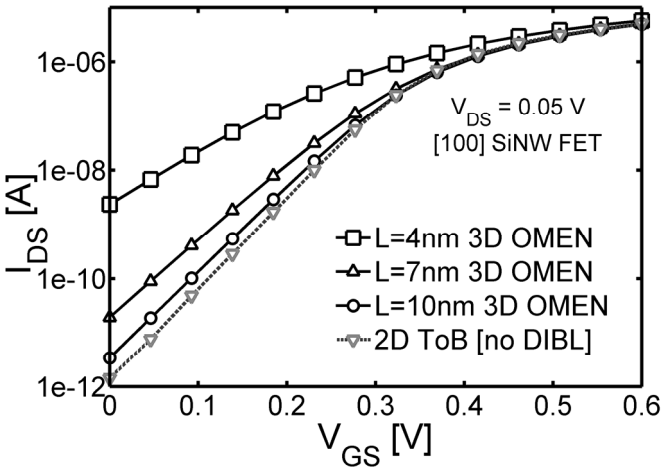

Figure 1. I_D-V_G plot obtained for a 3.1 nm × 3.1 nm, [100] square SiNW with GAA oxide using 3D OMEN for different Lc and ToB (without DIBL adjustment). At Lc=10nm, results from 2 methods are in close agreement.

width. Finally we also provide a rule of thumb for the valid simulation domain for SiNW FET devices where ToB model can be used faithfully. We also provide a comparison of compute times for the full 3D and the 2D ToB model.

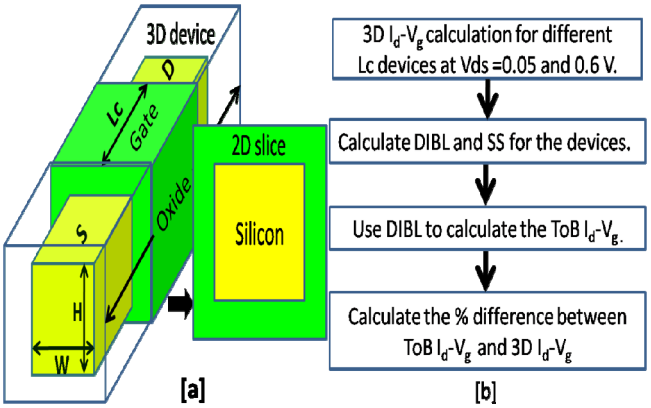

Figure 2. (a) 3D GAA SiNW MOSFET. Lc shows the gate/channel length. A 2D slice (one unitcell long) from this part is taken for ToB simulation. S and D represent source and drain respectively. W and H are silicon body width and height respectively. (b) Flowchart showing the numerical simulation approach used in this work.

II. APPROACH

Simulation Procedure: First a full 3D atomistic ballistic simulation [9, 10, 11, 16, 17, 18] is performed for gate-all-around (GAA) rectangular n-type SiNW FETs with a given cross-section width (W) and height (H), keeping W/H = 1, (Fig.2a) using OMEN [17, 18] for different gate lengths (Lc). The channel orientation is also specified for the FETs. 3D I_D-V_G simulations are done for low and high drain biases (V_{DS}). From these I_D-V_G curves DIBL is extracted. Using this DIBL value 2D I_D-V_G are simulated for exactly the same devices, using the ToB model to account for different *'channel lengths'* (Fig. 2b).

Simulation environment and devices: Square silicon nanowire FETs with cross-section size of 3.1 nm (W) X 3.1 nm (H) and Tox of 2nm are simulated using the 3D model for two different drain biases of V_{DS} = 0.05V (low) and 0.6V (high). Different channel lengths of 4, 7, 10, and 15 nm have been simulated with [100] and [110] channel orientations.The source/drain extension is 10nm with1e20cm^{-3} n-type doping. Exactly the same device structures are then simulated using the 2D ToB model.

III. RESULTS & DISCUSSION

Source/Drain tunnelling current: Figure 1 shows that I_D-V_G from ToB is in good agreement with the 3D OMEN result at low $V_{DS,}$ without any DIBL compensation, for Lc = 10nm. The deviation at shorter Lc can only be attributed to S/D tunnelling current [19, 20] under ballistic condition, which is not included in the ToB model. Fig.3a and table I shows that the sub-threshold swing (SS) becomes considerably larger than 60mV/dec (ideal ToB result) with decreasing Lc for both [100] & [110] SiNW, reflecting strong S/D tunnelling current in the OFF-state. Also [110] wires show larger SS compared to [100] wires [19], hence making them less scalable. *Thus, increased S/D tunnelling current causes 2D ToB to deviate from 3D I_D-V_G results for reduced Lc devices.*

Source to channel barrier (φ_{sc}) : Figure 4. and insets of Fig.5 and Fig.6 show that the source to channel barrier reduces as V_{GS} increases. This decrease is stronger for smaller Lc

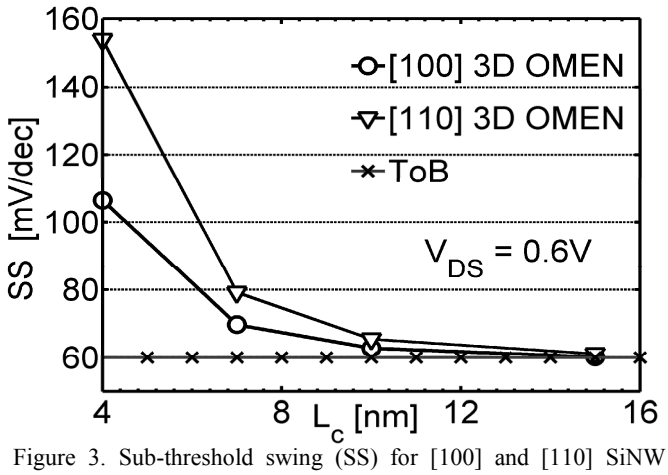

Figure 3. Sub-threshold swing (SS) for [100] and [110] SiNW FETs obtained from full 3D OMEN. ToB results in the ideal 60 mV/dec SS.

*DIBT is Drain Induced Barrier Thinning

TABLE I. SHORT-CHANNEL CHARACTERISTICS (SCE) FOR <100> AND <110> ORIENTED SINW FETS OBTAINED FROM OMEN [3] AND THE VALID SIMULATION REGIME FOR TOB.

Lc nm	SS (mV/dec)		DIBL(mV/V)		ToB valid	
	100	110	100	110	100	110
4	106.4	158.2	175.4	201.2	No	No
7	69.71	80.1	70.92	80.27	No	No
10	62.80	63.6	11.58	13.69	Partly	Partly
15	60.19	60.89	4.17	4.04	Yes	Yes

devices (Fig.4). ToB shows a strong deviation from 3D I_D-V_G results since the source to channel barrier becomes much smaller than the KT/q limit and causes an excessive S/D tunnelling current to flow. *Thus, existence of proper source to channel barrier is important for ToB to match 3D results*.

Longer Lc devices: To obtain the device regime where ToB provides reliable results, it is important to understand the effect of gate and drain electrostatics on the source to channel barrier. Figure 5 shows that ToB provides good agreement to 3D results for Lc = 15nm (long channel) in the OFF-state since the *S/D barrier is well defined* at low V_{GS} & high V_{DS} and also the *tunnelling current is minimal* due to longer Lc. However, in the ON-state ToB current is smaller compared to 3D under high V_{GS} and V_{DS}. As V_{GS} increases, the S/D barrier decreases, as a result carriers injected at the source side are no more reflected by the barrier. To ensure charge neutrality in the source, the electrostatic potential on the source side (φ_{sc}) decreases allowing more carrier injection causing an artificial increase in the ON-current. This is an artifact of the ballistic approximation that is not captured in ToB model and explains why the full 3D OMEN ON-current is larger at high V_{GS} (Fig.5 & 6)

Shorter Lc devices: As Lc decreases the drain bias starts to reduce the S/D barrier width (DIBT*) [20] (Fig.6 inset) causing

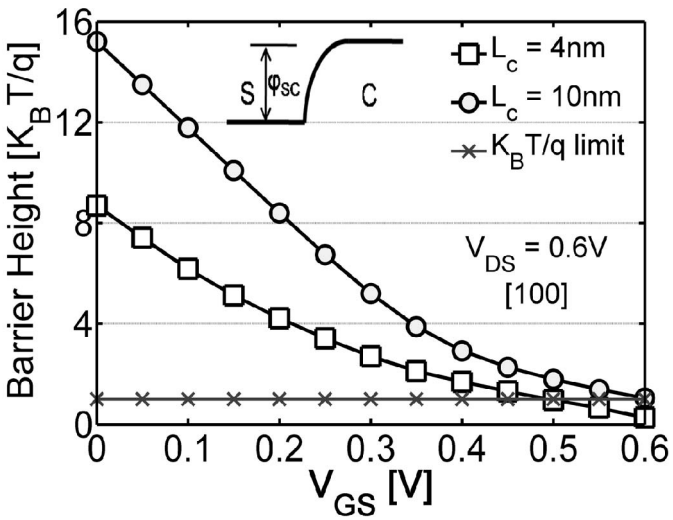

Figure 4. Source to channel barrier (φ_{SC}) height in terms of K_BT/q for [100] devices at two gate lengths. Inset shows the energy barrier between the source (S) and the channel (C).

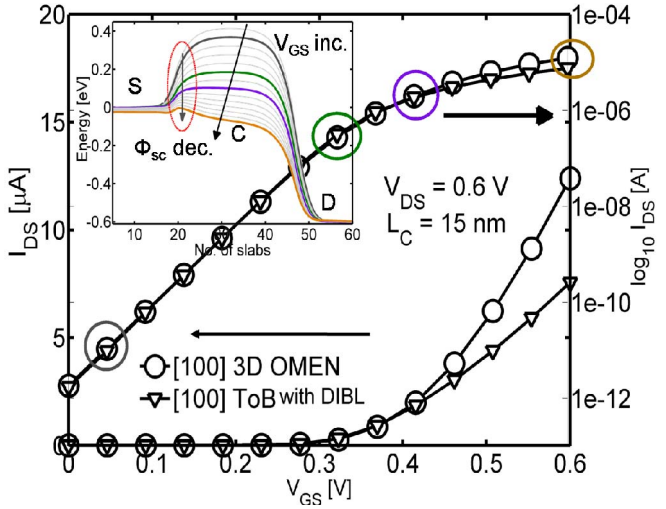

Figure 5. Long Lc I_D-V_G characteristics for ToB (with DIBL) vs. 3D OMEN for [100] SiNW, Lc = 15nm, at V_{DS} = 0.6V. Inset shows the variation in the S/D barrier at 4 different V_{GS} computed using 3D OMEN. I_{OFF} shows very good agreement; however, I_{ON} is higher for 3D.

excessive S/D tunnelling current to flow. For Lc = 4nm (short channel), ToB results are not in good agreement with full 3D OMEN anywhere (Fig.5) since the *S/D barrier is not well defined* and is below the thermal KT/q limit (Fig.4). Absence of a clear S/D barrier makes ToB inapplicable to short Lc devices. As a quantitative estimate for tunnelling current rate (R_{TUN}) (in the OFF-state) eqn. 1 is used:

$$R_{TUN} = 100 \times (J_{3D} - J_{TOB}) / J_{3D} \qquad \text{----} \qquad (1)$$

where, J_{3D}, J_{ToB} are currents from 3D and ToB simulations, respectively. Figure 7 shows that at I_{OFF}, tunnelling rate (R_{TUN}) increases dramatically with decreasing Lc , with [110] devices showing worse short channel effects (SCE) compared to [100] devices [19].

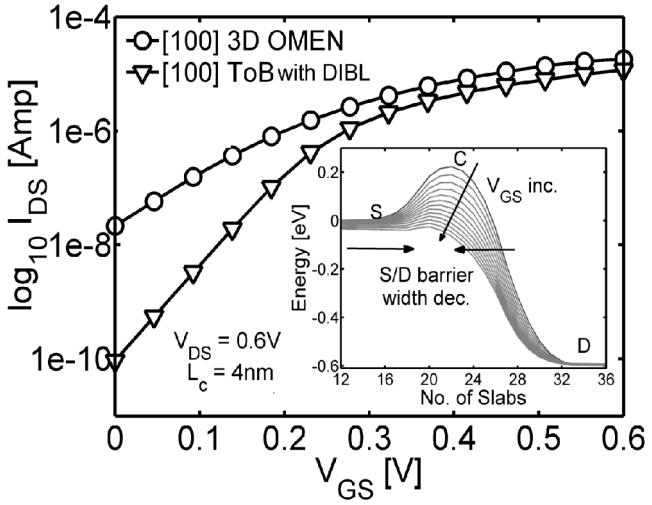

Figure 6. Short Lc comparison of I_D-V_G from ToB (with DIBL) with 3D OMEN, for [100] SiNW FET, Lc=4nm. Inset shows the S/D barrier for the device which decreases in width and height as V_{GS} increases.

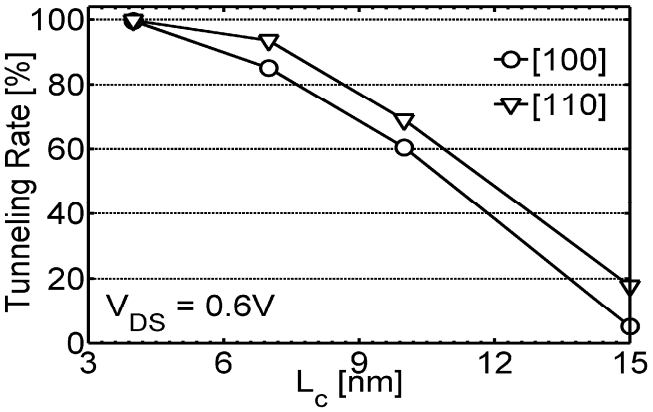

Figure 7. Tunneling current rate percentage in the off-state for [100] & [110] SiNW FETs for different Lc. Tunneling current decreases in OFF state, as Lc increases for both [100] and [110]. [110] wires have larger tunneling component hence worse short channel effect (SCE) .

Computational Speedup: One advantage of using the ToB lies in the reduced compute time compared to the full 3D OMEN atomistic quantum transport simulation. For square (W/H = 1) SiNW FETs, with longer Lc (Lc >= 5*W) devices 1 self-consistent Schrodinger-Poisson iteration time for 3D simulation goes as $W^{n3D,\ with}$ n3D = 5.63, whereas for 2D ToB it goes as W^{n2D} ,with n2D = 2.82, on a single CPU (Fig. 8). W is the silicon cross-section width (Fig.2a). The simulated devices have 1nm GAA oxide. Table II (next page) shows the actual compute times for both the models and the speedup obtained as a function of W for SiNW FETs. Speedup is defined by eqn.2. λ (eqn. 3) is the ratio of time intercepts for 3D and 2D simulation time (Fig. 8). Value of λ in Fig.8 is around 51. Speedup of 2D ToB simulations increases rapidly as W increases making it a very attractive model for device

$$\text{Speedup} = \lambda W^{(n3D - n2D)} \qquad \text{----} \qquad (2)$$

$$\lambda = C_{3D}/C_{2D} \qquad \text{----} \qquad (3)$$

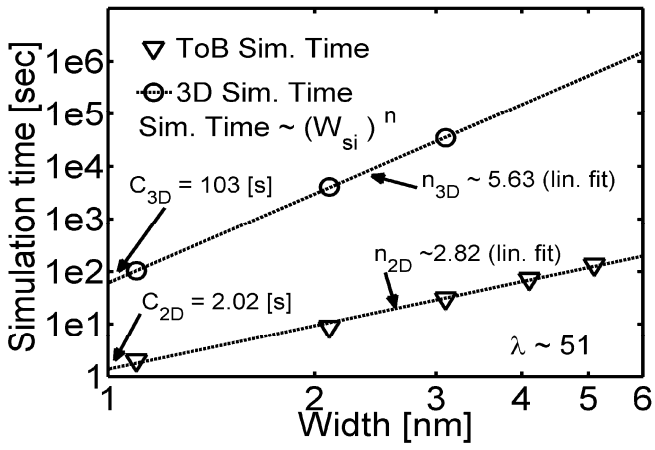

Figure 8. Simulation time for 1 self-consistent iteration for 3D OMEN vs. 2D ToB for a square SiNW with 1nm GAA oxide on 1CPU. ToB simulates ~$(Wsi)^2$ times faster compared to 3D OMEN, where Wsi is the silicon body thickness.

TABLE II. COMPARISON OF ACTUAL SIMULATION TIME FOR FULL 3D AND 2D MODEL WITH SPEED-UP ACHIEVED FROM 2D TOB MODEL FOR DIFFERENT CROSS-SECTION WIDTH (W) SINW FETS WITH 1NM GAA OXIDE.

W(width) [nm]	time[sec] (1 CPU)		Speed up ($\lambda \sim 51$)
	3D	2D	
1.1	103	2.02	66.65
2.1	4,080	8.92	410.13
3.1	35,200	30.63	1225.2
4.1	205,000	71.52	2688

simulation. Also the memory storage needed for ToB device simulation is much smaller compared to 3D simulation.

IV. CONCLUSION & OUTLOOK

Two factors are important in defining the valid device regime for ToB, (a) the presence of proper source to channel barrier ($\varphi_{sc} > KT/q$) and (b) a small source to drain tunneling current. Due to these reasons ToB compares well with 3D model for longer Lc devices. We find that for a ratio of Lc/W >= 5, that the ToB model can be used to obtain accurate 3D results. ToB is a suitable model for SiNW FETs where channel electrostatics is controlled mostly by the gate. In this regime, DIBL from experiments can be fed to ToB, to obtain accurate terminal characteristics. Computational speedup (Table II) as well as smaller memory storage requirements makes ToB a very attractive model for typical device simulation. The ToB model provides significant insight into the importance of atomistic bandstructure effects in nanowires [13, 14]. [100] and [110] wire orientations show similar short channel effects (SCE) at sufficiently long channel lengths. Table 1 elucidates the SCE and the regimes where the ToB model is applicable. It is shown that [100] n-type SiNW FETs are more scalable compared to [110] wires (Table I). The full 3D OMEN transport model is now deployed on nanoHUB.org [18] and readers can duplicate our simulation results for small diameter silicon nanowire FETs. The ToB model used in this work is also released as a part of the existing Bandstructure Lab [21] on nanoHUB.org.

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