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Metal-oxide-semiconductor field-effect transistors on GaAs (111)A surface with atomic-layer-deposited Al$_2$O$_3$ as gate dielectrics

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GaAs inversion-mode metal-oxide-semiconductor field-effect transistors (MOSFETs) with atomic-layer-deposited Al$_2$O$_3$ as gate dielectrics are fabricated on (111)A and (100) surfaces. With the same channel length of 0.75 μm, the maximum drain current of 15 mA/mm on n-channel MOSFET is obtained on (111)A surface, in great contrast to only 1 μA/mm on (100) surface. For p-channel MOSFETs, maximum drain currents of 0.17 mA/mm and 0.8 mA/mm are obtained on (111)A and (100) surfaces, respectively. An empirical model is proposed to correlate the experimental observation with the existing III-V MOS theories. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3147218]

Silicon-based complementary metal-oxide-semiconductor (CMOS) devices with traditional structures are approaching fundamental physical limits. Researchers are looking for ways to continue the trend of scaling by using alternative materials such as Ge and III-V compound semiconductors that could out-perform Si-based CMOS. Recently, an increasing number of III-V metal-oxide-semiconductor field-effect transistor (MOSFET) papers were published with high indium concentration channels showing the promising on-state device performance.[1–8] Fermi-level unpinning and strong inversion is realized in In-rich InGaAs with different gate dielectrics.[9–11] However, GaAs MOSFETs with directly deposited high-k dielectrics remain a big challenge, most showing minuscule drain currents.[12–14] Encouraging results are obtained with silicon interfacial layer, in particular, with saline passivation.[15–17] GaAs is of great importance for scientific understanding of III-V interfaces and also practical applications due to its high electron mobility, high saturation velocity, and wide bandgap. GaAs MOS devices can be used as a sensitive test bed for all dielectric techniques. The passivation technique developed on GaAs can naturally be applied to InGaAs or other III-V semiconductors.

In this letter, we systematically study the electrical properties of inversion-mode n-channel MOSFETs (NMOSFETs) and p-channel MOSFETs (PMOSFETs) on both GaAs (111)A and (100) surfaces with atomic-layer deposited (ALD) Al$_2$O$_3$ as gate dielectrics. (111)A is a pure Ga polar surface in contrast to (100) Ga–As nonpolar surface. The device work confirms that Fermi-level of GaAs (111)A surface is unpinned at the midgap with direct ALD Al$_2$O$_3$. The results obtained on GaAs (111)A surface are astonishingly different from those on GaAs (100) surface. An empirical model based on trap neutral level is proposed to correlate the experimental observation with the existing III-V MOS theories.

MOSFET fabrication starts with 2 in. semi-insulating GaAs (111)A or (100) substrates. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM F-120 ALD reactor. A 30 nm thick Al$_2$O$_3$ layer was deposited at a substrate temperature of 300 °C as an encapsulation layer. Source and drain regions were selectively implanted with Si for NMOSFETs and Zn for PMOSFETs with the same dose of 5 $\times 10^{14}$ cm^{-2} at 40 keV through the 30 nm thick Al$_2$O$_3$ layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 820 °C for 15 s in nitrogen ambient for NMOSFETs and at 750 °C for 15 s for PMOSFETs. An 8 nm Al$_2$O$_3$ film was regrown by ALD after removing the encapsulation layer by buffered oxide etch (BOE) solution and soaked in ammonia sulfide for 10 min for surface preparation. After 600 °C postdeposition anneal (PDA) in N$_2$ ambient, the source and drain Ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au for NMOSFETs or Pt/Ti/Pt/Au for PMOSFETs and a lift-off process, followed by a RTA process at 400 °C for 30 s also in a N$_2$ ambient. The gate electrode was defined by electron beam evaporation of Ni/Au and a lift-off process. It was found during the process that GaAs (111)A surface is more hydrophilic as In-rich InGaAs surface; GaAs (100) surface is more hydrophobic. Hydrophilic surface is believed to be favorable for ALD two-dimensional growth and good interface properties.[18]

The fabricated MOSFETs have a nominal channel length varying from 0.75 to 40 μm and a gate width of 100 μm. A Keithley 4200 was used for MOSFET output characteristics. The full conductance measurement was carried out using an HP4284A precision LCR meter with frequencies varying from 100 Hz to 1 MHz. For the above process, the contact resistance on (111)A surface is 0.28 Ω mm for NMOSFET and 3.3 Ω mm for PMOSFET, and the sheet resistance is 180 Ω/sq for Si implanted n-type area and 4900 Ω/sq for Zn implanted p-type area. The contact resistance on (100) surface is 0.43 Ω mm for NMOSFET and 46.8 Ω mm for PMOSFET, and the sheet resistance is 550 Ω/sq for Si implanted n-type area and 30150 Ω/sq for Zn implanted p-type area. All these values are determined by the transmission line model method. Due to relatively larger lattice spacing on (111)A crystal plane, the contact resistance and sheet resistance obtained on (111)A are better than those on (100) under the same implantation and activation conditions.

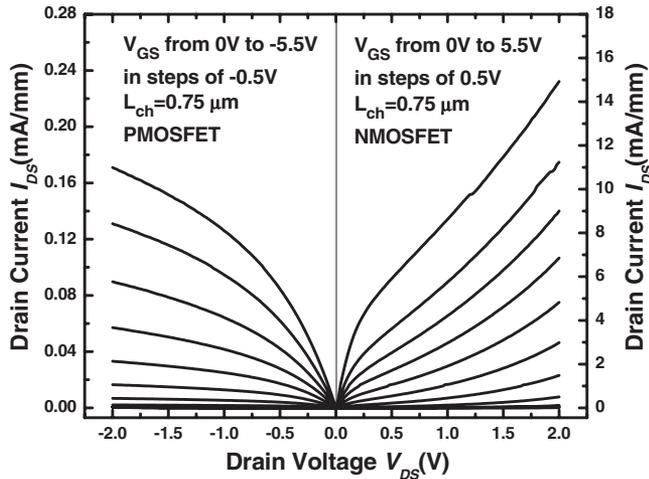[a]Author to whom correspondence should be addressed. Electronic mail: yep@purdue.edu.

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FIG. 1. *I-V* characteristics of a NMOSFET and a PMOSFET with 8 nm Al_2O_3 as gate dielectric.

FIG. 2. $G/\omega - V_g - f$ plot measured on the same NMOSFET clearly showing the Fermi-level movement at inversion region with the gate bias. The dashed white line is guide to the eyes.

The drain current in an inversion-mode MOSFET is the detrimental tester for Fermi-level pinning or unpinning. Figure 1 shows the well-behaved *I-V* characteristics of both NMOSFET and PMOSFET on GaAs (111)A with channel length of 0.75 μm. The maximum inversion drain current is 15 mA/mm for NMOSFET, which is among the highest values in inversion-mode GaAs MOSFETs with directly deposited oxides.[12–14] We ascribe the short-channel-effect like low output conductance on the 0.75 μm NMOSFET to lateral interdiffusion of Si dopant implanted at source/drain regions and activated at 820 °C. It is significantly improved at channel length ≥ 2 μm (not shown). The simple MEDICI simulation shows that only 0.2 pA/mm drain current is expected even without accounting interface traps if the Fermi-level is pinned at the midgap of GaAs with 0.75 μm channel length and $V_{ds} = 2$ V. From the simulation, Fermi-level in the channel region must be less than 0.05 eV near the conduction band minimum (CBM) for drain current of 15 mA/mm due to nearly two orders of magnitude lower effective density of states at CBM in GaAs than Si. The drain current for PMOSFET is 0.17 mA/mm, which is about two orders of magnitude lower than that for NMOSFET. However, it is not so surprising if we consider the hole mobility in bulk GaAs is 20 times smaller than the electron mobility. The contact resistance on fabricated PMOSFET is 3.3 Ω mm, which is also one order of magnitude higher than 0.28 Ω mm on NMOSFET.

The conductance method is widely used to quantitatively evaluate interface trap states within the semiconductor bandgap. At any given frequency of ac gate voltage, the energy loss from charge trapping and detrapping at $Al_2O_3/GaAs$ interface states depends both on the speed of response of interface traps and on the interface trap density near the Fermi level at GaAs surface. The energy loss, measured as an equivalent parallel conductance G, has its maximum when the energy level of the trap states is aligned with the GaAs surface Fermi level. The full $G/\omega - V_g - f$ measurement is developed by utilizing the location of the normalized conductance peaks to illustrate the Fermi-level movement at the $Al_2O_3/GaAs$ interface, because the measured frequency is transformable to the detected trap energy level and Fermi level in the bandgap.[19] Figure 2 shows an ensemble of $G/\omega - V_g$ measurements at 30 different frequencies between
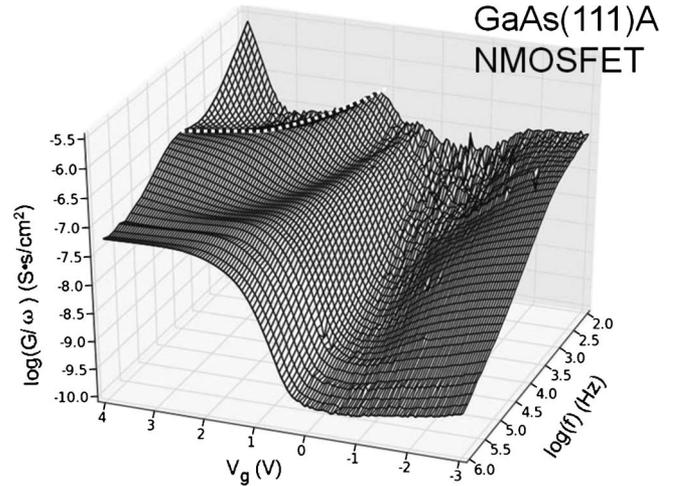
100 Hz and 1 MHz on the same 0.75 μm GaAs (111)A NMOSFET. The dashed white line illustrates the Fermi-level movement versus gate bias within GaAs bandgap at the $Al_2O_3/GaAs$ interface. The conductance peaks are from the inverted minority carriers (electrons for NMOSFETs). No conductance peaks from majority carriers are observed since it is fabricated on semi-insulating substrates. Tracing by the conductance peak, Fermi-level is clearly moved by changing the gate bias. The interface trap density D_{it} of $\sim 2 \times 10^{12}$ cm^2 eV is determined at upper half bandgap of GaAs (111)A from the measured magnitude of conductance peaks. Similar Fermi-level movement from tracing the conductance peaks is also observed on PMOSFETs where the energy loss is from trapping and detrapping of minority carrier holes (not shown).

Surprisingly, NMOSFETs processed at the same time on GaAs (100) substrates with the same gate length and oxide thickness have the maximum drain current of only ~ 1 μA/mm. Meanwhile, PMOSFETs on GaAs (100) have the maximum drain current of 0.8 mA/mm, a factor of five larger than that on GaAs (111)A. All these seemingly randomly distributed experimental results are well explained by the following proposed empirical model as shown in Fig. 3. It is based on the unified disorder induced gap state (DIGS) model proposed by Hasegawa and Ohno[20] in 1986, which explains the striking correlation between the energy location
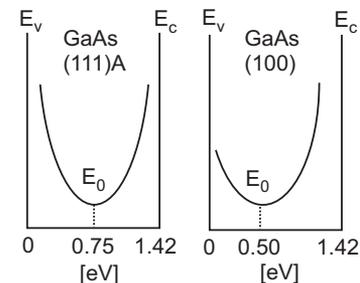

FIG. 3. Empirical model after Refs. 20–22. 0.75 eV is associated with a missing anion due to Ga (111)A surface; 0.5 eV is associated with a missing cation, which is the case most likely for (100) or (110) (Ref. 22). The minimum D_{it} and U-shape curvature depends on processing conditions, while the location of E_0 remains constant for each semiconductor with the same crystal facet.

$E_{\min}$ for the minimum interface state density at the insulator-semiconductor interface and the Fermi-level pinning position E_{pin} of the metal-semiconductor interface. The central concept is that there is an energy level called trap neutral level E_0 at the high-k/GaAs interface,[21] above which the trap states are of acceptor type or electron traps and below which are of donor type or hole traps. E_0 is at the same or similar energy level as $E_{\min}$, E_{pin}, and E_{HO} in Ref. 20. By photoemission and other experiments, Spicer *et al.*[22] discovered that E_{pin} in GaAs is 0.75 and 0.5 eV above the valence band maximum (VBM). The first energy given is associated with a missing anion (As) and the second with a missing cation (Ga). Ignoring the complications of surface reconstructions, GaAs (111)A surface is a Ga-terminated polar surface, which can be regarded as a missing anion (As) surface with E_0 =0.75 eV above VBM.[22,23] GaAs (100) is a Ga-As terminated nonpolar surface which might be more related with missing cations with E_0=0.5 eV above VBM, as shown in Fig. 3. The drain current strongly depends on the energy separation between E_0 and CBM for NMOSFET or VBM for PMOSFET. With the measured near midgap interface trap density D_{it} of 2×10^{12} cm^2 eV, the less the separation is, the less traps are filled in to prevent further Fermi-level movement for strong inversion, the more inversion charge and drain current can be achieved.[21] This model explains why NMOSFET on GaAs (111)A outperforms that on (100), and PMOSFET on GaAs (100) outperforms that on (111)A. It also explains why the frequency dispersion in accumulation is much better for PMOS capacitors than for NMOS capacitors on (100) and why it is similar on (111)A (not shown).

In conclusion, GaAs inversion-mode MOSFETs with ALD Al$_2$O$_3$ as gate dielectrics are fabricated on (111)A and (100) surfaces. Maximum drain current of 15 mA/mm is obtained on GaAs (111)A NMOSFET with the channel length of 0.75 μm. The original surface condition and the chemical based surface preparation before the dielectric deposition is the key to realize the unpinning of the Fermi level on GaAs. For example, Fermi level on GaAs (100) with SiH$_4$ passivation has recently been demonstrated unpinned.[16,17] Even the large discrepancy of 1 μA/mm drain current reported in this Letter and 4.5 mA/mm reported in Ref. 14 on GaAs (100) NMOSFETs using the same directly ALD Al$_2$O$_3$ as gate dielectrics could be related with some detailed difference on surface chemistry and process. Fermi-level pinning at the midgap of GaAs as proposed by the unified defect model[22] can be overcome by the appropriate surface preparation and the right dielectric deposition technique. More systematic studies on GaAs (111)B, (110), and (100) surfaces are ongoing for more conclusive experimental evidences. After submission of this manuscript, we became aware of the theoretical work with more accurate description of the related model.[24]

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