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Using a three-dimensional, atomistic quantum transport simulator based on the tight-binding method, we investigate statistical samples of single-gate graphene nanoribbon (GNR) tunneling field-effect transistors (TFETs) with different line edge roughness probabilities. We find that as the nanoribbon edges become rougher, the device OFF-current drastically increases due to a reduction of the graphene band gap and an enhancement of source-to-drain tunneling leakage through the gate potential barrier. At the same time, the ON-current remains almost constant. This leads to a deterioration of the transistor subthreshold slopes and to unacceptably low ON/OFF current ratios limiting the switching performances of GNR TFETs. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3140505]

The functionality of tunneling field-effect transistors (TFETs) with a subthreshold slope (SS) better than 60 mV/decade at room temperature has recently been experimentally demonstrated using a carbon nanotube[1] and a silicon-on-insulator[2] structure. Many theoretical studies have shown that tunneling transistors with steep subthreshold slopes could also be realized with other materials and/or configurations such as InAs (Ref. 3) nanowires, SiGe (Ref. 4) ultrathin bodies, or graphene nanoribbons (GNRs).[5,6]

TFETs based on graphene nanoribbon are especially interesting since they are expected to offer larger ON-currents, lower OFF-currents, and steeper SS than Si or III-V compound semiconductors, they are one-dimensional (1D), fully compatible with planar processing, and they have light and identical conduction and valence band effective masses as well as a width-tunable narrow band gap. Reference 5 theoretically predicts a subthreshold swing SS $=0.19$ mV/decade, an ON-current $I_{on}=800\ \mu A/\mu m$, and OFF-current $I_{off}=26$ pA/μm for a 5 nm wide GNR device with a gate length $L_g=20$ nm. In that work a 1D simulation approach based on the Wentzel-Kramers-Brillouin (WKB) approximation[7] and ideal GNR structures are used.

It seems, however, rather difficult to perfectly control the width of sub-10-nm GNRs and to avoid line edge roughness (LER).[8] The resulting variations of the ribbon dimensions cannot be captured by a 1D approach and require multidimensional simulation capabilities. Using a three-dimensional (3D), atomistic, quantum mechanical simulator,[9] we investigate the performance limitations of single-gate, 5.1-nm-wide, *p-i-n* GNR TFETs with a 40 nm gate contact and rough ribbon edges. Through quantitative simulation of realistically extended nonideal structures and statistical sampling of different random configurations we can address the LER issue and provide some insight into the physics that governs this effect.

After a brief description of the simulation approach, we will demonstrate that source-to-drain tunneling leakage through the gate potential barrier (i) increases with LER probability and (ii) strongly limits the ON/OFF current ratios and SS of devices with a LER probability of 10% to 22 and 70 mV/decade, respectively. The same quantities calculated in an ideal GNR TFET without LER are found to be 6080 for the ON/OFF ratio and 12 mV/decade for SS.

Our 3D, atomistic and ballistic quantum transport solver is based on a wave function approach with open boundary conditions, which is equivalent to the nonequilibrium Green's function formalism but numerically much more efficient.[9] The carbon atoms are described in a single-orbital p_z tight-binding model[10] with a coupling factor $t=-3.0$ eV. The insulator layers are modeled as fictitious materials with an infinite band gap and are only characterized by their relative dielectric constant ϵ_r. Electrons and holes are injected at different energies from the source and drain contacts to calculate charge density, which is self-consistently iterated with the solution of Poisson equation. Electrons that tunnel from the valence band of the *p*-doped side of the device into the conduction band of the *n*-doped side contribute to both the current and charge densities.

We consider 5.1-nm-wide ($N=21$), 90-nm-long armchair graphene nanoribbons with a band gap $E_g=0.25$ eV as the active components of single-gate, *p-i-n* TFETs with a gate length $L_g=40$ nm. The device structure is sketched in Fig. 1. Single-gate transistors are preferred to double-gate ones because they are easier to fabricate and produce less gate leakage currents through the insulator layers (not considered here).

The GNRs are deposed on a SiO_2 substrate (5 nm taken into account in the simulation domain, $\epsilon_r=3.9$) and separated from the gate contact by a 2.35 nm Al_2O_3 insulator ($\epsilon_r=9.1$, equivalent oxide thickness EOT=1 nm). The gate metal work function $\phi_M=4.45$ eV is chosen in such a way that the transistor OFF-state is aligned with $V_{gs}=0.0$ V. A supply voltage $V_{DD}=0.2$ V is applied to minimize power consumption and to make sure that $V_{bi}+V_{DD}<2E_g$, where $V_{bi}=0.27$ V is the built-in voltage of the *p-i-n* structures. This is the necessary condition to shut down the ambipolar tunneling channels in the transistor OFF-state, as can be seen in Fig. 2(a). LER is generated by randomly removing pairs of carbon atoms from the edges of a perfect $N=21$ armchair ribbon with a probability P comprised between 0% and 10%

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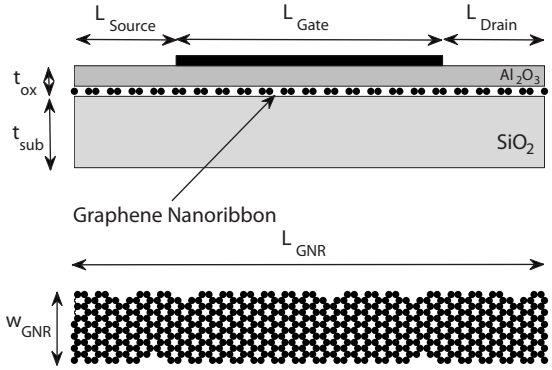

FIG. 1. (Top) Schematic of a *p-i-n* graphene nanoribbon (GNR) tunneling transistor where the GNR is deposed on a SiO_2 insulator layer. The gate contact has a length L_g=40 nm and is separated from the channel by an Al_2O_3 layer of thickness t_{ox}=2.35 nm (ϵ_r=9.1, EOT=1 nm). The *p*-doped source and *n*-doped drain extensions both measure 25 nm. A thickness t_{sub}=5 nm of the SiO_2 layer is included in the simulation. (Bottom) Example of an armchair GNR with line edge roughness. All the simulated GNRs have a width w_{GNR}=5.1 nm and a total length L_{GNR}=90 nm.

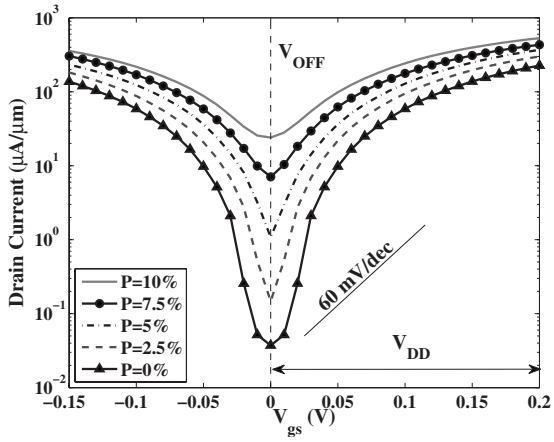

FIG. 3. Transfer characteristics I_d-V_{gs} at $V_{ds}=V_{DD}$=0.2 V of GNR tunneling transistors with line edge roughness. For each probability *P*, 90 different samples are simulated, the mean current value at each voltage is shown here. The current is normalized with the GNR width w_{GNR}=5.1 nm.

in step of 1.25%.[11–13] 90 different GNR samples are simulated at room temperature for each probability *P* for a total of more than 700 simulations.

The transfer characteristics of an ideal GNR TFET without LER is given in Fig. 3 (solid line with triangles). Such a device exhibits a OFF-current I_{off}=0.037 μA/μm (I_d at V_{gs}=0.0 V and $V_{ds}=V_{dd}$ normalized with the GNR width), an ON-current I_{on}=225 μA/μm (I_d at $V_{gs}=V_{ds}=V_{dd}$), an ON/OFF current ratio of 6080, and a subthreshold swing SS=12 mV/decade. These performances are poorer than those reported in Ref. 5 for a similar device structure but they are still encouraging. We think that our results are more realistic since we do not assume a 1D geometry and we account for the ambipolar behavior of the GNR TFETs and the leakage through the gate potential barrier.

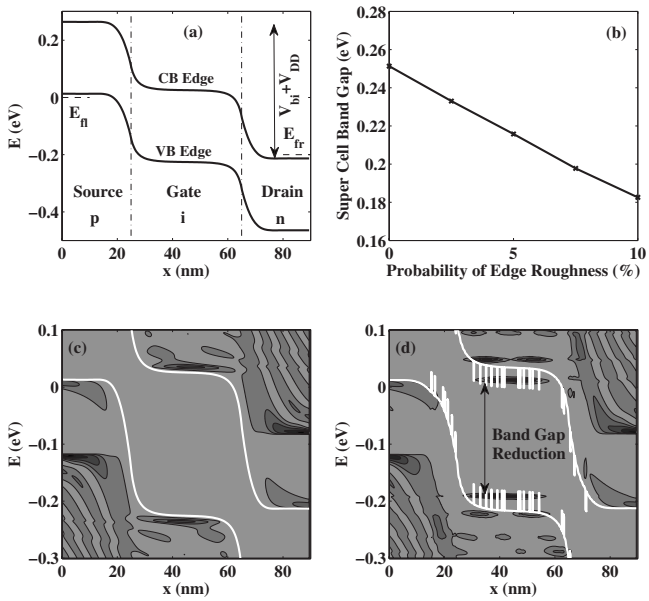

FIG. 2. (a) Band edges of a GNR tunneling transistor without LER in its off-state (V_{gs}=0.0 V, $V_{ds}=V_{DD}$ V). The source Fermi level E_{fl} is situated 10 meV below the VB edge, the drain Fermi level E_{fr} 10 meV above the CB edge. The total potential drop from source to drain corresponds to the built-in potential V_{bi}=0.27 eV plus the applied voltage V_{DD}. (b) Band gap of 5.1-nm-wide graphene nanoribbons composed of identical supercell with a LER probability *P* between 0 and 10%. Subplots (c) and (d) show the density-of-states of the transistor in its OFF-state without (c) and with (d) LER as well as the conduction and valence band edges. States below the CB and above the VB edges in (d) indicate a reduction of the GNR band gap due to LER.

The inclusion of LER tends to decrease the band gap of the 5.1 nm-wide GNRs due to the presence of atomic layers with *N*=20 atoms embedded between layers with *N*=21 elements as illustrated in Fig. 2(b)–2(d). The calculation of the bandstructure of GNRs which are perturbed by various LER probabilities provides some insight into the underlying physics. For that purpose a supercell approach[14] is used and the resulting band gaps are reported in subplot (b). For each probability *P* a ribbon is constructed by repeating the same unit cell along the transport direction *x*. These so-called "supercells" are larger than the primitive unit cell of graphene and its four atomic layers and their size is fixed so that by removing two carbon atoms from them the desired LER probability is obtained. For example the supercell corresponding to a LER probability *P*=10% is composed of 20 atomic layers whose two arbitrary, but consecutive layers have a missing carbon atom. To model a LER probability *P*=5% the supercell is made of 40 atomic layers. The band gap of the 5.1-nm-wide GNRs calculated using the supercell bandstructure linearly decreases from E_g=0.25 eV to E_g=0.18 eV as *P* increases from 0 to 10%.

The ribbon band gap is only locally reduced where edge atoms are missing, as shown in Fig. 2(d). If several layers with missing edge atoms are close to each other they form a kind of superlattice structure that eventually contains localized gap states situated below (above) the conduction (valence) band of the ideal structure without line edge roughness.[11,13]

This effective band gap reduction leads to an enhancement of the tunneling leakage from source to drain as indicated in Fig. 2(c) and 2(d). Without LER, the conduction band (valence band) edge under the gate contact is higher (lower) than the valence band (conduction band) edge in the source (drain) in the transistor OFF-state so that all the tunneling channels are closed. The presence of LER breaks this condition and opens an upper and lower tunneling leakage channel. This could be partly avoided by reducing the built-in voltage V_{bi} so that the condition $V_{bi}+V_{DD}<2E_{g,red}$, where $E_{g,red}$ is the reduced band gap, is still valid, but the

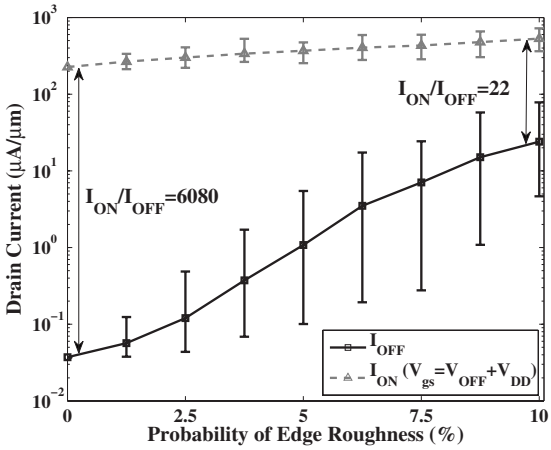

FIG. 4. OFF-current ($V_{gs}=V_{OFF}=0.0$ V, $V_{ds}=V_{DD}=0.2$ V) and ON-current ($V_{gs}=V_{OFF}+V_{DD}$, $V_{ds}=V_{DD}$) as function of the LER probability. The average of 90 samples per LER probability and the corresponding error bars of the lowest and highest values are reported. The ON/OFF ratios at $P=0$ and $P=10\%$ are also given.

strength of the electric field at the *p-i* interface and consequently the ON-current would also decrease.

Figure 3 reports the mean transfer characteristics I_d-V_{gs} of GNR TFETs with different LER probability P. Each curve is the average of 90 randomly generated samples. The evolution of the OFF- and ON-currents as function of P is summarized in Fig. 4 as well as the error bars of the lowest and highest value at each LER probability. The mean OFF-state current rapidly increases when P increases to reach a value $I_{off}=24$ $\mu A/\mu m$ at $P=10\%$. The average ON-current does not go beyond 530 $\mu A/\mu m$, reducing the ON/OFF ratio to an unacceptable value of 22. The standard deviation σ_{off} of the OFF-current from its mean value is 14 $\mu A/\mu m$ at $P=10\%$, while σ_{on} amounts to 70 $\mu A/\mu m$.

We have performed 3D simulations of GNR tunneling transistors including line edge roughness. A strong deterioration of the device performances is predicted. LER reduces the GNR band gap and increases source-to-drain tunneling leakage. It is therefore identified as a crucial design parameter for GNR TFETs that might be even more important in narrow ribbons with $w_{GNR}<5$ nm. Furthermore, the large current variations from device to device in addition to the poor ON/OFF current ratios obtained in the presence of LER need to be resolved before GNR TFETs can be used as low power logic gates in integrated circuits.

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