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Capacitance–Voltage Characterization of GaAs–Oxide Interfaces

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We will shortly review the basic physics of charge-carrier trapping and emission from trapping states within the bandgap of a semiconductor in order to show that high-temperature capacitance–voltage (C–V) measurements are necessary for GaAs metal–oxide–semiconductor characterization. The midgap trapping states in GaAs have characteristic emission times on the order of 1000 s, which makes them extremely complicated to measure at room temperature. Higher substrate temperatures speed up these emission times, which makes measurements of the midgap traps possible with standard C–V measurements. C–V characterizations of GaAs/Al2O3, GaAs/Gd2O3, GaAs/HfO2, and In0.15Ga0.85As/Al2O3 interfaces show the existence of four interface state peaks, independent of the gate oxide deposited: a hole trap peak close to the valence band, a hole trap peak close to midgap energies, an electron trap peak close to midgap energies, and an electron trap peak close to the conduction band.

In the past few years a growing interest in passivation of III–V surfaces has emerged again. Several problems exist, nevertheless, with the characterization of these interfaces, leading to some confusion in the literature. These problems have three main causes: First of all, these interfaces present very high densities of interface states, which leads to weak Fermi level pinning and Fermi level pinning behavior at the surfaces, phenomena rarely observed at Si surfaces. Also the interface state distributions are quite different from the "U"-shaped Si interface state distributions. Finally, the relatively larger bandgap of some III-V semiconductors as compared to Si leads to time constants of interface traps well above the usual time constants observed at Si surfaces, creating very long time constant phenomena, not observable with routine capacitance–voltage (C–V) characterization techniques. A possible solution to all of these problems is the photoluminescence intensity characterization technique, which is a fast measurement technique that has the big advantage of being sensitive to the integral of all interface states present at the III-V surface. Some disadvantages are the relative insensitivity of the technique in the range of 10^{12}–10^{15} interface states/cm², a range in which the largest majority of III-V interfaces unfortunately reside, as well as the difficulty to extract energy distributions of interface state densities (D(E)). In this contribution we apply a different technique, the conductance method, and we apply it at different temperatures, which allows the extraction of interface state density over the whole bandgap of GaAs or In0.15Ga0.85As. First, some general theory is presented, followed by the presentation of experimental measurements on different GaAs and InGaAs metal–oxide–semiconductor (MOS) capacitor samples with Al2O3, Gd2O3, and HfO2 gate dielectrics.

Measurement Method

C–V measurements are made on MOS structures. The band diagram of a typical MOS structure is shown in Fig. 1, where a gate voltage (\(V_g\)) is applied between the metal and the semiconductor, which fixes the value of the surface Fermi level (\(E_f\)). A hypothetical interface state distribution at the semiconductor–oxide interface is also shown on the band diagram. The C–V measurements consist in applying on top of the static gate bias voltage a small sinusoidal voltage with frequency \(f\) and amplitude of the order of 30 mV. This small periodic gate voltage causes the bands and the surface potential in the semiconductor to periodically move up and down, causing the interface traps lying around the value of the surface potential to fill and empty. Only if the traps around the surface potential have a characteristic response time that is of the order of the measurement frequency \(f\) can they interact with the measurement ac signal and affect the total impedance of the MOS capacitor.

\[ M \quad O \quad S \]

\[ E_f \quad \text{eV}_g \]

Figure 1. Band diagram of an n-type MOS structure with a bias voltage \(V_g\) applied between metal and semiconductor. A hypothetical interface state distribution is shown as well, with the interface traps filled up to the surface Fermi level (dark shaded region). A small ac voltage is applied on top of the gate bias, represented by the vertical arrows, which moves the semiconductor bands and surface Fermi level up and down, causing the traps within the oscillation amplitude (brighter shaded region) to periodically fill and empty. This filling and emptying of the interface traps allows for measurement of interface state distribution from C–V measurements.

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Therefore, the characteristic times related to carrier trapping and emission are very important properties which should be studied in detail.

The characteristic time \( \tau_c \) with which a trapped charge in a semiconductor is emitted from a trapping state of energy \( E_t \) can be determined from standard Fermi–Dirac statistics and is given by:

\[
\tau_c = \tau_1 \exp(\Delta E/kT)
\]

where \( \Delta E \) is the energy difference between the majority carrier band-edge energy and the trapping state energy \( E_t \), \( k \) is the Boltzmann constant, \( T \) is the semiconductor temperature, and \( \tau_1 \) is the charge carrier trapping time constant, given by:

\[
\tau_1^{-1} = \sigma v T N
\]

where \( \sigma \) is the capture cross section of the trapping state, \( v \) is the thermal velocity of the majority charge carriers, and \( N \) is the density of states in the majority carrier band. From this characteristic emission time \( \tau_c \), one can derive the characteristic response frequency \( f_c \), which is 1/2\( \pi \tau_c \) of the corresponding trapping state. This equation shows that the characteristic emission frequency depends exponentially on the depth of the trapping state in the bandgap. The further the trap is away from the bandedge, the slower it will emit a trapped charge.

Figure 2 shows the characteristic emission frequency of traps in Si as a function of the position of the trap in the bandgap. Both the emission times for electrons (solid line) and holes (dashed line) are shown in the figure. The valence band energy corresponds to the origin of the horizontal axis. Concerning the parameter values from Eq. 1, the thermal velocity and density of states are well-known and well-defined values for a specific semiconductor, whereas the capture cross section depends strongly on the nature of the trap. The capture cross section can take values varying from \( 10^{-12} \) to \( 10^{-20} \) cm\(^2\). Even larger values than \( 10^{-12} \) cm\(^2\) cannot be excluded. Nevertheless, the largest majority of trapping states has capture cross sections of the order of \( 10^{-14} \) cm\(^2\), which is the value that we adopted for the graph in Fig. 2. Possible deviations from this value will of course have an effect on the emission time, although the strongest dependency is still the exponential term. In the following, a capture cross section of \( 10^{-14} \) cm\(^2\) is assumed in order to illustrate the effects of the characteristic emission time constant.

From Fig. 2 it becomes apparent that only small portions of the bandgap can be measured with common C-V measurement equipment, which usually measures in the frequency range 100 Hz to 1 MHz. The traps at the majority carrier bandedges have characteristic frequencies which are way too fast to be measured with common C-V equipment, whereas the deeper traps are usually too slow. In Si, nevertheless, we can see that the full midgap region can be measured with C-V measurements, the range 0.25–0.55 eV above the valence band with p-type MOS (p-MOS) capacitors and the range 0.55–0.8 eV above the valence band with n-type MOS (n-MOS) capacitors. Sweeping the gate bias voltage will sweep the position of the surface potential over the bandgap. When the surface potential meets a trap level with characteristic emission time equal to the measurement frequency, the capacitance and resistance of the traps at this particular position in the bandgap will be measured by the C-V equipment, thereby allowing the extraction of information on interface state density as a function of position in the bandgap. Whereas this works reasonably well for Si, where the full midgap region can be measured if one combines n- and p-type MOS measurements, this is not the case for higher bandgap materials, such as GaAs. Figure 3 shows the characteristic charge emission times from traps in the GaAs bandgap, assuming again a capture cross section equal to \( 10^{-14} \) cm\(^2\). This time the situation is completely different from the Si case. Similar to Si, only small portions of the bandgap can be measured, but this time, because of the large bandgap of GaAs, the midgap trapping states cannot be measured, neither on p-type nor on n-type MOS capacitors. These midgap traps have characteristic emission frequencies on the order of \( 10^{-3} \) s\(^{-1}\), which corresponds to characteristic times of the order of 1000 s. Once a charge carrier is trapped in such a midgap trap it can stay in the trap for several tens of minutes to hours. With our equipment that measures at frequencies of 100 Hz to 1 MHz, we will of course never be able to measure these extremely slow traps. We are completely blind to the trap density at these positions in the bandgap, as they lie completely out of the measurement range. They might just eventually show up in the measurements as hysteresis, which appears as the charge carriers very slowly detrap from the interface state, thereby reducing the charge at the interface.

One possible way to solve this problem and to still measure these GaAs midgap traps is to perform quasi-static C-V measurements but with extremely long integration times in excess of 1 s. A full quasi-static C-V measurement takes then about 1 h or longer. Such a low
The emission time constants. Heating the semiconductor with a more elevated temperature. The temperature in Eq. 1 gives us the slow midgap states in GaAs, which is to thermally activate them up to 150°C in order to be able to measure the interface trap distribution in the bandgap. This proportionality between characteristic trap frequency and measurement frequency at which the maximum occurs.

\[ D_\theta(V_g) = 2.5 \frac{G_{\theta,\max}}{A_{qq}} \]

Here \( A \) is the area of the MOS capacitor under testing, \( \omega = 2\pi f \), and \( q \) is the charge of the majority charge carrier. Determining the maximum of \( G_{\theta}/A_{qq} \) as a function of frequency for different bias voltages, for which the device is in depletion, will provide us with a measure of the interface state density as a function of the position in the bandgap. This proportionality between \( D_\theta \) and \( G_{\theta}/A_{qq} \) holds only for interface state densities for which \( G_{\theta}/A_{qq} < C_{ox}^{-1} \).

In principle, the conduction method relies on the extraction of the flatband voltage in order to position the interface state distribution in the bandgap relative to this flatband voltage position. One can then determine the capture cross section of the trap states. This flatband voltage extraction is nevertheless impossible for III-V devices with large interface state densities, so we have to rely on the assumption of a reasonable capture cross section if we want to position our interface state distribution in the bandgap. This leads to an uncertainty concerning the absolute position of the interface state positions in the bandgap. The error will be larger the further the real trap capture cross section is off with respect to our assumed value of 10^{-14} cm^2.
Sample Preparation

Several GaAs samples were prepared on both 5 × 10^17 cm⁻³ n-type doped substrates and on 5 × 10^17 cm⁻³ p-type doped substrates. The In_{0.53}Ga_{0.47}As layers were deposited by metalorganic chemical vapor deposition and are 30 nm thick and also 5 × 10^17 cm⁻³ n- and p-type doped. The HfO₂ and Al₂O₃ samples were treated with an HCl wet clean before being introduced into an ASM Pulsar atomic layer deposition reactor. Using alternating pulses of H₂O and trimethylaluminum or HfCl₄ as precursors, 10 nm of Al₂O₃ or HfO₂ were deposited at 300°C. The Gd₂O₃ samples were deposited through a shadow mask.

Results

In order to get a good continuous picture of the movement of the surface potential and interface state distribution, we measured C-V curves with 25 frequencies varying logarithmically from 100 Hz to 1 MHz. Figure 6 shows all the C-V curves and Gₚ/Auq as a function of frequency and bias voltage (conductance map) for the GaAs/Al₂O₃ samples. As explained in the previous section, for GaAs MOS interface characterization it is not sufficient to make room temperature measurements. For the characterization of the interface, 25 and 150°C measurements should be made on both n- and p-type MOS. Figure 6 shows the four different measurements. Every one of the four measurements probes a different region in the GaAs bandgap, as witnessed by the vertical axis of the conductance maps, which is directly expressed in bandgap energy. For clarity, the measurement frequency is shown on the right side axis of the conductance map. The bandgap energy is derived from the measurement frequency through Eq. 1, assuming a capture cross section of 10⁻¹⁴ cm². Deviations of the real capture cross section from this value will result in an energy shift of the features observed. We therefore have a relatively large uncertainty on the real energy position of the features we observe. Deep-level transient spectroscopy measurements are currently being made on these samples in order to determine the real value of the capture cross section. The four measurements show how the surface potential moves over the measurement range as the bias voltage is varied. What can be seen is how the conductance responses from different trap levels with different characteristic time constants are measured as the applied gate voltage sweeps the surface Fermi level over the bandgap. For the room temperature measurement of the p-type sample, the Fermi level can move over the full measurement range, as witnessed by the response which runs from about 0.3 eV above the valence band at Vₚ = −1 V to about 0.55 eV above the valance band at Vₚ = 0.5 V. The high-temperature measurement shows a very large density of interface states around the mid-gap energy, nevertheless, which hinders the Fermi level from passing through this point. The interface state contribution becomes horizontal as a consequence, and large peaks in the depletion area of the MOS capacitor become visible which resemble an inversion response. Please note that it is very unlikely that this response is caused by minority carriers in GaAs. Simulations show that such a response can only be caused by minority carriers if the midgap trapping states have capture cross sections larger than 10⁻¹⁴ cm², which are excessively large values. It is more likely that this response is indeed caused by a large midgap interface state peak. We are not able at the moment to make the distinction between the two experimentally, as this necessitates full conductance measurements on fully processed MOS field effect transistors, which we currently do not have available. This will be verified in the near future, though. Nevertheless, the fact that both n- and p-type GaAs have the surface Fermi level pinned at around midgap energies, as measured already uncountable times with all kinds of different surface configurations in the past 40 years, makes it very likely that this response is indeed caused by a large midgap interface state peak.
Figure 7. More standard $G/\omega$ vs $\omega$ plots which show a subset (selected bias voltages) of the data in the conductance map in Fig. 6g, representing the conductance data of the n-type GaAs–Al$_2$O$_3$ sample at a substrate temperature of 150°C. Variation of $G/\omega q$ as a function of measurement frequency is shown for several bias voltages.

Figure 8. GaAs–Gd$_2$O$_3$ interface state distribution derived from four measurements made on both n- and p-type substrates at both low and high substrate temperature.

Figure 9. GaAs–HfO$_2$ interface state distribution derived from low and high substrate temperature C-V measurements on a p-type GaAs sample. In this case only five frequencies were measured at high temperature, leading to only five data points toward midgap energies.

Figure 10. In$_{0.15}$Ga$_{0.85}$As–Al$_2$O$_3$ interface state distribution derived from four measurements made on both n- and p-type substrates at low and high substrate temperature.
In0.15Ga0.85As–Al2O3 MOS capacitors yield an interface state distribution which presents four large and rather localized peaks on top of a relatively flat interface state background. These peaks are one hole trap peak around the midgap energy, one electron trap peak around the midgap energy, and one electron trap peak around 0.3 eV below the conduction band energy. Whereas the midgap trapping states are likely caused by structural damage induced at the GaAs–amorphous oxide interface, in agreement with the UDM by Spicer et al.\textsuperscript{2} we speculate that the somewhat lower density trapping states close to the bandedges are caused by As or Ga dangling bonds.

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