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A Self-Aligned Process for High-Voltage, Short-Channel Vertical DMOSFETs in 4H-SiC

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Abstract—In this paper, we describe a self-aligned process to produce short-channel vertical power MOSFETs in 4H-SiC. By reducing the channel length to <0.5 μm, the specific on-resistance of the MOSFET channel is proportionally reduced, significantly enhancing performance.

Index Terms—Counter-doping, DMOS, high-voltage MOSFET, nitric oxide (NO) anneal, self-aligned, short-channel, SiC.

I. INTRODUCTION

Reducing specific on-resistance is of great importance for power MOSFETs in all SiC polytypes, but it is particularly desirable for 4H-SiC devices. 4H-SiC is the material of choice for high voltage power MOSFETs because of its high critical electric field (~2 MV/cm), wide bandgap (~3.2 eV), high bulk electron mobility (~800 cm²/Vs), and minimal mobility anisotropy. However, 4H-SiC MOSFETs fabricated to date suffer from low inversion channel mobility, typically in the range of 5–10 cm²/Vs using standard oxidation procedures [1], and 20–50 cm²/Vs with a post-oxidation anneal in nitric oxide (NO) [1], [2]. In most 4H-SiC power MOSFETs reported to date, the resistance of the inversion channel is the dominant component of the total device on-resistance.

The inversion channel resistance in MOSFETs is inversely proportional to channel mobility, but directly proportional to channel length. The channel length in SiC DMOSFETs is lithographically determined by the alignment tolerance between the base and source implant masks, and is typically in the range of 2–3 μm using conventional optical lithography. If the channel length could be reduced to the order of 0.5 μm, the channel resistance would be reduced by a factor of four to six. Moreover, this improvement would be obtained in addition to any improvements achieved by increasing the inversion channel mobility.

Fig. 1 summarizes the performance of a number of SiC power MOSFETs reported to date, along with projected performance for DMOSFETs having 3 and 0.5 μm channel lengths [3]. The specific on-resistance is the sum of resistances due to the source, channel, accumulation layer, JFET region, and drift region [4]. In these calculations, we assume an inversion channel mobility of 20 cm²/Vs, a maximum oxide field of 4 MV/cm, and a cell pitch of 11 μm (JFET region width = 6 μm).

II. DEVICE DESIGN

The calculated on-resistance is plotted at 70% of the ideal plane-junction blocking voltage, assuming that the breakdown voltage in a real device will be reduced by two-dimensional field crowding. A significant reduction in on-resistance is predicted for short-channel (0.5 μm) DMOSFETs, especially for blocking voltages in the 600–1800 V range.

In this paper, we describe a robust self-aligned process for producing short-channel DMOSFETs in 4H-SiC, and report the first short-channel (0.5 μm) 4H-SiC power DMOSFETs. These devices exhibit record low specific on-resistances for blocking voltages in the range of 900 to 1000 V.

II. DEVICE DESIGN

A schematic cross section of the self-aligned DMOSFET is shown in Fig. 2. The fabrication of SiC DMOS (double...
implanted) transistors requires a p-type base implantation and an n+ source implantation. The p-type base region usually has a retrograde profile [5], with lower doping near the surface to provide a low threshold voltage, and higher doping near the bottom junction to prevent punchthrough in the OFF-state. In the blocking mode, a punchthrough condition exists if the depletion region of the n-type drift layer reaches the n+ source, either from the side or from the bottom. To investigate punchthrough, MEDICI simulations are performed on a 20-μm-thick, 2.5 × 10^{15} cm^{-3} drift layer with channel lengths of 0.5 and 0.3 μm. We assume a retrograde p-base doping profile with 2.5 × 10^{17} cm^{-3} in the channel region and 1 × 10^{18} cm^{-3} near the bottom junction. To reduce the threshold voltage, the surface of the p-base is also assumed to be counter-doped with nitrogen at a dose between 1 × 10^{12} and 3.4 × 10^{12} cm^{-2}. Fig. 3 shows that the DMOSFET with a 0.5-μm channel length does not punch through up to 70% of the theoretical plane-junction blocking voltage (~3 kV). Fig. 4 shows that a device with a channel length as short as 0.3 μm will not punch through if the counter-doped dose is kept ≤ 1 × 10^{12} cm^{-2}. For doses ≥ 1 × 10^{12} cm^{-2}, the blocking capability can be increased with the application of a negative gate voltage (Fig. 4).

A self-aligned source technique [3], [6] is used to obtain channel lengths ≤ 0.5 μm, as described in the next section. Recent studies of 4H-SiC MOSFETs on ion-implanted p-base regions show that significant improvements to inversion channel mobility are achieved by: 1) activating the p-type implants in a silane ambient to minimize surface roughness [7]; 2) performing a post-oxidation anneal in nitric oxide (NO) to reduce interface state density in the upper half of the bandgap [8]; and 3) counter-doping the channel with nitrogen [9]. All these features are incorporated in the fabrication process. Unlike previous devices [9], we exclude the counter-doped nitrogen implant from the JFET region to avoid increasing the oxide field in the blocking state. Single-zone junction termination extension (JTE) [10] is employed for edge termination. To reduce the cell pitch, we utilize a self-aligned source/base ohmic contact process with zero spacing between n+ and p+ contacts, as illustrated in Fig. 2.

III. DEVICE FABRICATION

Two 4H-SiC wafers are processed to fabricate the self-aligned short-channel DMOS transistors. The first wafer includes a 20-μm n-type epilayer doped 3.2 × 10^{15} cm^{-3}. The second wafer includes a 6-μm n-type epilayer doped 1.9 × 10^{16} cm^{-3}. The self-aligned process begins with the growth of a 40 nm sacrificial oxide, followed by low-pressure chemical vapor deposition (LPCVD) deposition of 1.5 μm of polysilicon, which is further oxidized to produce 35 nm of sacrificial oxide. A 200-nm Ti–Ni mask is formed by liftoff lithography and used to mask the reactive ion etching (RIE) of the polysilicon layer, which subsequently serves as the p-base implant mask. Fig. 5 shows an SEM image of one of the polysilicon fingers used to mask the p-base implant. The p-base regions are formed by implanting Al with a retrograde profile [5] having a surface concentration of 5 × 10^{17} cm^{-3}. Next, a threshold adjust implant of N is performed at a dose of 3.4 × 10^{12} cm^{-2} and energy of 30 keV. By introducing the counter-doped implant at the same time as the p-well implant, we exclude the n-type dopants from

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**Fig. 3.** Simulated reverse currents for self-aligned DMOSFETs with channel lengths of 0.5 μm and four different counter-doped doses. Note that all currents in this plot are well below those which would be expected under punch-through conditions.

**Fig. 4.** Simulated reverse currents for self-aligned DMOSFETs with channel lengths of 0.3 μm and three different counter-doped doses. Solid curves are for V_G = 0 and dashed curves are for V_G = −6 V.

**Fig. 5.** SEM image of one of the polysilicon fingers after RIE. The polysilicon mask is 6 μm wide.
Fig. 6. SEM image of the oxidized polysilicon finger used as a self-aligned mask for the source implant.

Fig. 7. DMOSFET after the n+ source implant. The light feature is a Ti–Au mask to block n+ implants in areas where p+ contacts will subsequently be formed.

Fig. 8. Completed self-aligned short-channel DMOSFET.

Fig. 9. ON-state characteristics of a DMOSFET on a 20-μm epilayer with $L_f = 8 \mu m$ and an area of $1.248 \times 10^{-4}$ cm$^2$. $R_{ON,SP} = 27$ mΩ·cm$^2$.

Fig. 10. ON-state characteristics of a DMOSFET on a 20-μm epilayer with $L_f = 6 \mu m$ and an area of $1.56 \times 10^{-4}$ cm$^2$. $R_{ON,SP} = 33$ mΩ·cm$^2$.

IV. EXPERIMENTAL RESULTS

Figs. 9 and 10 show current–voltage ($I$–$V$) characteristics of two self-aligned DMOSFETs on the 20-μm epilayer, fabricated...
Fig. 11. Blocking characteristics of the $1.248 \times 10^{-4} \text{ cm}^2$ and $1.56 \times 10^{-4} \text{ cm}^2$ DMOSFETs on the 20-\(\mu\)m epilayer. Both measurements are performed with the devices immersed in Fluorinert.

Fig. 12. ON-state characteristics of a DMOSFET on a 6-\(\mu\)m epilayer with \(L_J = 4 \mu m\) and an area of \(1.04 \times 10^{-4} \text{ cm}^2\). \(R_{ON,SP} = 9.95 \text{ m}\Omega \text{ cm}^2\).

Fig. 13. ON-state characteristics of a DMOSFET on a 6-\(\mu\)m epilayer with \(L_J = 6 \mu m\) and an area of \(1.56 \times 10^{-4} \text{ cm}^2\). \(R_{ON,SP} = 16.9 \text{ m}\Omega \text{ cm}^2\).

Fig. 14. OFF-state characteristics of the DMOSFET of Fig. 13, showing blocking voltage >900 V.

Fig. 15. Specific on-resistance of DMOSFETs on a 6-\(\mu\)m epilayer as a function of JFET width.

Fig. 16 shows measured on-resistance of DMOSFETs on the 6-\(\mu\)m epilayer as a function of the gate voltage. As the gate voltage is decreased and approaches the threshold voltage, the channel resistance increases rapidly. The specific on-resistance becomes almost independent of gate voltage for \(V_G > 15\) V. Since the inversion channel resistance is inversely proportional to gate voltage minus threshold voltage, and therefore continues to decrease as gate voltage is increased, this is evidence that in the “full-on” condition the inversion channel resistance is no longer the dominant component of total device resistance. This is in marked contrast to conventional 4H-SiC DMOSFETs,
where the channel resistance typically dominates the on-resistance of the device, even at the highest allowable gate voltages. In the DMOSFETs on the 6-μm epilayer, the source resistance is found to be the dominant component of the on-resistance. The source resistance is larger than expected in these devices due to misalignments in the minimum-size abutting source/base contacts shown in Fig. 2. This effect can be eliminated by minor changes to the source/base ohmic contact layout.

V. CONCLUSION

A novel self-aligned process was developed that allowed reliable fabrication of short-channel high voltage DMOSFETs in 4H-SiC. By reducing the channel length to ≤0.5 μm, we significantly reduced the resistance of the inversion channel so that it is no longer the dominant component of the specific on-resistance of the device. Fabricated DMOSFETs show low specific-on-resistance of 9.95 mΩ·cm².

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REFERENCES


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From 1973 to 1983, he was Member of Technical Staff, Bell Laboratories, Murray Hill, NJ. While at Bell Labs, he served as principal designer of AT&T’s first microprocessor, and developed a time-of-flight technique for measuring the high-field drift velocity of electrons in inversion layers on silicon. In 1983 he became a Professor of electrical engineering at Purdue, where he was the founding Director of the Purdue Optoelectronics Research Center. He is currently the Charles William Harrison Professor of Electrical and Computer Engineering at Purdue University. He has coauthored more than 250 technical papers and conference presentations (18 invited), five book chapters, and holds 13 U.S. patents. Since joining Purdue, he has been principal investigator of over $25 million in sponsored research contracts, and he was recently named Co-Director of the Birck Nanotechnology Center, a $58 million research facility being constructed in Purdue’s Discovery Park. During the 1980s, he focused on GaAs devices, but since 1990 he has worked almost exclusively on SiC. His Purdue group is responsible for a number of advances in SiC devices, including the first SiC nonvolatile memories, the first monolithic digital integrated circuits, the first charge-coupled devices, the first DMOS power transistors, and the first SiC IMPATT microwave diodes.

Dr. Cooper served as an Associate Editor of the IEEE TRANSACTIONS ON ELECTRON DEVICES from 1983 through 1986. He was Guest Editor of the 1999 Special Issue of the IEEE TRANSACTIONS ON ELECTRON DEVICES on SiC device technology.