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Submicrometer Inversion-Type Enhancement-Mode InGaAs MOSFET With Atomic-Layer-Deposited Al₂O₃ as Gate Dielectric

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Abstract—High-performance inversion-type enhancement-mode n-channel In₀.₅₃Ga₀.₄₇As MOSFETs with atomic-layer-deposited (ALD) Al₂O₃ as gate dielectric are demonstrated. The ALD process on III–V compound semiconductors enables the formation of high-quality gate oxides and unpinning of Fermi level on compound semiconductors in general. A 0.5-μm gate-length MOSFET with an Al₂O₃ gate oxide thickness of 8 nm shows a gate leakage current less than 10⁻¹⁰ A/cm² at 3-V gate bias, a threshold voltage of 0.25 V, a maximum drain current of 367 mA/mm, and a transconductance of 130 mS/mm at drain voltage of 2 V. The midgap interface trap density of regrown Al₂O₃ on In₀.₅₃Ga₀.₄₇As is ∼1.4 × 10¹²/cm² · eV which is determined by low- and high-frequency capacitance–voltage method. The peak effective mobility is ∼1100 cm²/V · s from dc measurement, ∼2200 cm²/V · s after interface trap correction, and with about a factor of two to three higher than Si universal mobility in the range of 0.5–1.0-MV/cm effective electric field.

Index Terms—Atomic layer deposition (ALD), compound semiconductor, enhancement mode (E-mode), inversion, MOSFETs.

I. INTRODUCTION

IN THE PAST four decades, great efforts have been made to produce “perfect” insulators for III–V MOSFETs. The literature testifies to the extent of this enormous effort [1]–[6], including some promising results from in situ molecular-beam-epitaxy (MBE) grown Ga₂O₃/Gd₂O₃ [7]–[11]. However, this letter is mainly focused on ex situ atomic-layer-deposited (ALD) high-κ dielectrics on III–V [12]–[17], since the Si industry is already familiar with the ALD Hf-based dielectrics for front-end processes. The transition from ALD high-κ on Si to high-κ on III–V compound semiconductors must be easier.

Although high-performance depletion-mode GaAs MOSFETs have been previously demonstrated [10], [12]–[14], the reported inversion-type enhancement-mode (E-mode) GaAs MOSFETs suffer from low drain currents [18]–[20]. In this letter, we report high-performance inversion-type E-mode In₀.₅₃Ga₀.₄₇As MOSFETs using ALD Al₂O₃ as gate dielectric. The maximum drain current of 367 mA/mm and extrinsic transconductance of 130 mS/mm for a 0.5-μm gate-length MOSFET are achieved, which has a significant improvement over the previously reported inversion-type E-mode In₀.₂₅Ga₀.₇₅As MOSFETs [19]. Al₂O₃ has a high bandgap (∼9 eV), a high breakdown electric field (5–30 MV/cm), a high permittivity (8.6–10), and a high thermal stability (up to at least 1000 °C), and it remains amorphous under typical processing conditions. Compared to the conventional methods to form thin Al₂O₃ films, i.e., by sputtering, electron beam evaporation, chemical vapor deposition, or oxidation of pure Al films, ALD Al₂O₃ is of much higher quality. [21] The disadvantage for Al₂O₃ is its relative low-κ value compared to other high-κ materials. However, the similar ALD process of HfO₂, HfAlO, or other high-κ dielectrics could be applied to this device structure and significantly reduce the equivalent oxide thickness down to 1–2 nm.

II. DEVICE STRUCTURE AND FABRICATION

Fig. 1(a) shows the cross-sectional schematic of the device structure of an ALD Al₂O₃/In₀.₅₃Ga₀.₄₇As MOSFET. A 500-nm p-doped 4 × 10¹⁷-cm⁻³ buffer layer and a 300-nm p-doped 1 × 10¹⁷-cm⁻³ In₀.₅₃Ga₀.₄₇As channel layer were sequentially grown by MBE on a 2-in InP p+ substrate. After surface degreasing and ammonia-based native oxide etching, the wafers were transferred via room ambient to an ASM...
F-120 ALD reactor. A 30-nm thick Al2O3 layer was deposited at a substrate temperature of 300 °C as an encapsulation layer.

For device fabrication, source and drain regions were selectively implanted with a Si dose of $1 \times 10^{14}$ cm$^{-2}$ at 30 keV and $1 \times 10^{14}$ cm$^{-2}$ at 80 keV through the 30-nm-thick Al2O3 layer. Implantation activation was achieved by rapid thermal anneal (RTA) at 650 °C–850 °C for 10 s in a nitrogen ambient. An 8-nm Al2O3 film was regrown by ALD after removing the encapsulation layer by buffered-oxide-etch (BOE) solution (BOE: H2O = 1:5 for 2 min) and soaking in ammonia sulfide for 10 min for surface preparation. After 600°C PDA in N2 ambient, the source and drain ohmic contacts were made by an electron beam evaporation of a combination of AuGe/Ni/Au and a lift-off process, followed by an RTA process at 400 °C for 30 s also in a N2 ambient. The gate electrode was defined by the electron beam evaporation of Ni/Au and the lift-off process. The fabricated MOSFETs have a nominal gate length varying from 0.50 to 40 μm and a gate width of 100 μm. An HP4284 LCR meter was used for the capacitance measurement, and a Keithley 4200 was used for the MOSFET output characteristics.

III. RESULTS AND DISCUSSION

Fig. 1(b) shows the dc $I_{ds}$–$V_{ds}$ characteristics with a gate bias from 0 to 5 V in steps of +1 V. The measured MOSFET has a mask-designed gate length $L_{\text{mask}}$ of 0.50 μm and a gate width of 100 μm. $L_{\text{mask}}$ is defined by source–drain implantation mask. A maximum drain current of 367 mA/mm is obtained at a gate bias of 5 V and a drain bias of 2 V. The device performance has a significant leap in drain current, compared to our previous results on InGaAs MOSFETs [19]. We ascribe this improvement to the fact that InGaAs is the more forgiving material with respect to the Fermi-level pinning and has a narrower bandgap which makes the realization of electron inversion easier.

The gate leakage current is below $10^{-4}$ A/cm$^2$ at 3-V gate bias and around 0.3 A/cm$^2$ at 5-V gate bias, which is still more than five orders of magnitude smaller than the drain ON-current. The source–drain leakage current is another issue for narrow bandgap semiconductor devices that is caused mainly by drain-induced-barrier-lowering (DIBL) effect and impact ionization.

The source–drain leakage current at zero gate bias is $\sim$1 μA from virgin devices and increases to tens of microamperes after multiple measurements or heat cycles at $V_{ds}$ = 2 V. It is significantly reduced to less than 5 μA at $V_{ds}$ = 1 V even after stress. ON/OFF ratio of $\sim$4 × 10$^3$ is achieved at $V_{gs}$ = 5 V (ON) and $V_{gs}$ = 0 V (OFF), and $V_{ds}$ = 1.0 V on these devices.

Since the fabrication process used is not a self-aligned process, accurate determination of the effective gate length and series resistance is important in evaluating the intrinsic device performance and the potential for further optimization. The inset of Fig. 2(b) shows the effective gate length ($L_{\text{eff}}$) and the series resistance ($R_{\text{SD}}$) extracted by plotting $R_{\text{Ch}}$ versus $L_{\text{mask}}$. Here, $R_{\text{Ch}}$ is the measured channel resistance. $R_{\text{SD}}$ and $\Delta L$ are determined to be 15 Ω and $<0.05$ μm, respectively. $\Delta L$, which is the difference between $L_{\text{mask}}$ and $L_{\text{eff}}$, is negligible in this letter so that $L_{\text{mask}} \approx L_{\text{eff}} \approx L$.

The maximum extrinsic transconductance $G_m$ is $\sim$130 mS/mm, and the on-resistance is only 2 Ω · mm at $V_g$ = 5 V. The extrinsic $G_m$ could be further improved by reducing the thickness of the dielectric and improving the quality of the interface. To evaluate the output characteristics more accurately, the intrinsic transfer characteristics are calculated by subtracting the half of $R_{SD}$ and are compared with the extrinsic ones in Fig. 2(a). The resulting intrinsic maximum drain current and transconductance for 0.5-μm device are 425 mA/mm and 145 mS/mm, respectively. By the conventional linear region extrapolation method or second derivative method, the extrinsic threshold voltage is determined around 0.25 V. The subthreshold slope and the DIBL for this particular device are 260 mV/decade and 150 mV/V, respectively.

Fig. 2(b) summarizes all measured drain current $I_{ds}$ versus $1/L_{\text{mask}}$ under $V_{gs}$ = 5 V and $V_{ds}$ = 2 V or $V_{ds}$ = 1 V. The drain current or transconductance is linearly and inversely proportional to $L_{\text{mask}}$, as expected, and starts to saturate at $L_{\text{mask}} = 0.75$ μm. For a simple linear extrapolation, we expect to have the maximum drain current of 510 mA/mm for 0.25-μm device and 930 mA/mm for 0.1-μm device, not considering parasitic resistance and short-channel effect. The large subthreshold slope and $m$-factor indicates that $D_A$ of Al2O3/InGaAs is still significant compared to SiO2/Si interface. With the optimization of surface preparation and high-$n$ dielectric formation process, the drain current and the $G_m$ could increase at least a factor of two to three further [9].

Detailed capacitance–voltage (C–V) measurements of MOS capacitors, fabricated on the same device wafers, are also carried out to evaluate the interface quality of ALD Al2O3 on InGaAs, as shown in Fig. 3(a). The high-frequency (HF) C–V at 10 kHz shows a clear transition from accumulation to depletion for a typical p-type MOS capacitor. The inversion features of low-frequency (LF) C–V from 1 kHz down to 300 Hz indicate that the conventional Fermi-level pinning phenomenon on III–V is overcome in this ALD-Al2O3/InGaAs interface. We ascribe the small (3% per decade) frequency dispersion at accumulation capacitance to the relative high $D_A$ at the
valence band edge, although the extrinsic parasitic effects could also contribute to it. The midgap \( D_A \) is estimated to be around 1.4 \( \times 10^{12} \) cm\(^{-2} \) eV which is determined by the HF-LF method. Moderate hysteresis of \(~100\) mV exhibits in the \( C-V \) loops, as shown in the inset of Fig. 3(a).

Effective mobility is another important parameter to evaluate the MOSFET performance. DC “split \( C-V \)” method is used to measure the channel capacitance of a 40-\( \mu \)m-gate-length device which can be used to calculate the total inversion charge in the channel by integrating the \( C-V \) curve. The effective mobility \( \mu_{\text{eff}} \) has a peak value of 1100 cm\(^2\) V\(^{-1}\)s\(^{-1}\) around a normal electric field \( E_{\text{eff}} \) of 0.25 MV/cm and twice higher \( \mu_{\text{eff}} \) than the Si universal mobility [22] at \( E_{\text{eff}} \) of 0.50 MV/cm, as shown in Fig. 3(b). It is slightly higher than the mobility value from strain silicon. The peak \( \mu_{\text{eff}} \) increases to 2200 cm\(^2\) V\(^{-1}\)s\(^{-1}\) after the correction of overestimated inversion charge by the dc split \( C-V \) due to the interface traps [24]. More sophisticated measurement by pulse \( I-V \) and pulse \( C-V \) is ongoing. A better mobility performance is expected to be achievable by further optimizing the dielectric formation and the device fabrication process.

IV. CONCLUSION

In summary, we have demonstrated the high-performance inversion-type E-mode \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) MOSFETs using ALD high-\( k \) gate dielectrics. These results suggest that \( \text{In}_{0.53}\text{Ga}_{0.47}\text{As} \) could be an ideal channel material, which has higher electron effective mobility, low surface recombination velocity to have enough inversion charge, and wide enough bandgap for ultimate CMOS applications with low drain voltage.

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