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Accumulation Gate Capacitance of MOS Devices With Ultrathin High- κ Gate Dielectrics: Modeling and Characterization

Ahmad Ehteshamul Islam and Anisul Haque, *Member, IEEE*

Abstract—A quantum–mechanical (QM) model is presented for accumulation gate capacitance of MOS structures with high- κ gate dielectrics. The model incorporates effects due to penetration of wave functions of accumulation carriers into the gate dielectric. Excellent agreement is obtained between simulation and experimental C – V data. It is found that the slope of the C – V curves in weak and moderate accumulation as well as gate capacitance in strong accumulation varies from one dielectric material to another. Inclusion of penetration effect is essential to accurately describe this behavior. The physically based calculation shows that the relationship between the accumulation semiconductor capacitance and Si surface potential may be approximated by a linear function in moderate accumulation. Using this relationship, a simple technique to extract dielectric capacitance for high- κ gate dielectrics is proposed. The accuracy of the technique is verified by successfully applying the method to a number of different simulated and experimental C – V characteristics. The proposed technique is also compared with another method available in the literature. The improvements made in the proposed technique by properly incorporating QM and other physical effects are clearly demonstrated.

Index Terms—High- κ dielectric, MOS capacitors, parameter extraction, quantum–mechanical (QM) modeling.

I. INTRODUCTION

THE CONTINUOUS scaling of MOSFETs, as outlined in the International Technology Roadmap for Semiconductors (ITRS) [1], requires that SiO₂ should be replaced by high- κ dielectric materials as gate insulators to avoid excessive direct tunneling gate current and reliability problems. Significant advances have been made in recent years in realizing MOS devices with good quality high- κ gate dielectric materials. A review of this topic may be found in [2].

Modeling and characterization of MOSFETs with ultrathin high- κ gate dielectrics are nontrivial because of the variation of the potential barrier height ϕ_b at the dielectric–Si interface and the dielectric constant ϵ_{di} from one dielectric to

another. Higher density of interface traps further complicates the problem. Gate capacitance C_g of these devices is influenced by quantum–mechanical (QM) effects under large gate bias voltage for both accumulation and inversion conditions. Wave function penetration into the gate dielectric causes a shift in the semiconductor charge centroid resulting in an increase in calculated C_g . A number of studies have investigated penetration effect in MOS structures with SiO₂ gate dielectric [3]–[8]. On the other hand, few works have been done to study penetration effect in devices with high- κ gate dielectrics, although this effect is expected to be more severe in such devices due to lower values of ϕ_b . Hakim and Haque have calculated C_g of MOSFETs with high- κ gate dielectric layers in inversion condition [9]. It is shown that for the same equivalent oxide thickness (EOT), C_g varies significantly with gate dielectric materials due to variations in ϕ_b and ϵ_{di} . Here, EOT is defined as the scaled (to SiO₂) physical width of the high- κ dielectric layer, i.e., $EOT = \epsilon_{SiO_2} T_{di} / \epsilon_{di}$, where T_{di} is the thickness of dielectric layer.

Gate capacitance of MOSFETs under accumulation condition is important from characterization point of view. Suñé *et al.* [7] have proposed a QM accumulation region model of MOS transistors with SiO₂ gate dielectric using a quantum box, considering the contribution from both bound and extended states and taking into account the effect of wave function penetration. The effectiveness of the model to simulate devices with high- κ gate dielectrics has not been investigated. Chim *et al.* [8] have proposed a model to calculate accumulation gate capacitance for SiO₂ considering penetration effect. However, they have approximated the potential profile by an exponential function and have neglected the extended states. Such assumptions are known to be not always justified [7], [10]. As such, this model is not expected to match experimental data accurately, especially for devices with high- κ gate dielectrics.

It is well known [11], [12] that existing semiclassical methods to extract oxide (dielectric) capacitance from experimental C – V data (for example, [13], [14]) do not work well for devices with ultrathin high- κ gate dielectrics, or even for ultrathin SiO₂ layer. It is therefore not uncommon to extract T_{di} or the dielectric capacitance C_{di} by matching simulated C – V with measured data using T_{di} as a fitting parameter [15], [16]. This method is prone to error due to the simplifying assumptions invoked in the simulator (such as lack of self-consistency, consideration of a small number of eigenstates, neglecting wave function penetration, etc.). Inasmuch as accurate simulators

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are usually computationally intensive and determination of C_{di} involves several runs, such approaches need significant computational time. In addition, the number of fitting parameters increases when this technique is applied to high- κ materials. Kar has recently proposed a technique to extract C_{di} and some other parameters from measured accumulation $C-V$ for MOS capacitance of ultrathin high- κ gate dielectric [11], [12]. This method is simple, easy to use, and does not need any simulation. The central assumption of this method, that the accumulation semiconductor capacitance C_{acc} is an exponential function of Si surface potential ϕ_s , was used without providing any justification. For this reason, the accuracy of this method could not be verified.

In this paper, we present a model for accumulation gate capacitance of MOS structures with ultrathin high- κ gate dielectrics. The model is based on the self-consistent solution of one-dimensional (1-D) Schrödinger's and Poisson's equations including wave function penetration. The accuracy of the proposed model is verified by comparing its results to those of another $C-V$ simulator and with published experimental data. The model is used to obtain a physically based relationship between C_{acc} and ϕ_s . Based on this relationship, we propose a simple technique to characterize C_{di} from measured $C-V$ data. The validity of this technique is confirmed from simulated results and by applying the technique successfully to different published experimental $C-V$ curves.

II. MODELING

A. Theory

Our model presented in this section is valid for both n- and p-type substrates using any dielectric stack with metal or poly-Si gate. Electronic states of a MOS accumulation layer is calculated via self-consistent solution of coupled 1-D Schrödinger's and Poisson's equations within the effective mass approximation. In principle, valence band structures are nonparabolic, and one should use multiband Schrödinger's equation to determine hole states. However, such a scheme within the self-consistent loop is computationally prohibitive. On the other hand, it has been shown that the calculated $C-V$, even for holes, is not sensitive to the complicated valence band structure, and the simple single-band equation with bulk values of the effective masses accurately describes the capacitance [6].

1-D Schrödinger's equation is solved using a technique based on the Green's function formalism with transmission line analogy [3]. The carrier density in bound states N_{ij} , associated with the j th subband in the i th valley, is calculated using the procedure of Haque and Kauser [6]. Our model is capable of considering any value or energy (or bias) dependent function for carrier effective mass within the dielectric region m_{di} . Carriers in the three-dimensional (3-D) extended states are taken into account semiclassically using Fermi-Dirac statistics and parabolic density-of-states [17]. The total charge density at any position z (z is normal to the Si-dielectric interface) for a pMOS is expressed as

$$\rho(z) = eN_D^+(z) - eN_{acc} \quad (1)$$

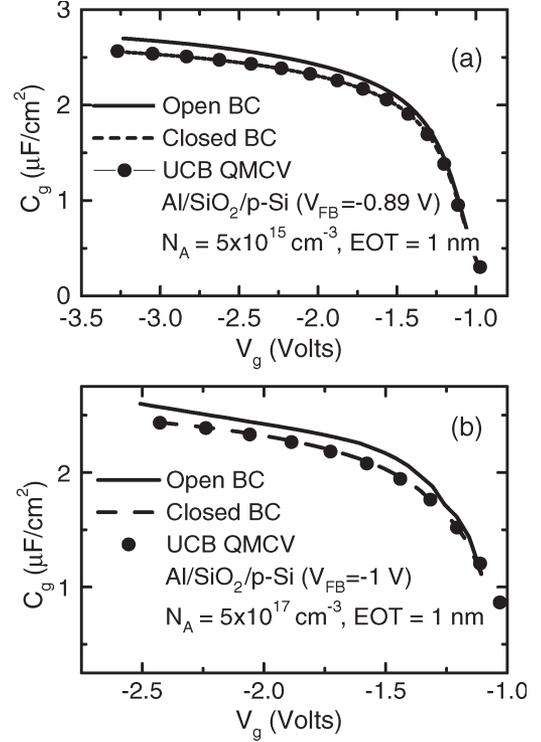


Fig. 1. C_g versus V_g curve for an Al/SiO₂/p-Si MOS structure with two different doping densities operating in accumulation region, with and without considering wave function penetration effect. Results of UCB QMCV are also provided for comparison.

and

$$N_{acc} = \sum_i \sum_j N_{ij} |\psi_{ij}(z)|^2 + N_{cl}(z) \quad (2)$$

where $N_D^+(z)$ is the distribution of ionized donors, $\psi_{ij}(z)$ is the electron wave function, and $N_{cl}(z)$ is the semiclassical distribution of carriers in the extended states. $\rho(z)$ is used to solve the Poisson's equation in the combined oxide-semiconductor regions using finite-difference method with nonuniform mesh size. Nonuniformity of mesh size has been incorporated in the model exactly without using any approximation. Once the self-consistent loop converges, C_{acc} and C_g are calculated from the basic definitions $C_{acc} = e\partial N_{acc}/\partial\phi_s$ and $C_g = e\partial N_{acc}/\partial V_g$.

B. Results

The results of our self-consistent calculations are presented here. All calculations are performed at room temperature. It has been shown that C_g is only weakly dependent on m_{di} under inversion bias [9]. Our numerical calculation has shown that under accumulation bias, C_g is even less sensitive to m_{di} . Therefore, we have used a constant value of $m_{di} = 0.5m_0$ in our numerical calculations. This eliminates m_{di} as a fitting parameter without sacrificing accuracy. Fig. 1 shows calculated C_g as a function of gate voltage V_g for the following MOS structure: Al/SiO₂/p-Si with $T_{di} = 1$ nm. In Fig. 1(a), acceptor doping density $N_A = 5 \times 10^{15} \text{ cm}^{-3}$, and in Fig. 1(b), $N_A = 5 \times 10^{17} \text{ cm}^{-3}$. Work function for Al is considered to be 4.1 eV,

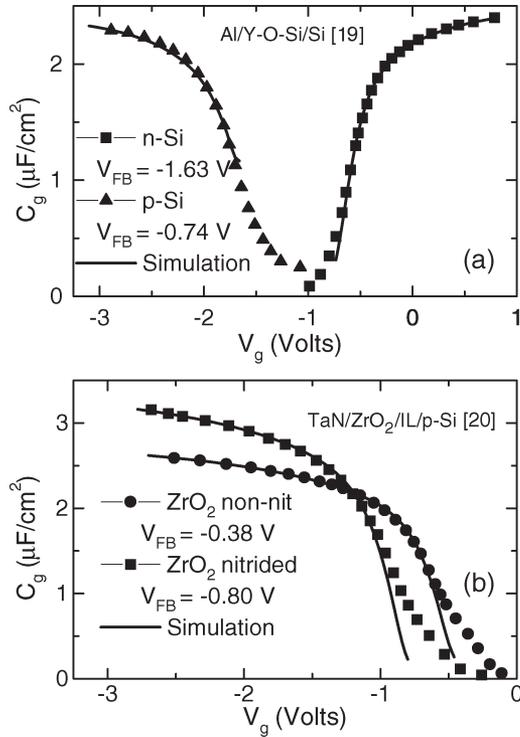


Fig. 2. Simulated C_g versus V_g curves for four different MOS structures along with experimental data. (a) “Triangles” represent Al/Y–O–Si/p–Si device and “squares” represent Al/Y–O–Si/n–Si device [19]. (b) “Squares” represent TaN/(nitrided)ZrO₂/IL/p–Si device and “circles” represent TaN/(nonnitrided)ZrO₂/IL/p–Si device [20].

whereas ϕ_b is taken as 4.58 eV for holes. Results calculated using open boundary condition (BC), including wave function penetration, as well as closed BC, neglecting wave function penetration, are presented. For the sake of comparison, we also include the results of a popular QM C – V simulator (QMCV from the University of California, Berkeley (UCB) [18]) that neglects wave function penetration. It is observed that our results for both doping densities, calculated using closed BC, are identical to that of QMCV, and, as expected, C_g is higher when open BC is used.

Next, we compare our calculated C – V with published experimental data in Fig. 2. Four different MOS structures are chosen from [19] and [20]. The structures used in our simulation are described in Table I. For all the devices, thickness values are taken from the TEM images provided in the references. In case of Fig. 2(a), the values of ϵ_{di} used are the same as suggested in [19], but for devices of Fig. 2(b), ϵ_{di} of ZrO₂ is chosen the same as the value reported in [2] instead of that in [20]. QM effects have not been considered in [20] in extracting ϵ_{di} , which may have resulted in an underestimation of ϵ_{di} . For the same reason, we also choose a somewhat higher value of ϵ_{di} for the interfacial layers (IL) than that reported in [20]. The value of ϕ_b in Fig. 2(b) is unknown as it represents the barrier height at the IL–Si interface. Therefore, to simulate these devices, we have treated ϕ_b as a fitting parameter. It may be mentioned that any error in T_{di} value obtained from TEM image may lead to an altered value of ϵ_{di} . The fitted value of ϕ_b should be independent of this error as the slope of the C – V curve is much more sensitive to ϕ_b than to T_{di}/ϵ_{di} . Results for the best matched

TABLE I
PARAMETERS USED IN THE CALCULATIONS OF FIG. 2

MOS Structures [Reference]	Dielectric material properties	$N_{A(D)}$ (cm ⁻³)	ϕ_b (eV)
Al/Y–O–Si/n–Si [19]	$\epsilon_{di} = 14$ $T_{di} = 4.2$ nm	5×10^{15}	2
Al/Y–O–Si/p–Si [19]	$\epsilon_{di} = 14.2$ $T_{di} = 4.2$ nm	1×10^{17}	4.5
TaN/(non-nitrided)ZrO ₂ /IL/p–Si [20]	ZrO ₂ : $\epsilon_{di} = 25$ $T_{di} = 3.5$ nm IL: $\epsilon_{di} = 5.6$ $T_{di} = 0.8$ nm	2.1×10^{15}	2
TaN/(nitrided)ZrO ₂ /IL/p–Si [20]	ZrO ₂ : $\epsilon_{di} = 25$ $T_{di} = 3.3$ nm IL: $\epsilon_{di} = 13$ $T_{di} = 1.2$ nm	2.1×10^{15}	1.8

conditions are shown in Fig. 2. Excellent agreement between model and measurement has been achieved for both nMOS and pMOS devices, except for low accumulation bias. The mismatch for low accumulation bias may be attributed to the presence of interface traps. It should be pointed out that the ϕ_b values that we have chosen for the two IL (nitrided and nonnitrided) in Fig. 2(b) are lower than the known values of ϕ_b for ZrO₂ [2]. An important observation in Fig. 2 is that the slopes of the C – V curves in strong accumulation are different for different high- κ dielectric materials. As will be seen in the next section, this slope plays a critical role in extracting C_{di} . We have verified that the difference in the slope is caused by, in addition to different EOT, different values of ϕ_b for different dielectric materials. Inasmuch as QM modeling with closed BC inherently assumes that $\phi_b \rightarrow \infty$, such models cannot incorporate any effect of variation of ϕ_b . It is therefore essential to consider wave function penetration through using open BC for accurately simulating accumulation gate capacitance of MOS structures with different high- κ dielectric materials.

To investigate the effect of ϕ_b on C_g further, we consider three hypothetical MOS structures with Ta₂O₅ ($\phi_b = 1.88$ eV, $\epsilon_{di} = 26$), HfO₂ ($\phi_b = 3.08$ eV, $\epsilon_{di} = 25$), and SiO₂ ($\phi_b = 4.58$ eV, $\epsilon_{di} = 3.9$) gate dielectrics, respectively. The dielectric properties of these devices are taken from [2]. All three devices have EOT = 1 nm. If modeled using closed BC, all three devices would be represented by identical C – V curves. However, Fig. 3 shows that C_g is different for all three devices. Not only the value of C_g increases in strong accumulation with decreasing ϕ_b but also the slope of C – V curve increases in weak and moderate accumulation with decreasing ϕ_b . The dependence of the C – V curve on ϕ_b can be best explained in terms of C_{acc} versus ϕ_s curve. Fig. 4 shows the calculated C_{acc} versus ϕ_s curves for the nitrided ZrO₂ device studied in Fig. 2(b). Results obtained from three different models, namely,

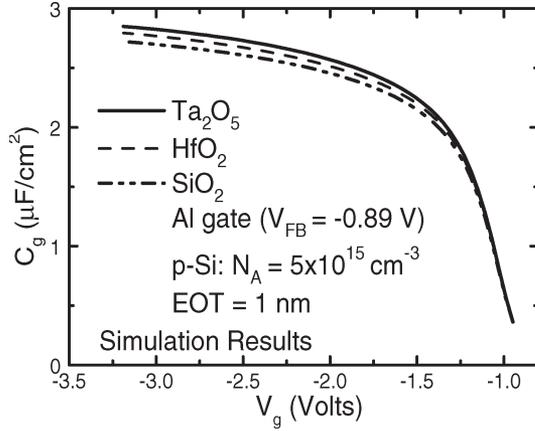


Fig. 3. Effect of ϕ_b on C_g - V_g characteristics for three different nMOS structures as described in the text.

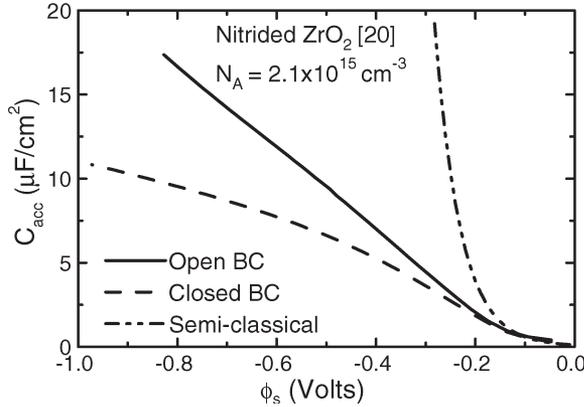


Fig. 4. C_{acc} versus ϕ_s calculated for nitrided ZrO_2 dielectric (EOT = 1 nm) using three different models.

QM with open BC, QM with closed BC, and semiclassical (charge sheet model), are presented. Significant differences among the three calculations are observed. The semiclassical C_{acc} shows an exponential dependence on ϕ_s . This is a consequence of neglecting the nonzero value of the accumulation charge centroid due to quantization. Quantization makes the QM C_{acc} much smaller. As the accumulation charge centroid shifts toward the Si-dielectric interface in the presence of wave function penetration, QM calculation with open BC results in a higher C_{acc} than that calculated with closed BC. Fig. 5 shows C_{acc} versus ϕ_s for the three devices considered in Fig. 3, calculated with QM model using open BC. The properties of these curves will be discussed in detail in the next section. Here, we observe that for a given ϕ_s in moderate and strong accumulation, the value of C_{acc} , as well as the slope of C_{acc} versus ϕ_s curve, increases with decreasing ϕ_b . This is due to the fact that a lower ϕ_b allows greater penetration of the wave function into the gate dielectric, thus reducing the value of the accumulation charge centroid in Si. As C_g is the series combination of C_{acc} and C_{di} , an increase in the value of C_{acc} and slope of C_{acc} versus ϕ_s curve also increases the value of C_g and slope of C - V curve. We have also considered C_{acc} versus ϕ_s curves for different dielectric materials with different doping densities between 10^{15} and 10^{18} cm^{-3} . The trend has always been found the same.

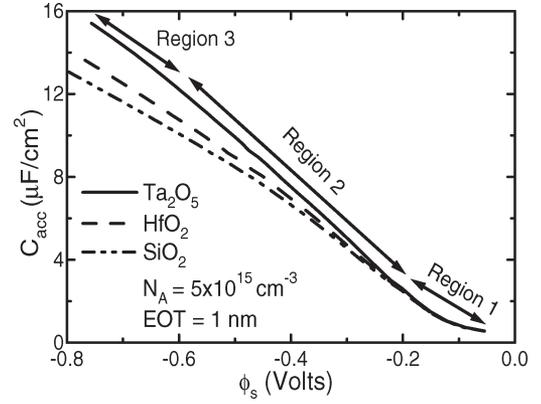


Fig. 5. C_{acc} versus ϕ_s for the three devices considered in Fig. 3. The three accumulation regions are also indicated.

III. CHARACTERIZATION OF C_{di}

A. Theory

As mentioned in Section I, several techniques are available to extract C_{di} of MOS structures. The semiclassical techniques [13], [14] are not applicable to devices in which strong QM effects are present. The limitations of the curve fitting method have also been discussed in Section I. The method proposed by Kar [11], [12] is similar to the semiclassical techniques in terms of its simplicity, and it claims to include QM effects and the effects of interface traps. However, no justification was provided for its central assumption that both C_{acc} and interface trap capacitance C_{it} are exponential functions of ϕ_s in strong accumulation with the same exponent. Our calculations in Figs. 4 and 5 reveal that the exponential assumption of Kar [11], [12] implies neglecting QM effects. In a QM model, C_{acc} exponentially depends on ϕ_s only in weak accumulation. As accumulation becomes stronger, C_{acc} first becomes linear, and then, it turns sublinear. Physical origin of such dependence of C_{acc} on ϕ_s will be discussed elsewhere. As Kar's semiclassical exponential approximation greatly overestimates C_{acc} (as observed in Fig. 4), it is suspected that this model would underestimate C_{di} when extracted from experimental C - V characteristics.

We identify three separate regions in C_{acc} versus ϕ_s curve shown in Fig. 5 over the entire accumulation bias. These are weak accumulation (region 1), moderate accumulation (region 2), and strong accumulation (region 3). Region 1 is the region in which QM effect is negligible and C_{acc} versus ϕ_s curve follows the semiclassical exponential relationship. In region 2, C_{acc} deviates from exponential nature and becomes approximately linear. To introduce a unique definition of region 3 (strong accumulation), we state that region 3 begins when N_{acc} becomes greater than 1.5×10^{13} cm^{-3} . The value of ϕ_s or (V_g) at which C_{acc} deviates from linearity depends strongly on ϕ_b and doping density. For lower value of ϕ_b (Ta_2O_5 , for example), C_{acc} may continue to be linear even deep in strong accumulation. On the other hand, for higher value of ϕ_b (SiO_2 , for example), sublinearity may onset for a N_{acc} much lower than 1.5×10^{13} cm^{-3} . Table II lists the values of ϕ_s and V_g (relative to the flatband voltage V_{FB}) at the transitions between regions 1 and 2 and regions 2 and 3.

TABLE II
 ϕ_s AND V_g VALUES AT THE TRANSITIONS BETWEEN DIFFERENT REGIONS
 IN ACCUMULATION FOR A NUMBER OF SIMULATED
 C_{acc} VERSUS ϕ_s CHARACTERISTICS

Nominal EOT (nm)	N_A (cm^{-3})	Dielectric	ϕ_s (V)		$V_g - V_{FB}$ (V)		N_{acc} (10^{13} cm^{-3})	
			1-2	2-3	1-2	2-3	1-2	2-3
1.0	5×10^{15}	Ta ₂ O ₅	-0.19	-0.53	-0.25	-1.23	0.18	1.5
	5×10^{15}	HfO ₂	-0.19	-0.55	-0.25	-1.24	0.16	1.5
	5×10^{15}	SiO ₂	-0.19	-0.56	-0.25	-1.27	0.13	1.5
0.5	5×10^{15}	Ta ₂ O ₅	-0.20	-0.53	-0.25	-0.88	0.15	1.5
	5×10^{15}	HfO ₂	-0.21	-0.55	-0.25	-0.90	0.15	1.5
	5×10^{15}	SiO ₂	-0.20	-0.53	-0.25	-1.05	0.13	1.5
0.5	5×10^{17}	Ta ₂ O ₅	-0.30	-0.41	-0.50	-0.76	0.86	1.5
	5×10^{17}	HfO ₂	-0.30	-0.43	-0.50	-0.78	0.83	1.5
	5×10^{17}	SiO ₂	-0.30	-0.44	-0.50	-0.80	0.81	1.5

The same three dielectrics as studied in Fig. 5 are chosen, and two different doping densities with two different EOT are considered. Al is the gate metal in these calculations. It is found that the transition from one region to another depends primarily on doping density. As doping density increases, moderate accumulation region becomes narrower. However, at both doping densities, for both the high- κ dielectrics considered here, C_{acc} is approximately linear for a significant portion of the strong accumulation region as well. Table III lists the values of ϕ_s and $V_g - V_{FB}$ at the transitions for the four experimental $C-V$ data presented in Fig. 2.

C_{acc} versus ϕ_s for all three regions can be accurately fitted by a complicated Boltzmann-type curve. Inasmuch as regions 2 and 3 are mostly important for parameter extraction, these two regions may be represented by the following equation:

$$C_{acc} = a_1 - a_2 \exp(-a_3 \phi_s) - a_4 \exp(-a_5 \phi_s). \quad (3)$$

Even (3) contains too many parameters for efficient and accurate extraction of C_{di} . To bypass this problem, we exploit the fact that C_{acc} versus ϕ_s is approximately linear in region 2 (sometimes also in some portion of region 3). Thus, for these regions, for both nMOS and pMOS devices, we write

$$C_{acc} = a_{acc} + b_{acc} \phi_s. \quad (4)$$

We have shown in Fig. 2 that our model, which does not consider interface traps, agrees well with experimental data in moderate and strong accumulation. The mismatch at low bias has been attributed to the presence of interface traps (D_{it}). We therefore assume that the effect of D_{it} is negligible in moderate and strong accumulation regions. This assumption is consistent

TABLE III
 ϕ_s AND V_g VALUES AT THE TRANSITIONS BETWEEN DIFFERENT REGIONS
 IN ACCUMULATION FOR THE FOUR EXPERIMENTAL $C-V$
 CHARACTERISTICS SHOWN IN FIG. 2

Material	Reference	V_{FB} (V)	ϕ_s (V)		$V_g - V_{FB}$ (V)		N_{acc} (10^{13} cm^{-3})	
			1-2	2-3	1-2	2-3	1-2	2-3
ZrO ₂ (non-nitrided)	[19]	-0.38	-0.25	-0.56	-0.75	-1.69	0.24	1.5
ZrO ₂ (nitrided)	[19]	-0.80	-0.19	-0.49	-1.09	-1.89	0.25	1.5
Y-O-Si (p-Si)	[20]	-1.63	-0.15	-0.39	-1.91	-2.87	0.23	1.5
Y-O-Si (n-Si)	[20]	-0.74	0.18	0.43	-0.46	0.53	0.18	1.5

with experimental observations for SiO₂ and should also be valid for high- κ dielectrics unless D_{it} is high in the energy range deep inside the conduction and the valence bands. The justification of this assumption from experimental data will be given in the next section. A consequence of this assumption is that C_{it} should be negligible in moderate and strong accumulation regions. The total parallel capacitance $C_p = C_{acc} + C_{it}$ in moderate and strong accumulation is then approximately equal to C_{acc} . Differentiating C_p with respect to V_g and using

$$\frac{d\phi_s}{dV_g} = 1 - \frac{C_g}{C_{di}} \quad (5)$$

we have

$$\frac{dC_p}{dV_g} = b_{acc} \left(1 - \frac{C_g}{C_{di}} \right). \quad (6)$$

Equation (5) may be derived from the definitions of C_g and C_{acc} given in Section II-A. Noting that C_g is equal to the series combination of C_{di} and C_p , we differentiate C_g with respect to V_g to obtain

$$\left| \frac{dC_g}{dV_g} \right|^{1/3} = |b_{acc}|^{1/3} \left(1 - \frac{C_g}{C_{di}} \right). \quad (7)$$

According to (7), a plot of $|dC_g/dV_g|^{1/3}$ versus C_g in accumulation region 2 (and sometimes also in some portion of region 3) should give a straight line, whose intercept with the C_g axis would yield C_{di} . b_{acc} , the slope of the C_p versus ϕ_s curve in the linear region, depends on ϕ_b , among other parameters. If the values of the other parameters are known, in principle, information on ϕ_b can be obtained from extracted b_{acc} . Work in this direction is underway.

In MOS structures with very thin gate dielectrics, gate leakage current due to direct tunneling and other transport processes distorts $C-V$ characteristics for high gate voltage. Our C_{di}

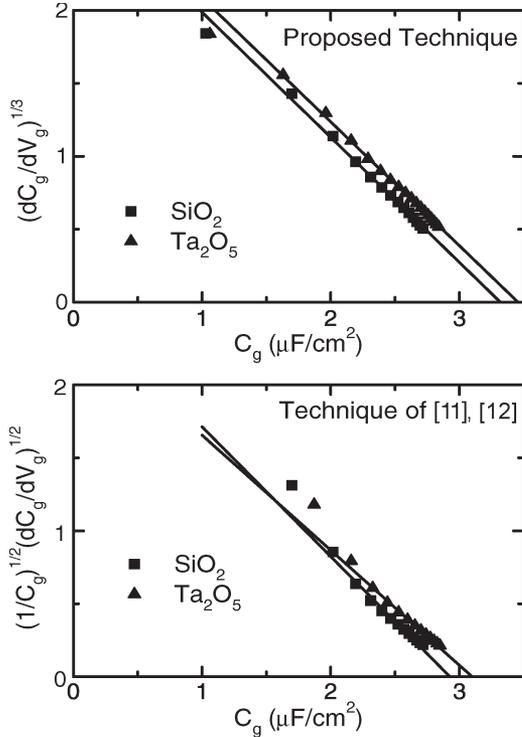


Fig. 6. Extraction of C_{di} using our proposed technique and the technique of Kar [11], [12] from simulated $C-V$ with Ta_2O_5 and SiO_2 as gate dielectric having nominal EOT = 1 nm.

extraction technique does not take into account this effect. There exists a number of techniques ([21]–[23], for example) to correct for the observed degradation. Our method should be applicable to the corrected $C-V$ curves. The direct tunneling current is smaller in MOS structures with high- κ dielectrics for a given EOT owing to a higher physical thickness of the dielectric layer. Moreover, our extraction technique is applicable in moderate accumulation where the gate voltage is smaller. These two factors should make the proposed extraction technique less susceptible due to gate leakage current. Therefore, the technique should remain valid as long as the gate leakage current is not excessive.

B. Results

We first apply our technique to the simulated devices that we have considered in Fig. 3. EOT of these devices is equal to 1 nm, leading to a $C_{di} = 3.45 \mu F/cm^2$. No interface trap states are considered. The technique of Kar [11], [12] is also applied to these devices for comparison. The extraction curves for the two techniques are shown in Fig. 6, and the extracted C_{di} values are tabulated in Table IV. We observe that the extracted C_{di} using our technique is nearly the same as the nominal C_{di} for the entire range of ϕ_b considered. On the other hand, the minimum error in Kar's technique is more than 10%, and the error increases sharply with increasing ϕ_b . Because Kar's exponential approximation has a semiclassical origin, it neglects QM effects. Consequently, C_{di} is consistently underestimated, and EOT is overestimated as observed in Table IV. Another observation worth noting in Fig. 6 and Table IV is

TABLE IV
EXTRACTED VALUES OF C_{di} AND EOT USING OUR PROPOSED TECHNIQUE, AS WELL AS THE TECHNIQUE OF KAR [11], [12], FOR THE SIMULATED DEVICES AS DISCUSSED IN THE TEXT

Dielectric material	Proposed Technique		Technique of [11], [12]	
	C_{di} ($\mu F/cm^2$)	EOT (nm)	C_{di} ($\mu F/cm^2$)	EOT (nm)
Ta_2O_5	3.45	1.00	3.10	1.11
HfO_2	3.43	1.01	3.02	1.14
SiO_2	3.32	1.04	2.93	1.18

TABLE V
COMPARISON OF NOMINAL AND EXTRACTED EOT FOR A NUMBER OF SIMULATED $C-V$ CHARACTERISTICS WITH Ta_2O_5 GATE DIELECTRIC

Doping density N_A (cm^{-3})	Nominal EOT (nm)	Extracted EOT (nm)	Extracted C_{di} ($\mu F cm^{-2}$)	ΔEOT (nm)
5×10^{15}	1	1.0142	3.4048	0.0142
	0.75	0.7580	4.5558	0.0080
	0.5	0.5056	6.8296	0.0056
5×10^{17}	1	1.0159	3.3990	0.0159
	0.75	0.7534	4.5833	0.0034
	0.5	0.5089	6.7853	0.0089

that the accuracy of our proposed technique suffers slightly with increasing ϕ_b . This may be attributed to the fact that for higher ϕ_b , the linear region in C_{acc} versus ϕ_s curve is shorter, which makes accurate extraction of C_{di} somewhat difficult. However, as the error is small even for SiO_2 , and because high- κ dielectric materials are usually characterized by lower values of ϕ_b , this limitation of our extraction technique does not pose any serious problem.

Next, we determine the error ΔEOT [$\Delta EOT = EOT(\text{nominal}) - EOT(\text{extracted})$] in extracting EOT using the proposed method from a number of simulated $C-V$ curves for Ta_2O_5 gate dielectric with Al gate electrode. We have considered two different doping densities and three different nominal EOT. Table V gives the error made in extracting EOT. ΔEOT is found to be insignificant for each data. Even higher doping density, which increases the gate voltage at the onset of linearity, does not make accurate extraction of EOT difficult.

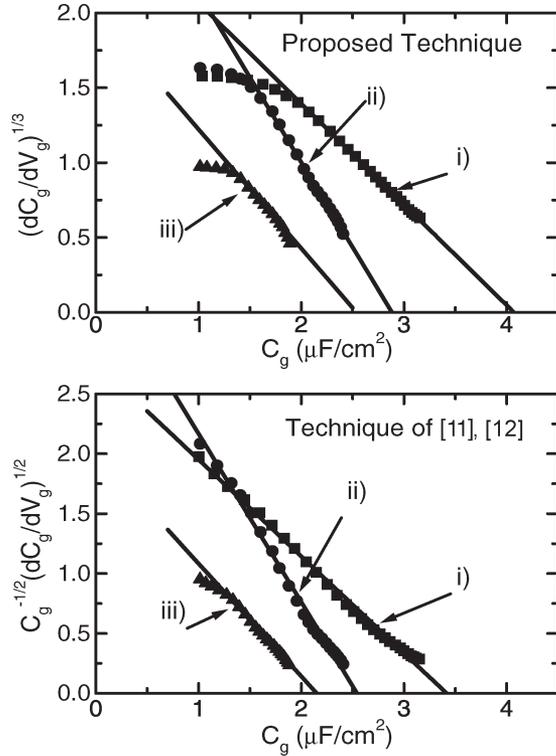


Fig. 7. Extraction of C_{di} from experimental data using our proposed technique and the technique of Kar [11], [12]. Here, i) TaN/(nitrided)ZrO₂/IL/p-Si [20], ii) Al/Y-O-Si/n-Si [19], and iii) Au/Hf₆Si₂₉O₆₅/n⁺-Si [24].

Our proposed technique is also applied to a number of experimental 1-MHz $C-V$ data obtained from [19], [20], and [24]. Extracted C_{di} values are also compared with the values extracted by Kar's technique. The extraction curves are shown in Fig. 7 for three MOS structures, and results for eight different MOS structures are summarized in Table VI. Our extraction equation is found to yield straight lines in the mentioned accumulation regions, as predicted, for each of the eight dielectrics. The experimental results also verify that Kar [11], [12] consistently underestimates C_{di} .

Comparing our extracted EOT to that of [19], where a QM model without considering wave function penetration effect is used for EOT determination, it can be seen that our extracted EOT is nearly the same as the value extracted in [19] for n-Si substrate, but higher for p-Si substrate. Inasmuch as wave function penetration effect is more severe for holes compared with electrons [6], neglect of such penetration would have more effect on EOT extraction for p-Si, thus underestimating EOT for p-Si in [19]. This agreement between our extracted EOT and that in [19] validates the accuracy of our proposed technique.

We also compare our extraction technique with another QM technique that includes wave function penetration effect [25]. The compact QM $C-V$ simulator of [25] has been developed considering wave function penetration into only the SiO₂ gate dielectric. Two sets of experimental data, one for SiO₂ gate dielectric [26] and one for HfO₂ gate dielectric [27], are considered. EOT extracted in [25], using the curve fitting approach, is 2.76 nm for SiO₂ and 1.29 nm for HfO₂. We have extracted the EOT to be 2.74 nm for SiO₂ and 1.36 nm for HfO₂. The agreement is excellent for SiO₂ and reasonably good for

TABLE VI
EXTRACTED VALUES OF C_{di} AND EOT USING OUR PROPOSED TECHNIQUE, AS WELL AS THE TECHNIQUE OF KAR [11], [12], FOR A NUMBER OF EXPERIMENTAL $C-V$ DATA

MOS Structure [Reference]	Proposed Technique		Technique of [11], [12]	
	C_{di} ($\mu\text{F}/\text{cm}^2$)	EOT (nm)	C_{di} ($\mu\text{F}/\text{cm}^2$)	EOT (nm)
Al/Y-O-Si: 42Å/n-Si [19]	2.88	1.20	2.54	1.36
Al/Y-O-Si: 42Å/p-Si [19]	2.84	1.22	2.49	1.39
TaN/(non-nitrided) ZrO ₂ /IL/p-Si [20]	3.19	1.08	2.72	1.27
TaN/(nitrided) ZrO ₂ /IL/p-Si [20]	4.07	0.85	3.42	1.01
Au/Hf ₆ Si ₂₉ O ₆₅ : 50Å/n ⁺ Si [24]	2.54	1.36	2.15	1.61
Au/Zr ₄ Si ₃₁ O ₆₅ : 50Å/n ⁺ Si [24]	1.88	1.84	1.74	1.98
Au/Hf ₅ Si ₃₁ O ₆₄ : 65Å/p ⁺ Si [24]	1.84	1.88	1.69	2.04
Au/Hf ₇ Si ₂₉ O ₆₄ : 60Å/n ⁺ Si [24]	1.15	3.00	1.05	3.29

HfO₂. That the compact model [25] does not consider increased wave function penetration in HfO₂ relative to that in SiO₂ is reflected in the underestimation of EOT for HfO₂ in [25]. This comparison, on one hand, further establishes the validity of our extraction technique and, on the other hand, demonstrates the need for including wave function penetration effect in an accurate manner.

Once C_{di} is known for an experimental $C-V$ curve, C_p versus ϕ_s characteristics may be extracted in a straightforward way. For a given point on the $C-V$ curve, C_p is determined from the fact that C_g is equal to the series combination of C_p and C_{di} . Corresponding ϕ_s is determined using (8).

$$\phi_s = \int_{V_{FB}}^V (1 - C_g(V')/C_{di}) dV'. \quad (8)$$

Extracted $C_p-\phi_s$ characteristics from all four experimental $C-V$ data of Fig. 2 are presented in Fig. 8. Extraction has been done with C_{di} values determined using both the proposed

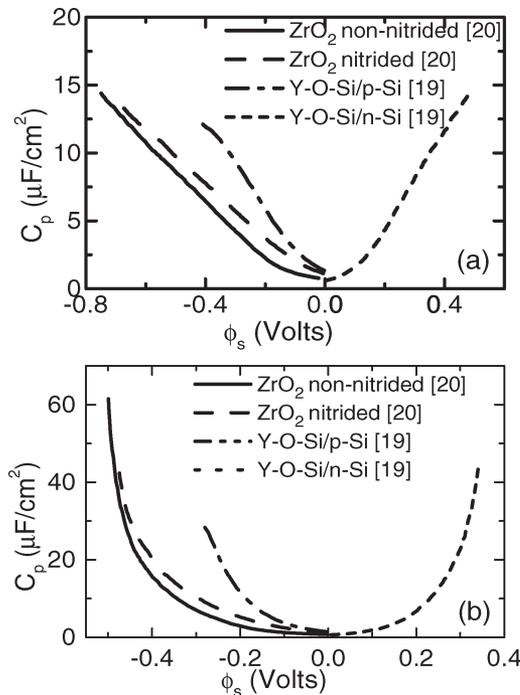


Fig. 8. Extracted C_p versus ϕ_s curves from four experimental $C-V$ characteristics of Fig. 2. (a) Using C_{di} values extracted using the proposed technique. (b) Using C_{di} values extracted using the technique of Kar [11], [12].

and Kar's [11], [12] techniques. When our values of C_{di} are used, the shapes of the extracted curves are very similar to our calculated $C_{acc}-\phi_s$ curves (Fig. 5), including the initial exponential portion in weak accumulation and deviation from linearity in strong accumulation for the Y-O-Si/p-Si device [19]. This correspondence may be viewed as an experimental verification of our model and extraction technique. The presence of the linear region in the extracted C_p also confirms our assumption that C_{it} is indeed negligible in moderate and strong accumulation. The extracted $C_p-\phi_s$ using C_{di} determined by Kar's technique is found to be exponential, in agreement with the assumption of Kar [11], [12]. This is not surprising because the use of the "semiclassically" determined C_{di} in extracting C_p obviously recovers the semiclassical exponential curve C_p .

IV. CONCLUSION

We have presented a model for the accumulation gate capacitance of n- and pMOS structures with ultrathin high- κ gate dielectrics. The self-consistent model incorporates QM effects including wave function penetration. The accuracy of the model has been verified by comparing its results to those of another $C-V$ simulator and to published experimental data. Inclusion of wave function penetration effect is essential for accurately simulating accumulation capacitance of high- κ gate dielectric materials. The presented model has been used to obtain a physically based relationship between C_{acc} and ϕ_s . This relationship has been used to propose a simple technique to extract C_{di} from measured $C-V$ data. The proposed technique includes the strong QM effects on the MOS capacitance. The accuracy of our technique is validated by applying it successfully to different simulated and experimental $C-V$ data.

Our technique is also compared with another C_{di} extraction technique available in the literature, and the improvements in our method are demonstrated.

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