Virtual-Source based accurate model for predicting noise behaviour at high frequencies in nanoscale PMOS SOI transistors

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Received 4 August 2017; accepted

Abstract

Complementary Metal Oxide Semiconductor (CMOS) technology at the nanometre scale is an excellent platform to implement monolithically integrated systems because of the low cost of manufacturing and ease of integration. Newly developed CMOS Silicon on Insulator (SOI) transistors that are currently developed are suitable for use in radio frequency circuits. They find applications in many areas such as 5G telecommunication systems, high speed Wi-Fi and airport body-scanners. Unfortunately, the models for CMOS SOI transistors that are currently used in these circuits are inaccurate because of their complexity. The models currently used require the optimization of more than 200 variables. This paper aims to accurately create a scalable model of a P-type MOS transistor using a Virtual Source (VS) model with much less complexity. The VS model's DC characteristics will require the optimization of only ten parameters and is supplemented with parasitic resistances, inductances and capacitances to accurately predict behaviour at radio frequencies. These parameters were optimized two at a time using a multivariate optimization algorithm while fixing the remaining parameter's values within a certain range. A simulation of the voltage and current at the drain of the transistor was performed and the resulting I-V curves were plotted. A frequency simulation was also conducted in order to test the high frequency performance of the MOSFET. A typical I-V characteristic curve for a PMOS was obtained with no change in shape when the transistor width was scaled. The model's performance under high frequencies also matched those displayed by a standard 45nm PMOS. The I-V characteristic plots that were obtained displayed the general behaviour of a p-type MOSFET under those voltage conditions. This demonstrates that the Virtual source model is able to predict the general behaviour of the I-V characteristic curves of the p-type MOSFET as well as function properly at high frequencies typically seen in RF circuits.

Keywords: CMOS SOI, microwave frequency circuits, Virtual Source model, thermal module, high frequency model, noise

1. Introduction

Nanoscale CMOS SOI technology is a very robust platform that can be used to implement monolithic (single-chip) integrated circuits. It has several advantages over other platforms, such as cost of manufacturing and ease of integration with other digital circuits. Significant advancements in nanoscale MOSFETs have allowed them to be successfully implemented in microwave as well as mm-wave circuits, due to their high cut off (f_T) and maximum oscillation (f_{MAX}) frequencies. However, it is still difficult to implement these nanoscale MOSFETs with immediate success due to the numerous variables present in the models currently available. These difficulties are even more pronounced when it comes to modelling the characteristics of sub-100nm MOSFETs, which are in great demand in various applications such as 5G telecommunication networks, high speed Wi-Fi, biotechnology and airport body scanners. The reason for the availability of such models is because they require the difficult task of optimizing over 200 variables for an accurate representation of MOSFET performance, a task which can be quite daunting. [1]

One solution that has been proposed to rectify this process is by using another MOSFET modelling method called the Virtual-Source (VS) model which uses 10 parameters and can accurately describe the nonlinear DC characteristics of CMOS SOI transistors. [3][4][7] This VS model assumes a semi-ballistic transport mechanism, which allows for good accuracy. (Assumption of transport of electrons over long distances without any scattering.) The drawback of using this model, is that it does not yet have statistical modelling required to capture corner simulation. One solution proposed is the assumption that most of the noise generated at high frequencies is due to the device's thermal noise. While this assumption works for most cases (long-channel MOSFETs), it still fails to completely explain the noise of nanoscale transistors. To account for this discrepancy, the shot noise, which is noise generated by the random injection of electrons from the source into the channel, is also considered. [5][6] This inclusion seems to account for the noise seen in short-channel MOSFETs and as such, a combined shot-thermal noise model is used to accurately describe the complete noise behaviour of the device at high frequencies. [9]

This research aims to design a compact, scalable and easy-to-implement MOSFET model for PMOS transistors based off of the commercial Global Foundry 45nm CMOS SOI technology. [8] The Virtual-Source model is used to describe the non-linear DC characteristics of the MOSFET. It is also supplemented by geometry and bias dependent parasitic resistances, capacitances and inductances, to be suitable for employment at high frequencies, in the range of 1-50GHz.

2. Methods

A Virtual-Source model was utilized to simplify the modelling process without sacrificing accuracy. The 10

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modelling parameters required to describe the DC behaviour of the model are listed in Table 1. The model was also supplemented with parasitic capacitances, resistances and inductances. These parasitic elements are specifically for a transistor width of 126µm.
The extracted parameters were optimized using a multivariate optimization algorithm after observing the effects of each parameter on the Drain current. Nine of the ten DC parameters were fixed within a suitable range while the remaining the remaining parameter was optimized. A test circuit was developed to assess the DC performance of the VS model, the circuit of which is shown in Fig. 2. A simulation of the voltages and currents of the MOSFET was run for each given combination of parameter values. A linear sweep of the drain to source voltage (V_{DS}) from 0V to -1.2V was performed at varying voltages between the gate and source (V_{GS}). The V_{GS} voltage was varied between 0V to -1.2V as well in steps of 0.24V. The resulting drain current obtained was plotted against the drain to source voltage (V_{DS}).
Further testing was performed to ensure MOSFET performance at high frequencies. A test bench similar to the one developed for DC analysis was set up with additional inductances and capacitances to prevent damage to the MOSFET, as shown in Fig. 3. An s-parameter analysis was performed on the model, using frequency as the sweeping parameter, to check the variation in current gain (H_{21}) as well as the power gain (G_{max}). The model was tested up to 50GHz and the obtained graphs were extrapolated to discern the cut-off and maximum oscillating frequencies. The frequencies at which the model's H_{21} and G_{max} were noted to be 0dB were marked as the cutoff frequency (f_T) and the maximum oscillating frequency (f_{MAX}) respectively. [10]

Table 1
VS parameters describing DC characteristics

Parameters	Notes
L_g (nm)	Channel Length
L_{ov} (nm)	Total Overlap Channel Length
C_g (µF/cm^2)	Gate Capacitance
R_s (Ω µm)	Series Contact Resistance
DIBL (mV/V)	Drain-induced Barrier Lowering
SS (mV/dec)	Subthreshold Swing
V_{t0} (V)	Threshold Voltage
v_{xo} (cm/s)	Electron Velocity at Virtual Source
µ (cm^2/V s)	Mobility
α	Fitting Parameter
β	Fitting Parameter

Table 2
Supplemented Parasitic elements

Width (µm)	126
C_{pd} (fF)	13.653
C_{pg} (fF)	12.113
L_g (pH)	85.37
L_d (pH)	35.371
L_s (pH)	44.549
R_g (Ω)	6.4361
R_d (Ω)	1.2182
R_s (Ω)	1.2182

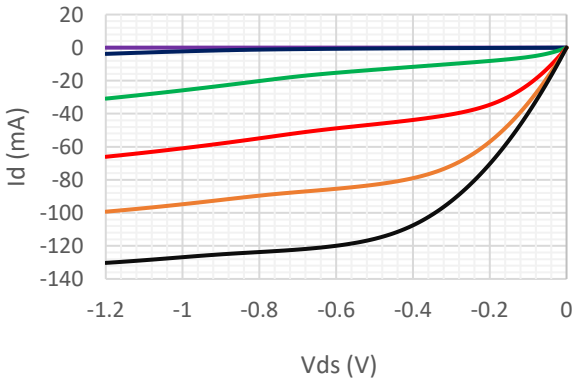

Fig. 1. I-V characteristic curve at varying gate voltages (V_{GS}) for 45nm Global Foundries PMOS model.

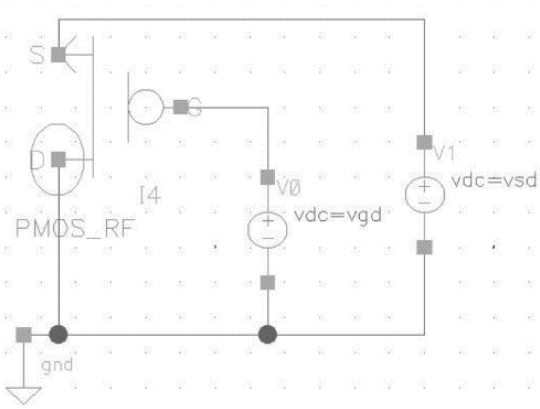

Fig. 2. Test Circuit for PMOS model. VGD and VSD are used as design variables and are related to VDS and VGS by the following equations: (1) $V_{GD} = V_{GS} + V_{SD}$ and (2) $V_{SD} = -V_{DS}$

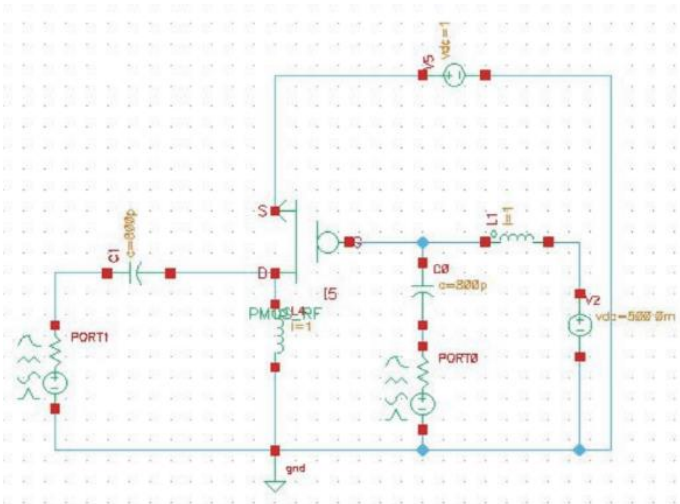

Fig. 3. Test circuit for observing performance of MOSFET at high frequencies (1-50GHz). Port 0 is the input and Port 1 is the output. External capacitances are set at 800pF and external inductances are 1H. Gate is biased at 0.5V while the Source is biased at 1.0V.

3. Equations

(1) $I_{ds} = -\mathrm{W} * \mathrm{Q}_i(\mathrm{x}_0) * \mathrm{v}_{x0} * F_{sat}$

(2) $\mathrm{F}_{sat} = \frac{\mathrm{V}_{ds}/\mathrm{V}_{dsat}}{(1+(\mathrm{V}_{ds}/\mathrm{V}_{dsat})^{\beta})^{1/\beta}}$

(3) $\mathrm{V}_{tp} = \mathrm{V}_{t0} - \mathrm{DIBL} * \mathrm{V}_{ds}$

(4) $F_f = \frac{1}{1+\mathrm{e}^{\frac{\left|\mathrm{V}_{gs}-(\mathrm{V}_{tp}+0.5\alpha\varphi_T)\right|}{\alpha\varphi_T}}}$

(5) $\mathrm{Q}_i(\mathrm{x}_0) = \mathrm{C}_{inv} * \mathrm{n}\varphi_T * \ln\left(1+\mathrm{e}^{\frac{-\left(\mathrm{V}_{gs}-(\mathrm{V}_{tp}+\alpha\varphi_T * F_f)\right)}{\mathrm{n}\varphi_T}}\right)$

(6) $V_{dsats} = \mathrm{v}_{x0} * (L_g - L_{ov})/\mu_0$

(7) $V_{dsat} = V_{dsats} * (1 - F_f) + \varphi_T * F_f$

4. Results

The supplementary parasitic components present in the VS model are listed in Table 2. The extracted VS parameter values are listed in table 3 along with their relationship with the drain current. These parameter values yielded the I-V characteristic curves shown in Fig. 4 for the voltages applied in the simulation. The I-V characteristics were found to be within 7.1% of the standard PMOS I-V characteristics as shown by the Global Foundries model.

Table 3
Extracted VS parameter values for PMOS model

Parameters	PMOS	Effects on I_D
L_g (nm)	40	Inversely related to Drain current
L_{ov} (nm)	12	Inversely related to Drain Current
C_g (μF/cm^2)	2.475	Directly related to Drain current
R_s (Ω μm)	102.328	Affects curvature of plot in linear region
DIBL (mV/V)	141	Affects threshold voltage at higher V_{DS}
SS (mV/dec)	93.554	Slope of the curves at voltages below V_{t0}
V_{t0} (V)	-0.475	Affects transition of I-V curve from linear to saturation and current outputted
v_{x0} (cm/s)	5.586e6	Directly related to Drain current
μ (cm^2/V s)	77.82	Directly related to drain current
α	6.85	Changes slope of curve at low V_{DS} voltages
B	3.5	Changes slope of curve at low V_{DS} voltages

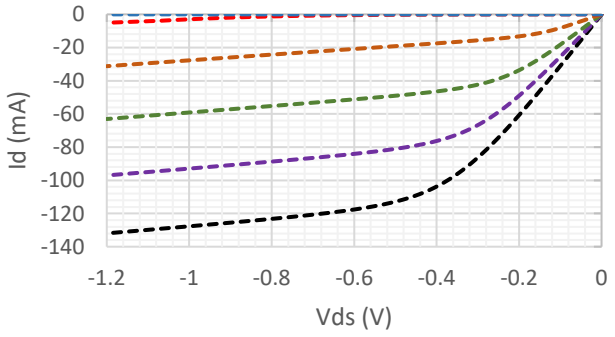

Fig. 4. Obtained I-V characteristics for the VS model based on the values from table 1. Each curve represents an I_D vs V_{DS} sweep at a particular V_{GS} voltage. V_{GS} increases from 0V to -1.2V from top trace to bottom trace.

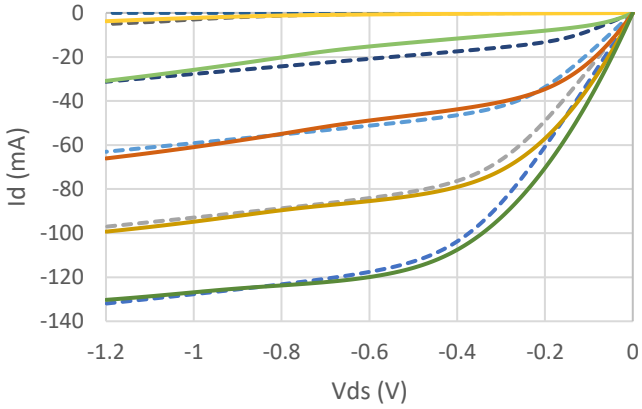

Fig. 5. Overlay of obtained I-V characteristics from VS model over standard I-V characteristics. 7.1% error between the two sets of curves. Dashed lines represent VS models I-V characteristics while solid lines are the standard characteristics. Again, V_{GS} increases from 0V to -1.2V from top to bottom trace.

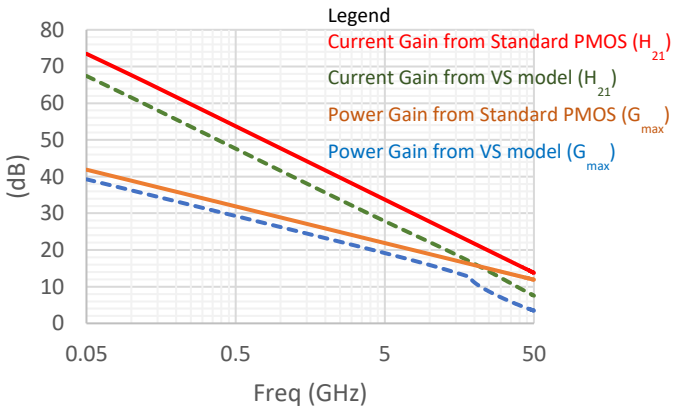

Fig. 6. Overlay of current and power gain of VS model over the standard model's parameters. VS model displays the exact same performance and trends as a standard 45nm PMOS up to 50GHz.

5. Discussion

The values for the model parameters, listed in Table 3, were determined using equations (1) - (7), as listed in section 3, while simultaneously gauging their effect on the I-V characteristics of the model. The equations were used to predict the extent of the effect each parameter would have on the output drain current allowing for better optimization of the parameter values. Parameters such as gate capacitance, mobility and electron velocity at virtual source were found to directly impact the drain current. Increasing or decreasing these parameters brought about a corresponding change in the currents outputted at different V_{GS} voltages. Parameters such as series resistance and threshold voltage affected the transition of the curves from the linear to the saturation region. An increase in the threshold voltage as found to reduce the current outputted

at each curve while also shifting the transition point from linear to saturation to a lower voltage. A decrease in threshold voltage was shown to do the opposite. A sharp increase in the series contact resistance began to induce a kink in curves at high V_{GS} and low V_{DS} voltages where the current would rapidly increase and then drop down to expected levels. DIBL mainly affected the threshold voltage at high V_{DS} values. An increase or decrease in DIBL causes an increase or decrease in the current outputted at low V_{GS} and high V_{DS} voltages. The subthreshold swing inversely affected the slope of the curve in the linear region while α and β were simply parameters used to shape the curve to match the standard characteristics. The I-V characteristic graphs were obtained at V_{GS} = 0V, -0.24V, -0.48V, -0.72V, -0.96V and -1.2V and for each curve V_{DS} was swept from 0V to -1.2V. For the frequency test the model performance was tested from 1GHz-50GHz and H_{21} and G_{max} were measured at steps of 50MHz. The frequency at which H_{21} and G_{max} equal 0dB is the point at which the model's cut-off (f_T) and maximum oscillation (f_{MAX}) frequencies were determined through extrapolation of their graphs beyond 50GHz. These frequencies were found to be 102.456GHz for the f_{MAX} and 123.8GHz for the f_T of the VS model, while the standard model had f_{MAX} at 774.1GHz and f_T at 244.22GHz. Although the data presented here is specifically for a 45nm PMOS having a width of 126µm, it should be noted that this model is scalable and displays the same performance with minor changes in the values of the extrinsic parasitic resistances, inductances and capacitances which can be extracted from the measured S-parameter data.

6. Conclusions

A publicly available Process Design Kit (PDK) containing a simpler, streamlined and scalable 45nm MOSFET model using the Virtual Source model has been developed. Through the optimization of the model parameters and DC analyses performed, the DC characteristics of the MOSFET model has been verified to produce results within a 7.1% error margin when compared to the standard 45nm model provided by Global Foundries. Though the parasitic elements have been extracted specifically for
The model's accuracy is further confirmed through inspection of its performance under high frequencies. The close relation between the standard and the models cut-off and maximum oscillation frequencies shows that the model behaves exactly as expected under high frequencies.
The work conducted in this paper demonstrates the advantages of using the VS model. Nearly identical DC performance is attained by utilizing a fraction of the parameters as compared to previous models.

Acknowledgements

The authors would like to gratefully acknowledge the contributions from the NCN-NEEDS program, which is funded by the National Science Foundation, the NCN group and the SURF program for their valuable input in this research.

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