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Room temperature device performance of electrodeposited InSb nanowire field effect transistors

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InSb nanowires have been formed by electrodeposition in porous anodic alumina templates and employed as transistor channels. The 100 nm diameter nanowires had a zinc blende crystal structure. Single-nanowire field-effect transistors (NW-FETs) with a channel length of 500 nm exhibited on-currents of ~40 μA, on/off ratios of ~16–20, drain conductances of ~71 μS and field-effect electron mobility of ~1200 $cm^2\ V^{-1}\ s^{-1}$. Compared with reported NW-FETs, the on-current is large and the current saturation occurs at low source-drain voltages. These characteristics can be understood in terms of velocity saturation effects with enhanced scattering. © *2011 American Institute of Physics*. [doi:10.1063/1.3587638]

Nanowire field-effect transistors (NW-FETs) have attracted significant research interest in recent years.[1–3] While a number of NW materials have been studied, narrow band gap materials can provide one-dimensional (1D) quantization effects at modest diameter and high mobility, making them suitable candidates for future nanoelectronics applications. Compared to other common semiconductors, InSb has a high room temperature mobility, low effective mass, and low (direct) band gap, making it suitable for use in applications such as high-speed, low-power transistors, tunneling FETs, and infrared optoelectronics devices.[4,5] The first reported high-speed and low-power InSb FETs were $InSb/In_{1-x}Al_xSb$ enhancement mode devices operating with an f_{max} of 89 GHz at $V_{ds} < 0.5$ V.[6] Intel and QinetiQ have demonstrated InSb quantum well transistors with unity gain cutoff frequencies above 250 GHz.[7] The results on planar devices reflect the potential for enabling high-performance devices.

The relatively large lattice mismatch between InSb and commonly available semiconductor substrates presents a significant challenge for development of planar devices employing InSb epilayers. However, NW structures can be grown without a lattice-matched substrate. The vapor-liquid-solid (VLS) growth mechanism, where a metal seed particle of desired diameter dispersed on a substrate acts as a point of initiation of NW growth, has been utilized to grow InSb NWs.[8] Reported InSb NW-FET showed very good performance with either ambipolar or *n*-type channel conduction.[9–11] However, repeatable growth of InSb NWs is challenging due to the difficulty in the stoichiometric growth of InSb due to vapor pressure differences of In and Sb and processing temperatures, barrier oxide layer formation around NWs and various twin defect and stacking fault formation in the structure.[12–14] Despite widespread use of the VLS method, Hannon *et al.* recently demonstrated that in Si NWs there is always a wetting issue arising from the diffusion of Au atoms into the NW sidewalls from the seed particle as the NW growth continues.[15] An alternative growth method uses electrodeposition of the desired ionic species into the nanochannels of a porous anodic alumina (PAA) template with approximately cylindrical pores.[16] The first reported InSb NWFETs using NWs grown by electrodeposition showed *p*-type channel conduction with a hole mobility of ~57 $cm^2\ V^{-1}\ s^{-1}$.[17] In this letter, we report NW-FETs employing individual, electrodeposited InSb NWs with high on-current (I_{ON} ~ 40 μA) per NW and current saturation at low drain-source (S/D) voltage (V_{ds}).

Commercial PAA templates (Anodisc 13 from Whatman) with a thickness of 60 μm and a pore diameter that tapered from 20 to 200 nm over the thickness were utilized. A working electrode was formed by e-beam evaporation of 100 nm Au on the 20 nm pore side of the PAA surface. A Pt-mesh counter electrode and an Ag/AgCl (KCl) reference electrode were employed in a three-electrode electrochemical cell. The InSb NWs were grown by direct electrodeposition in an aqueous solution, at *p*H 1.8 and at a reduction potential of −1.5 V.[16] The as-deposited NWs were annealed in argon atmosphere at 125 °C for 6 h and then at 420 °C for 4 h.[16] The PAA template was then dissolved in 1M KOH solution (overnight) and the NWs were released into isopropyl alcohol via sonication. The NWs were imaged using a Hitachi field emission scanning electron microscope (FESEM) and FEI Titan 80–300 kV transmission electron microscope (TEM).

Back-gated NW-FETs were fabricated using a p+ silicon substrate as the gate contact and a 20 nm thermal oxide as the gate dielectric. Following deposition of alignment markers, the NWs were dispersed onto the wafer by solution casting. Source and drain contacts were then individually aligned to each wire and defined by an e-beam lithography, nickel deposition (90 nm), and liftoff process. Channel lengths (L_{CH}) and contact lengths were both 500 nm. The current-voltage (I-V) characteristics of the devices were measured using a semiconductor parameter analyzer.

Figure 1 shows a high resolution TEM (HRTEM) image of one of the electrodeposited InSb NWs. The wires were found to be single crystalline without any visible dislocations, twin defects or stacking faults. The magnified image

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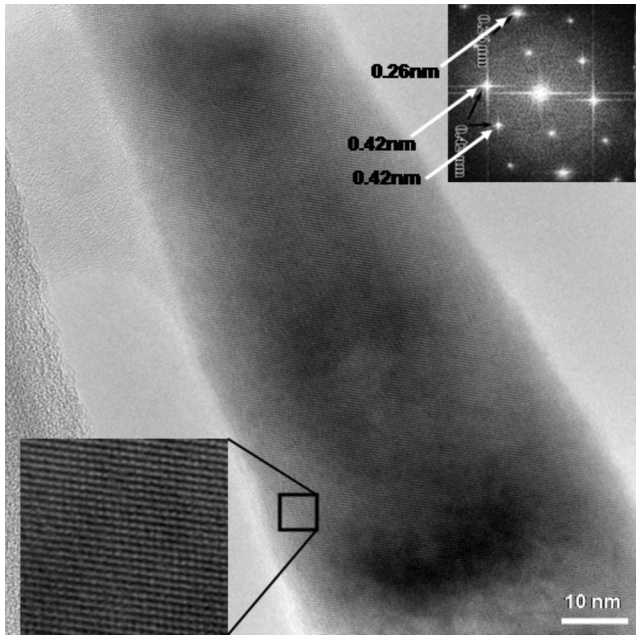

FIG. 1. HRTEM image of an InSb NW. Lower left inset shows magnified view of the individual lattice planes. Upper right inset shows the SAED pattern of the InSb NW.

shows the lattice planes of the NW along with the [111] growth direction. The inset shows the selective area electron diffraction (SAED) pattern obtained from FFT analysis, which indicates a crystal structure consistent with that of bulk InSb without any crystal defects. X-ray diffraction indicated a zinc blende structure with a lattice constant of 6.4782 Å. The wires were generally found to be tapered, consistent with the tapering in the PAA template. Near the narrow end, a diameter of ~100 nm is obtained over a length of ~2 μm. The device (on which the present data is shown) has a uniform diameter of around 100 nm as confirmed from the FESEM image.

The measured n-channel, room temperature output characteristics of the device are shown in Fig. 2 after the devices are annealed at 300 °C in argon ambient for 10 min. Before

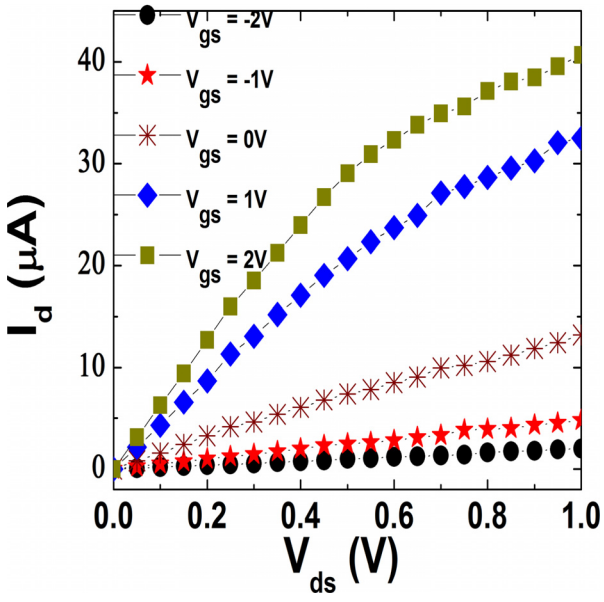

FIG. 2. (Color online) Output characteristics (I_d-V_{gs}) of the device after annealing in argon.

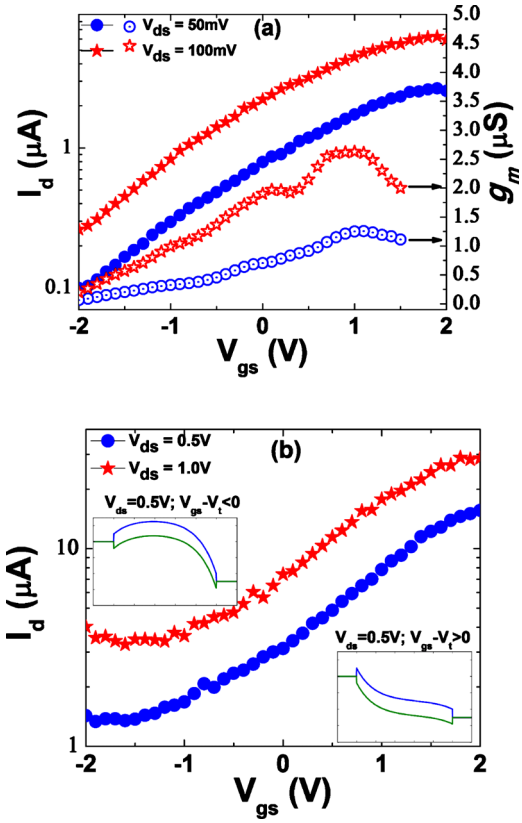

FIG. 3. (Color online) (a) Transfer characteristics (I_d-V_{gs}) and the transconductance versus gate voltage of the annealed device in linear regime (V_{ds} of 50 and 100 mV). (b) Transfer characteristics (I_d-V_{gs}) of the annealed device in saturation regime. Figure 3(b) inset illustrates the band diagram of 500 nm channel InSb NWFET at V_{ds}=0.5 V with subthreshold and above threshold gate voltages.

annealing the representative devices showed no visible current saturation, channel resistance (R_{ds}) of 90 k Ω for small V_{ds} and a gate-source voltage (V_{gs})=2 V, and heavily contact-dominated output characteristics (indicated by diode-like characteristics). After annealing, the low-field R_{ds} at V_{gs}=2 V improved to 14 k Ω (indicating reduction in contact effects upon annealing) and the devices exhibited I-V characteristics more consistent with channel-dominated behavior including saturation, consistent with prior report.[3] The on-currents were found to be around 40 μA for drain voltages of 1 V, significantly higher than reported values on wider band gap materials. The extracted transconductance in the linear regime of operation is shown in Fig. 3(a) and the peak g_m of 2.75 μS for V_{ds}=100 mV was obtained from the plot. Using a cylinder-on-plate capacitance model for the gate (since $d_{NW} \gg t_{ox}$) and the peak g_m value,[18] an effective electron field-effect mobility of $\mu \sim 1200$ cm^2 V^{-1} s^{-1} was extracted. This value is significantly lower than reported values for bulk InSb, indicating that contact effects or scattering mechanisms such as boundary scattering play a significant role. In the saturation region (V_{ds}=1 V), a peak g_m of 16 μS was extracted and the output resistance was ~75 k Ω, yielding to an intrinsic gain ($G_m \times R_{ds}$) of 1.2

In a long-channel metal-oxide-semiconductor FET model, I_d saturation corresponds to channel pinch-off at the drain end of the channel, and the saturation (knee) voltage is $V_{knee}=(V_{gs}-V_{th})$. In our devices, current saturation occurred at V_{ds} values around 500 mV even for $(V_{gs}-V_{th})$ ~3 V. This early onset of saturation indicates that a mechanism

other than channel pinch-off is responsible for the saturation. We did not observe hard saturation in the drain current up to $V_{ds}=1$ V. The increase in I_d with increasing V_{ds} (beyond V_{knee}) can be explained, at least in part, by modulation of the channel potential (particularly near the source) by the drain. Due to 1D electrostatics for the case in which the gate overlaps the S/D regions, the band bending near the source and drain is exponential with a characteristic length of $\lambda = \sqrt{(d_{wire} d_{ox} \varepsilon_{wire}/\varepsilon_{ox})} \approx 90$ nm.[19] Although a channel length of $\sim 5\lambda$ should be long enough to avoid substantial short channel electrostatic effects, a modest modulation of the source barrier is expected. Fringing fields from the extended drain contact also will modulate the channel potential.

Figure 3(a) illustrates the transfer characteristics of the annealed devices in the linear regime at drain voltages of 50 mV and 100 mV, respectively, with an $I_{ON}/I_{OFF} \sim 16-20$. These measurements were done following the high V_{ds} measurements, which may have caused a bias-induced shift of threshold voltage to a more negative value. Subthreshold swings of several volts per decade were observed, which can be explained in part by the relatively thick body (NW diameter) but also likely indicating the presence of a high level of interface traps between the oxide and NWs which is common for this bottom-gate geometry, particularly on SiO_2.

Figure 3(b) shows the transfer characteristics of the annealed devices in the saturation regime at drain voltages of 0.5 V and 1 V, respectively. An I_{ON}/I_{OFF} ratio of $\sim 12-15$ was observed and the threshold voltage was estimated near -1 V. The inset shows the expected energy band diagram along the 500 nm channel at S/D voltage of 0.5 V and both at low and high gate bias points, reflecting the exponential potential profiles. Due to the low band gap, ambipolar behavior starts to appear at this drain voltage and higher (V_{ds} of 1 V also shown) and gate voltages below threshold. In this bias regime, a thin drain barrier allows electrons to tunnel out of the valence band into the drain, increasing the current. This is consistent with the measured transfer characteristics which show slight increase in current at high V_{ds} and low V_{gs}, but no drastic increase at lower V_{ds} [Fig. 3(a)]. The band gap of the wire can be approximated from the I_{ON}/I_{OFF} ratio to be ~ 0.20 eV, using the relationship $(I_{ON}/I_{OFF}) = (1/2)\exp(E_g/2kT)$. This value is consistent with the accepted value of 0.175 eV for crystalline InSb. While this relationship is strictly correct for a 1D, ballistic channel at low drain voltages, it can provide an estimate of band gap for devices in which both electrons and holes can be readily injected and heavily doped "body" regions are not present.

The carrier velocity can be estimated and compared to the bulk saturation velocity v_{sat} for InSb. The number of carriers in the channel per unit length at $V_{gs}=2$ V can be estimated by the gate capacitance and gate voltage to be $\sim 4.7\times 10^7$ cm^{-1}. In conjunction with the measured saturation current of 40 μA, an average electron velocity can be calculated to be $\sim 5.3\times 10^6$ cm/s. This is significantly lower than the 4×10^7 cm/s v_{sat} of bulk InSb.[20] While detailed calculations of v_{sat} in NWs are not available, a reduced v_{sat} could result from enhanced scattering (surface, electron–phonon, and electron–electron) in the NWs and is generally consistent with the observation of mobility lower than reported bulk values. For velocity saturation, the critical electric field (E_{crit}) should to be related to the v_{sat} by $v_{sat} \sim \mu E_{crit}$. Assuming that our inferred velocity corresponds to v_{sat}, and using our measured μ, we estimate $E_{crit} \sim 5000$ V/cm. The electric field at the onset of saturation ($V_{knee}/L_{CH} \sim 10$ kV/cm) is consistent with this estimate, indicating that a velocity saturation model may be valid.

The room temperature ballistic mean free path of the electrons in bulk InSb is reported to be 580 nm.[6] Based on the channel length in the present study (500 nm), one might expect the devices to be operating in a semiballistic transport regime. However, the measured g_m in our NW-FET is significantly smaller than the conductance quantum G_0 ($G_0 = 2e^2/h = 77.5$ μS), indicating that the devices are not in the ballistic limit. This is consistent with the observation of μ lower than the bulk value and associated enhanced scattering.

In summary, n-channel InSb NWFETs were fabricated using single crystalline electrodeposited InSb NWs. The measured room temperature I-V characteristics show low on-resistance, high drain current and saturation at low V_{ds}. An I_{ON}/I_{OFF} ratio of ~ 20 in the linear and saturation regimes and an electron mobility of 1200 cm^2 V^{-1} s^{-1} were achieved. The I_{ON}/I_{OFF} ratio and ambipolar behavior are both indicative of the low band gap of the InSb NWs.

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[1] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, Nature (London) **424**, 654 (2003).
[2] X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, Nature (London) **409**, 66 (2001).
[3] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, Nano Lett. **3**, 149 (2003).
[4] T. Ashley, L. Buckle, S. Datta, M. T. Emeny, D. G. Hayes, K. P. Hilton, R. Jefferies, T. Martin, T. J. Phillips, D. J. Wallis, P. J. Wilding, and R. Chau, Electron. Lett. **43**, 777 (2007).
[5] A. Rogalski, Prog. Quantum Electron. **27**, 59 (2003).
[6] T. Ashley, A. B. Dean, C. T. Elliott, R. Jefferies, F. Khaleque, and T. J. Phillips, Tech. Dig. - Int. Electron Devices Meet. **1997**, 751.
[7] S. Datta, T. Ashley, J. Brask, L. Buckle, M. Doczy, M. Emeny, D. Hayes, K. Hilton, R. Jefferies, T. Martin, T. Phillips, D. Wallis, P. Wilding, and R. Chau, Tech. Dig. - Int. Electron Devices Meet. **2005**, 763.
[8] Y. Wu and P. Yang, J. Am. Chem. Soc. **123**, 3165 (2001).
[9] D. Candebat, Y. Zhao, C. Sandow, B. Koshel, C. Yang, and J. Appenzeller, Proceedings of 67th Device Research Conference, University Park, PA, June 22–24 (2009).
[10] H. A. Nilsson, P. Caroff, C. Thelander, E. Lind, O. Karlstrom, and L. E. Wernersson, Appl. Phys. Lett. **96**, 153505 (2010).
[11] Y. Wang, J. Chi, K. Banerjee, D. Grutzmacher, T. Schapers, and J. G. Lu, J. Mater. Chem. **21**, 2459 (2011).
[12] U. Philipose, G. Sapkota, J. Salfi, and H. E. Ruda, Semicond. Sci. Technol. **25**, 075004 (2010).
[13] F. Zhou, A. L. Moore, M. T. Pettes, Y. Lee, J. H. Seol, Q. L. Ye, L. Rabenberg, and Li Shi, J. Phys. D: Appl. Phys. **43**, 025406 (2010).
[14] P. Caroff, K. A. Dick, J. Johansson, M. E. Messing, K. Deppert, and L. Samuelson, Nat. Nanotechnol. **4**, 50 (2009).
[15] J. B. Hannon, S. Kodambaka, F. M. Ross, and R. M. Tromp, Nature (London) **440**, 69 (2006).
[16] X. Zhang, Y. Hao, G. Meng, and L. Zhang, J. Electrochem. Soc. **152**, C664 (2005).
[17] M. I. Khan, M. Penchev, X. Jing, X. Wang, K. N. Bozhilov, M. Ozkan, and C. S. Ozkan, J. Nanoelectron. Optoelectron. **3**, 199 (2008).
[18] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd ed. (Wiley, New York, 2006), p. 501.
[19] R.-H. Yan, A. Ourmazd, and K. F. Lee, IEEE Trans. Electron Devices **39**, 1704 (1992).
[20] R. Asauskas, Z. Dobrovolskis, and A. Krotkus, Sov. Phys. Semicond. **14**, 1377 (1980).