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We demonstrate experimentally single-electron quantum dots using a single-top-gate transistor configuration on a composite quantum well. The data indicate a 15 meV Coulomb charging energy and a 20 meV orbital energy spacing, which imply a quantum dot of 20 nm in diameter. Combining with the inherent advantage of a large electron g^* factor in InAs, our demonstration is significant for a solid state implementation of a scalable quantum computing. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2202100]

A major challenge for quantum computing[1] is scaling quantum systems up to a large number of logical qubits. Solid state implementations of qubits offer the advantage of being scalable, and, in particular, those based on semiconductors can be integrated by existing technologies. The two Zeeman states of an electron spin in a quantum dot (QD) provide a promising candidate for a qubit,[2] and lateral QDs provide the best opportunity for scaling. Spins in lateral QDs in the GaAs/$Al_xGa_{1-x}As$ single-electron transistors (SETs) have been intensively investigated,[3–6] and considerable progress has been made in their development as qubits and quantum gate by coupling two qubits. However, there are inherent shortcomings in this system that may inhibit the ultimate implementation of a scalable quantum computation based on them. In particular, it is necessary to use additional quantum point contacts (QPCs) adjacent to the SET to serve as an electrometer to verify that only a single electron remains in the dot.[4,6] The necessity for QPCs hinders scaling.[7] Furthermore, the GaAs system is characterized by a small energy level spacing and a small g factor ($g^*=-0.44$). This results in a considerable mixing of orbital levels, causing the Zeeman-split ground level in GaAs dots from the ideal two-level system, and an increase of dephasing.

In this letter, we propose and demonstrate an enhancement-mode lateral SET. In contrast to the depletion-mode lateral[3–6] and vertical[7] SETs that reach a one-electron regime by expeling electrons from multielectron QDs, the enhancement-mode SET contains no electrons initially. Our SET structure uses a single top gate to create two symmetric tunnel barriers and make electrons tunnel into this empty QD one at a time. This enhancement-mode setting possesses the advantages of both vertical and lateral depletion-mode SETs and more. First, the tunneling barriers that define a QD are, to the first order, independent of the top gate voltage in the few-electron regime, which makes possible a conductance identification of a single electron. Second, the lateral configuration makes the control of the coupling of two dots straightforward. In addition, the simplicity of a single top gate configuration makes possible the realization of a two-dimentional (2D) QD array that would be necessary to allow the transportation of qubits.[8]

The samples used in this work to demonstrate the novel SET concept are InAs/GaSb composite quantum wells (CQWs).[9] The InAs/GaSb heterojunction has a staggered energy band alignment, as shown in Fig. 1(a), and the CQW becomes a narrow-band-gap semiconductor, whose band gap is tunable by the thicknesses of the two QWs and is ~100 meV in our case. The CQW is sandwiched by p-doped $Al_xGa_{1-x}Sb$ barriers, resulting in 2D holes in the GaSb QW. Developing a single-electron transistor in the InAs system is an important step. InAs quantum dots are characterized by a large orbital splitting, and therefore Coulomb blockade ef-

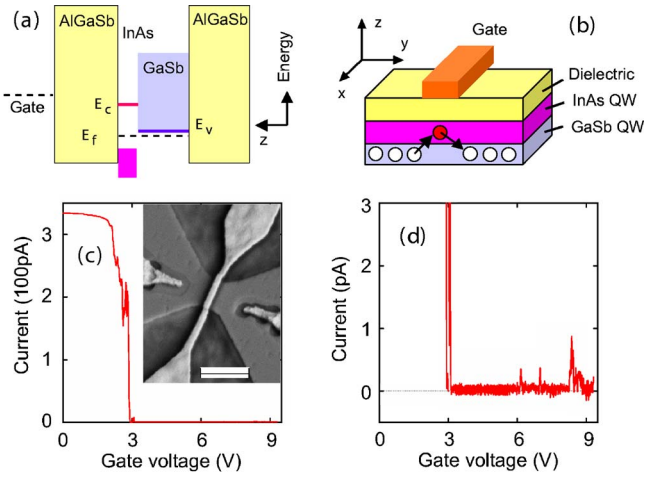

FIG. 1. (Color online) (a) Schematic of the band diagram of the composite quantum well. (b) Schematic of the enhancement-mode single-electron transistor, where one electron is induced in the InAs layer by a top metal gate. (c) The dc current-voltage characteristic of a gated single-electron transistor, where the drain current is plotted against the sweeping gate voltage. The inset shows a scanning electron micrograph of a transistor where the scale bar is 1 μm in length. (d) Same as that in (a), but with a different drain current scale where the peaks in the current results from a single-electron tunneling.

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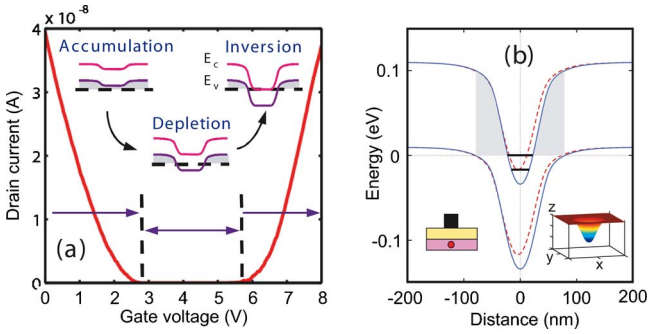

FIG. 2. (Color online) (a) The dc current-voltage characteristic of a gated Hall bar transistor. The insets plot the schematic potential profiles along the current direction for three operating regimes, where E_c (E_v) is the first electron (hole) subband in the InAs (GaSb) layer. (b) Calculated potential profiles when the first (dashed curve, where the center of the dot is shifted for comparison of the tunneling barrier) and the second quantization levels (solid) are aligned with the Fermi level. Here the Coulomb charging energy is excluded and the shaded areas illustrate the tunneling barriers. The insets show the model capacitor structure and a simulated 2D potential plot, where x and y dimensions are 400 nm and the energy span (z) is 150 meV.

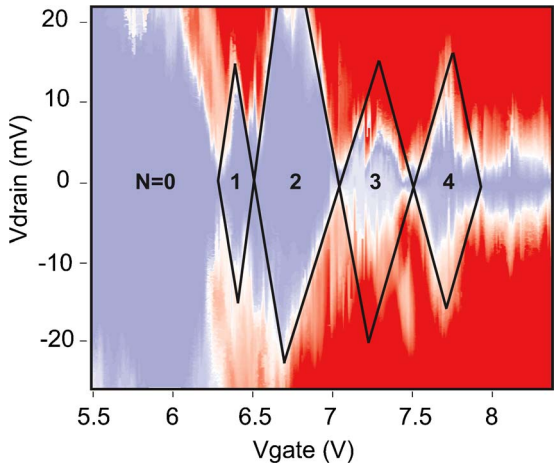

FIG. 3. (Color online) Diamond chart of an enhancement-mode SET measured at 4.2 K.

fects can be observed at higher temperatures. In addition, for quantum computing, it is particularly important that the InAs system has a large g factor ($g^* \sim -15$). The reason is that a qubit manipulation is achieved by Rabi pulses, and the duration of these pulses is controlled by the product of the g factor and the ac field, i.e., a larger g factor gives the opportunity to use a smaller ac magnetic field to achieve a certain duration of pulses. Therefore, the integrated wires on the sample will carry smaller ac currents, and dissipation effects will be reduced.[10]

However, the InAs system is well known as a system that is very difficult to control by electric gates because of the problem of leakage currents. Our achievement of InAs SET is made possible by reducing leakage currents primarily using an additional SiO_2 layer below the gate metal. Figure 1(b) shows the schematic of the InAs/GaSb transistor structure. The top gate voltage (V_{gate}) controls the population and the type of carriers in the CQW. At $V_{gate}=0$, the transistor conducts because of the 2D holes in the GaSb layer. As the top gate is biased to be more positive, the 2D holes in the GaSb QW are gradually depleted. A further increase of the top gate bias results in the formation of electrons in the InAs layer. Such gate-controlled transition from the accumulation of 2D holes to a depletion and finally to an inversion of electrons is verified by large sized, gated Hall bars (with a 10 μm channel width and a 100 μm channel length). The dc current-voltage characteristics measured at 4.2 K in the common-source configuration is plotted in Fig. 2(a), where the schematic potential profiles along the source-drain direction in three operating regimes are also shown. The conductance is found to be large when there are either 2D electrons or 2D holes in the CQW under the gate area. Both the gate leakage current and the drain current in the depletion region are less than the measurement resolution (0.1 pA).

In order to understand the effect of gating better and to provide the parameters for the design of the SET devices, we have computed numerically the potential profile of InAs QDs. The model structure, as depicted in the left inset of Fig. 2(b), is a standard MOS capacitor, but the gate here is a small metallic cylinder with a diameter (D) less than 100 nm. Details of the numerical simulation are discussed elsewhere.[11] The right inset of Fig. 2(b) shows an example of the simulation, assuming the effective band gap of the CQW being 100 meV and a 2D hole density of 1×10^{12} cm^{-2} in the GaSb layer. We find that for a smaller gate diameter, although it takes a higher gate voltage to induce the first electron, the confinement potential is steeper and the size-quantization energies are larger. For example, when a single electron resides in the QD, the quantization energy is 13, 15, and 17 meV for $D=100$, 75, and 50 nm, respectively. One key operating principle, substantiated through the simulation, is that the band-to-band tunneling barrier is not sensitive to the top gate bias for the first few electrons, as illustrated in Fig. 2(b). The height of the tunneling barrier and its width are primarily dependent on the band gap of CQW and 2D hole density, respectively. In other words, the tunneling transmission coefficient in enhancement-mode QDs is determined by the potential profile of the heterostructure, similar to the depletion-mode vertical QDs.

For the fabrication of SETs, we have used electron-beam lithography and wet etching to fabricate transistors with a gate length down to a few tens of nanometers. Transistors with a channel width of approximately 700 nm show a complete depletion of 2D holes, indicating a surface depletion of 350 nm at the sidewall. Many transistors were characterized, and data taken from one transistor that shows typical results are presented here. The small transistors display the expected Coulomb blockade. Figures 1(c) and 1(d) show the data taken at 4.2 K, where the dc drain current is measured at a fixed drain voltage of 1 mV. At $V_{gate}=0$, the system is in the accumulation regime, and the transistor shows an Ohmic conductance. As the gate voltage increases, the drain current drops because the transistor goes from the accumulation to the depletion regime, where the drain current is zero. When the gate voltage bias is higher (6.2 V) the lowest single electron quantum state beneath the gated region is aligned with the Fermi level, resulting in a current peak. As the gate voltage becomes more positive, the current peaks due to the second and the third electron occupation are observed near $V_{gate}=7.0$ and 8.4 V, respectively.

To investigate the operation of this enhancement-mode InAs SET further, we have carried out the stability measurement: the drain current is measured as a function of a stepping gate voltage and a sweeping drain bias. Figure 3 shows the contour plot of the drain current using a linear scale. In the manifestation of a single-electron transport in the Cou-

TABLE I. The capacitances and the addition energies obtained from the diamonds in Fig 3.

N	1	2	4
C_{gate} (aF)	0.69	0.29	0.37
C_{drain} (aF)	4.7	1.7	5.1
C_{source} (aF)	5.4	2.6	4.4
E (meV)	15	35	16

lomb blockade regime, the contour plot shows a series of diamond-shaped blocks. The solid lines highlight the boundaries of the blocks and are labeled by $N=0$, 1, 2, 3, and 4, referring to the number of electrons in the QD. According to the "orthodox" theory[12] of the Coulomb blockade, the height (e/C_{Σ}), the width (e/C_{gate}), and the slopes defining the diamond (C_{gate}/C_{drain} and C_{gate}/C_{source}) uniquely determine the SET charging energy. Following this standard analysis procedure, we have calculated for the first, the second, and the fourth diamonds their respective capacitances and the addition energies, as listed in Table I. We obtained an addition energy of 15 meV for the first block and 35 meV for the second, indicating that the level spacing due to the size-quantization effect is 20 meV. Comparing to our potential simulation, the obtained quantization energy implies a QD less than 50 nm in diameter. If we model the QD as a disc with a radius r, the obtained capacitance of our QD suggests an effective diameter of about 20 nm. Here, we use $C_{\Sigma}=8\varepsilon r$ and the dielectric constant of InAs $\varepsilon=12.3$. We notice that the third diamond contains several spikes. We attribute them to single electron traps in the vicinity of SET that happen to be activated under specific operating conditions. The size of the third diamond should therefore be smaller than the apparent result shown in Fig. 3.

The observations of relatively large Coulomb and size-quantization energies are significant. The criteria for observing single-electron tunneling characteristics are that the Coulomb energy (e^2/C_{Σ}) should be larger than the thermal energy and that the tunneling conductance should be smaller than the conductance quantum e^2/h. Consequently, SETs in the many-electron regime have been demonstrated in a variety of systems, including $In_xGa_{1-x}As$, GaAs, Si, carbon nanotubes, and metal-based structures. However, the experimental requirement is more stringent for observing the size-quantization effect due to two additional criteria: One is that the Fermi wavelength should be comparable to the island's size; the other is that the system should be in the few-electron regime. Depletion-mode lateral and vertical SETs were the only two systems reported thus far that show size-quantization energies, typically a few meV. A larger quantization energy allows for an SET operation at a higher temperature, as evident from 4 K operating temperature of our SET versus 10–50 mK in depletion-mode SETs.[4–7] It is also important for quantum computing from the vantage point of spin decoherence: the important factor in the decoherence mechanisms is the admixture of electron states due to spin-orbit interactions, and such admixture is reduced as a result of the large orbital level energy spacing, mainly removing the effect of the strong spin-orbit interaction in InAs. Furthermore, other effects related to the admixture of the excited electron levels, including their virtual occupation by other electrons, are also suppressed, making the ground state of the InAs quantum dot closer to an ideal two-level system. The observed large quantization energy is due to a small electron effective mass in InAs and a steep confinement potential resulting from the band-to-band tunneling design. We note that the steep confinement potential also makes it possible to place QDs in proximity which is needed for a stronger exchange coupling between dots and for constructing an array of QDs capable of transporting qubits via the paths of empty QDs.[8]

In conclusion, we have proposed an enhancement-mode SET and demonstrated it using a InAs/GaSb composite QW that effectively gives a QW with a narrow band gap. We achieved the one-electron regime in a 20 nm InAs quantum dot with an orbital energy spacing of 20 meV. Our approach is advantageous for applications in quantum information technology, including lateral configuration, a single top gate design, steep potential confinement, large g^* factor, and straightforward identification of a single electron.

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