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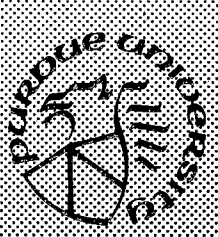

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ABSTRACT

The use of ZnSe on GaAs epilayers (epi) as a pseudo-insulator in field-effect device applications is demonstrated. The passivating ZnSe layers are grown on GaAs(epi) by interrupted growth molecular beam epitaxy (MBE) using two separate MBE machines. A thin layer of amorphous arsenic protects the GaAs(epi) during transfer between the MBE systems. When nucleated on the GaAs(epi), the ZnSe grows layer-by-layer as revealed by the reflection high energy electron diffraction pattern generated in the II-VI MBE growth chamber. A study of intensity oscillations in the electron diffraction pattern is further used to understand the initial growth stages of ZnSe on GaAs(epi).

The material properties of the ZnSe/GaAs(epi) heterostructure are briefly examined. Even though ZnSe and GaAs have a 0.25% lattice mismatch, transmission electron micrographs show that very thin films (1000Å) of ZnSe form a coherent and dislocation free interface with the GaAs(epi). In thicker ZnSe films, strain relieving misfit dislocations are observed. Photoluminescence measurements reveal information about the effect of the lattice mismatch on the energy band structure of the ZnSe. For the 1000Å film, the excitonic features are shifted upwards in energy, and the normally degenerate light and heavy hole valence bands split into two

bands.

As the 1000Å of ZnSe is an appropriate thickness for an insulator in a field-effect device, the ZnSe/GaAs(epi) heterostructure is then used in metal-insulator-semiconductor (MIS) capacitors and transistors. Most prominent, the fabrication of the first depletion-mode field-effect transistors based on the ZnSe/n-GaAs heterointerface are described. The transistors display near ideal characteristics with complete current saturation and cutoff; the channel modulation indicates that the Fermi level is not pinned at the ZnSe/n-GaAs interface. With the success of the depletion-mode transistors, the use of ZnSe and GaAs(epi) in future MIS devices appears promising.

CHAPTER 1
INTRODUCTION

1.1 Material Properties of Zinc Selenide

Zinc selenide (ZnSe) is an important compound semiconductor and has received much scientific interest in recent years because of its significant material properties. Of its many properties, ZnSe is most noted for its relatively large direct energy band gap of 2.7eV. This II-VI compound also possesses direct band-to-band recombination which suggests that efficient ZnSe light emitting devices can be realized. ZnSe is especially important for blue light emitting devices since the near-band-edge emission occurs at 4600Å.

Not only does ZnSe have a large band gap, but it is also closely lattice matched to gallium arsenide (GaAs). (The lattice mismatch is approximately 0.25%.) GaAs is an important III-V compound semiconductor because the mobility of electrons and holes in this material is much higher than in the type IV semiconductors such as silicon and germanium. GaAs, like ZnSe, is also an important optical material with a relatively large direct band gap of 1.45eV. Because ZnSe has a smaller dielectric constant (ϵ_r=8.8) than GaAs (ϵ_r=12.9), ZnSe can be used for optical confinement in GaAs based light emitting devices.

Both zinc selenide and gallium arsenide thin films are deposited by many epitaxial growth techniques including molecular beam epitaxy (MBE) which is the growth process used in this work. Epitaxial growth refers to the formation of one crystalline layer on top of another layer such that there is an oriented relationship between the two films.

Each growth technique has many advantages and disadvantages which can effect the "extrinsic" material properties of the resultant semiconductor layers. For example, ZnSe has been grown in the past by liquid phase epitaxy and chemical vapor deposition which are conducted under equilibrium conditions at high growth temperatures (750 °C-1050 °C) [2]. Typically, the ZnSe layers are grown on GaAs substrates because the lattice

mismatch is so small. Under high growth temperatures, gallium, arsenic, and other impurities from the GaAs substrate tend to diffuse into the ZnSe and unintentionally dope the material. (Gallium is a n-type dopant in ZnSe.) In addition, ZnSe, grown at elevated temperatures, often contains many non-stoichiometric defects such as zinc and selenium vacancies or misplaced zinc and selenium atoms (interstitial). These defects make the doping of ZnSe very difficult because they tend to compensate for dopants that are intentionally incorporated into the film. Essentially, the non-stoichiometric defects cause ZnSe to only have n-type conduction and make the conversion to p-type conduction very difficult [2].

The growth of the II-VI compounds by MBE has been instrumental in improving the material properties of ZnSe. Molecular beam epitaxy of ZnSe involves the reaction of thermal beams of Zn and Se with a crystalline surface (GaAs substrate) under ultrahigh-vacuum conditions. MBE is known for its precise control of beam fluxes and growth conditions. Because of the ultra-high vacuum environment, MBE system's often contain in situ surface analysis equipment that permits the study of the semiconductors during all parts of the epitaxy. One of the important advantages of MBE is that the epitaxy occurs at a relatively low substrate temperature (250 ° C-400 ° C). At these low temperatures, diffusion of gallium, arsenic, and other impurities from the GaAs substrate into the ZnSe is reduced. The low deposition temperature also favors a reduction in zinc and selenium vacancies and interstitial defects [2].

Another important advantage of MBE is that it uses very high purity source material in an ultra-high vacuum environment. Both of these factors aid in the reduction of impurity contamination in ZnSe [2]. For example, the elemental zinc and selenium source materials typically contain less than 1 impurity in 1 million parts. In our laboratory, a multiple distillation technique is used to obtain this type of ultra-pure source material. The elements are housed in a growth chamber where the background pressure can be as low as the 10^{-11}Torr range. Following pump down from atmospheric pressure, the walls of the vacuum chambers are heated in order to evaporate trapped gases and eliminate them from the vacuum. Subsequently, the source materials are heated to very high temperatures before deposition in order to outgas any oxides or surface contamination.

Several laboratories [3] have demonstrated the growth of high quality ZnSe by molecular beam epitaxy. Many parameters can be used to evaluate the quality of the ZnSe films. Because we are interested in using ZnSe as a

"pseudo-insulator" for GaAs, the property of interest in this work is the film resistivity. For GaAs insulating applications, high resistivity undoped ZnSe is essential. As an example, Yoneda et. al [3] have recently grown relatively high resistivity ($\rho = 10^4 \Omega$-cm) ZnSe on (100) GaAs substrates. The high resistivity ZnSe of carrier concentration $7x10^{14}cm^{-3}$ is obtained when the selenium source material is purified nine times by a sublimation process. For no purification of the selenium, the ZnSe contains a carrier concentration of $1x10^{17}cm^{-3}$. Films grown in Purdue's MBE facility using multiple distilled sources have also demonstrated high resistivity of this nature.

In summary, ZnSe is an important compound semiconductor because it: (1) has a relatively large band gap, (2) has efficient, direct band-to-band recombination, (3) is closely lattice matched to GaAs, and (4) has a smaller dielectric constant than GaAs. ZnSe has been grown by many deposition techniques including molecular beam epitaxy. The material properties of ZnSe have been improved by MBE, particularly in the control of impurity contamination and non-stoichiometric defects, because of the low growth temperatures, the pure source material, and the ultra-high vacuum environment. As a result, undoped ZnSe can be grown in a high resistivity form by MBE.

1.2 Applications of "Insulating" ZnSe on GaAs by MBE

One of the most exciting applications of ZnSe on GaAs is the use of ZnSe as a pseudo-insulator in GaAs based devices. Some recent device applications demonstrate this point. A good example is the fabrication of a ZnSe direct current (D.C.) electroluminescence (EL) cell grown on a GaAs substrate by MBE [4]. In the work by Mishima [4], 0.6μm of ZnSe is deposited on a n+ doped (100) GaAs substrate at a growth temperature of 380 °C - 450 °C. The cell structure consists of gold metal on the ZnSe (doped with manganese) on the n+ type GaAs substrate. The n+ GaAs substrate serves as both the starting substrate for the ZnSe epitaxy and also as an ohmic contact for the EL cell.

For small positive voltages, the current in the cell was carried by thermally-excited carriers contained in the ZnSe:Mn layer. This conduction appeared ohmic. Under higher positive voltages (0.1-2V), the current in the ZnSe was nearly proportional to the square of the voltage. According to Mishima [4], this type of voltage dependence is indicative of space charge limited current flow which is observed in insulating films. At even higher voltages, the current increased rapidly and was thought to be caused by

either intertrap tunneling and-or impact ionization. Hence, for a portion of the I-V relationship, the ZnSe appeared to be an insulating layer in the EL cell application. This research was the first investigation that demonstrated the potential of MBE-grown ZnSe as an insulator for GaAs.

Another example of insulating ZnSe is the recent use of ZnSe for current confinement in an aluminum-gallium-arsenide (AlGaAs) laser diode [5]. Aluminum, like gallium, is a column III element and can replace gallium in GaAs forming a ternary compound. A direct band gap of 2.0eV occurs at 50% substitution of Ga with Al. In this laser diode, the AlGaAs is first grown by liquid phase epitaxy (LPE) on a n-type GaAs substrate. After processing the AlGaAs-GaAs layers, the ZnSe is grown by MBE on top to form a cladding layer.

In the work by Niina [5], it was stated that ZnSe films grown under similar MBE conditions demonstrated a resistivity of at least $10^5\Omega$cm. Because of the high resistivity ZnSe, the confinement factor in the laser diode was large enough to negate the influence of leakage currents on the operating characteristics of the device. Also, according to Niina [5], several other insulating layers such as silicon dioxide (SiO_2) and silicon nitride (Si_3N_4) could also be used as the confinement material. ZnSe was preferred, however, for several reasons, most of which were given in section 1.1. Most notably, MBE-grown ZnSe was deposited at relatively low temperatures which preserved the LPE-grown GaAs-AlGaAs structure. Other reasons noted were that ZnSe had a thermal expansion coefficient closer to GaAs than either SiO_2 or Si_3N_4 and that ZnSe had a larger thermal conductivity than either of the other two materials.

Both the previous examples suggest that ZnSe could serve as a passivating insulator in other GaAs based devices such as field-effect transistors (FETs). To date, the use of GaAs has been limited in field-effect device applications because of the lack of a high quality insulator. Researchers have used amorphous materials on GaAs such as native oxides, silicon nitride, aluminum oxide, and silicon dioxide, but these materials have achieved limited success as GaAs insulators [6]. Usually, the interface between the insulators and the GaAs is dominated by a high concentration of unwanted interface traps. The traps cause electrical instability and are difficult to eliminate. Elaborate techniques have been developed to reduce the trap density at the GaAs-insulator interface. One process [7] uses laser light in conjunction with water to reduce the interfacial defect density but

only improves the electrical stability of the interface for a short period of time. Thermal annealing in hydrogen and nitrogen (as is done in the silicon-silicon dioxide material system) has also been attempted [6] but with limited success.

The most successful pseudo-insulating layer for GaAs to date has been aluminum-gallium-arsenide. AlGaAs is MBE compatible and has a larger band gap than GaAs. AlGaAs is widely used as an insulator in both depletion-mode [8,9,10] and enhancement-mode [11] field-effect transistors. However, the AlGaAs/GaAs heterojunction presents a very low interfacial barrier (0.4eV at maximum) to carrier flow from GaAs into the AlGaAs. Having a band gap of 2.7eV, ZnSe could provide an improvement and alternative to AlGaAs as a passivating layer for GaAs in some device applications.

Additional ZnSe properties further suggest that ZnSe is a likely candidate for use as an insulator in GaAs field-effect devices. As previously mentioned, ZnSe can be grown by MBE in a high resistivity form on GaAs. Because of the small lattice mismatch, pseudomorphic ZnSe can form a coherent interface with GaAs, similar in structural quality to the AlGaAs-GaAs interface. As explained in Chapter 3, the coherent interface occurs for very thin ($\simeq$ 1000Å) ZnSe films. One might expect that a coherent semiconductor-semiconductor interface would have less surface states than the incoherent interface formed by an amorphous material deposited onto a semiconductor. In addition, given its dielectric constant, 1000Å of ZnSe is a convenient thickness for an insulator in a metal-insulator-semiconductor (MIS) structure.

The advent of interrupted growth molecular beam epitaxy has provided the first means for using ZnSe as an insulating layer in GaAs based MIS devices. We have recently reported the successful growth of ZnSe on MBE-grown GaAs epilayers [12]. Because GaAs and ZnSe tend to unintentionally dope each other, the different semiconductor layers are grown in two separate MBE machines. In this case, interrupted MBE growth means that the ZnSe epitaxy occurs on a GaAs epilayer (versus a substrate) after the growth of the GaAs is interrupted in the III-V MBE machine. This is in contrast to AlGaAs epitaxy that is continuously grown on GaAs without any interruption in the epitaxy; AlGaAs can be nucleated on GaAs by simply opening the shutter to an aluminum source oven.

For the first time, thin film ZnSe has been deposited on either doped or undoped GaAs epilayers which are the essential structures for both depletion and enhancement mode transistors. The properties of the ZnSe(epi)/GaAs(epi) heterostructure, as revealed by several diagnostic measurements, are much different than for ZnSe grown on a GaAs substrate. It is the purpose of this report to briefly examine these properties and then demonstrate the use of insulating ZnSe on GaAs epilayers in a MIS transistor application [13].

1.3 Interrupted Molecular Beam Epitaxy

The key to fabricating ZnSe on GaAs epilayers utilizing two separate MBE systems, is the preservation of the GaAs surface after the interruption of the III-V MBE growth. When the molecular beam epitaxy of GaAs is interrupted the surface becomes contaminated with undesirable impurities. The surface impurities act as negatively charged centers and cause electrons to be depleted from the surface [14]. For example, Kawai [14] has demonstrated that n-type GaAs samples doped $2x10^{16}cm^{-3}/1.2x10^{17}cm^{-3}$ have a depletion region of 300/135Å, respectively when the MBE growth is interrupted and the as-grown GaAs is exposed to dry nitrogen at room pressure. The amount of charge that is depleted from the surface is approximately $2x10^{11}cm^{-2}$. When GaAs is again grown on top of the contaminated surface, the negatively charged centers tend to diffuse outwards into the second epitaxial layer.

The negatively charged centers are a source of unwanted traps that cause the Fermi level at the GaAs interface to be fixed at a particular surface potential. This phenomenon, known as Fermi level "pinning", limits the amount of band bending that can occur in the underlying semiconductor. For example, when a metal is placed on a contaminated GaAs surface, the Fermi level is usually restricted to between 0.4-0.8 eV above the valence band [15]. Charge placed on the gate is not entirely imaged by dopants in the GaAs but rather by the filling and emptying of the traps. Hence, the surface contamination taking place at interrupted growth interfaces is a serious problem for GaAs devices involving the electrical stability of the interface.

To attempt to minimize surface contamination, GaAs passivation schemes have recently been developed. One of the most successful protection methods uses layers of amorphous arsenic (As) as passivation for GaAs. The thin amorphous arsenic protects the GaAs while the film is being

processed outside the MBE vacuum. In our case, the amorphous As acts to protect the GaAs during the transfer between MBE machines. First conceived by Kowalczyk et. al [16], As passivation is a relatively simple technique for protecting GaAs, AlGaAs, and AlAs surfaces.

In Kowalczyk's experiments, the overlayer of amorphous arsenic was deposited at the end of the GaAs growth by closing the Ga shutter with the arsenic flux still present. Because As was not adsorbed at the MBE GaAs growth temperatures (580-650 ° C), the sample was cooled to room temperature. To expedite the cooling process, the sample holder was placed in intimate contact with the MBE system's liquid nitrogen shroud. Approximately 100-1000Å of As was formed by the time the substrate temperature was 25 ° C [16]. The sample was then transferred from the MBE system through air to a vacuum chamber containing an x-ray photoelectron spectrometer (XPS) for studying the constituents of the surface. The amorphous arsenic layer was then desorbed by heating the sample to 300-350 ° C. After arsenic desorption, the GaAs epilayer surface, as characterized by XPS, showed no carbon, oxygen or other contaminants, which indicated that the arsenic layer successfully protected the GaAs surface.

Further studies by Miller [17] showed that GaAs surfaces protected by amorphous arsenic had less carrier depletion and fewer contaminants than unprotected GaAs films. Miller used secondary-ion-mass-spectroscopy (SIMS) and capacitance-voltage profiling as diagnostic tools. An unprotected and etched sample contained a $3x10^{11}$ cm^{-2} surface depletion and contamination from carbon, oxygen, and other elements. The As protected films showed virtually no carbon or oxygen peaks in profiles by SIMS and less than $5x10^{9}cm^{-2}$ charge depletion for vacuum and air exposure. Only exposure to water caused appreciable carrier depletion of $2.5x10^{10}cm^{-2}$ which was still less than the unprotected surface.

Interrupted molecular beam epitaxy is emerging as an important field of research in semiconductor devices. Extensive work at Purdue [18] has been involved in using advanced MBE techniques combined with arsenic passivation in the production of new novel GaAs based transistors. As the properties of semiconductor layers become more understood, the use of two or more layers together in device applications is becoming attractive. Interrupted MBE and passivation of semiconductor surfaces make these applications feasible.

This report details the use of interrupted MBE growth with arsenic passivation in the fabrication of ZnSe/GaAs(epi) heterostructures which are to be used in MIS devices. Most prominent, a prototype ZnSe/n-GaAs doped channel field-effect transistor is described. The emphasis of this work has been in the growth, fabrication, and characterization of the transistor structure.

The second chapter describes the MBE growth of both material systems. The description includes substrate preparation, GaAs deposition, arsenic passivation, arsenic desorption, and finally ZnSe epitaxy. The third chapter describes the properties of the ZnSe/GaAs (epi) heterostructure. It is only a brief exposition and is not meant to be a thorough evaluation of the material properties. Reflection high energy electron diffraction (RHEED) is used to compare the nucleation behavior of ZnSe on GaAs epilayers versus nucleation on GaAs substrates. Transmission electron microscopy (TEM) is then used to demonstrate that the 1000Å ZnSe/GaAs interface is coherent. Photoluminescence (PL) studies reveal the effects of the lattice mismatch between the ZnSe and the GaAs on the energy band structure of the ZnSe.

Chapters four and five involve the fabrication and characterization of the doped-channel field-effect transistor. After detailing the fabrication process in chapter four, chapter five examines the electrical characteristics of MIS-capacitors and the metal-insulator-semiconductor field-effect transistors (MISFETs). The analysis of the transistor is divided into three sections: a study of (i) long channel devices, (ii) short channel devices, and (iii) the gate region.

Chapter six summarizes both the material properties and the electrical properties of the heterostructure and offers suggestions for new devices based on the ZnSe/GaAs(epi) material system. Two appendices follow the last chapter. Appendix A is a listing of the fabrication steps for the doped channel transistor and appendix B is a derivation of the transistor equations.

CHAPTER 2
MBE OF MIS HETEROSTRUCTURES

The following chapter describes the interrupted molecular beam epitaxy of ZnSe on GaAs epilayers. Because every layer of the ZnSe/GaAs heterostructure is relevant to the successful performance of the MIS device, the entire growth process is described. The GaAs substrate preparation and epitaxy is performed by M. Melloch. Before the growth is described, a brief description of the MBE systems is given.

2.1 MBE System Description

The molecular beam epitaxy systems in this work are first generation machines having small oven and wafer capacities. Because of their age, the MBE systems are well understood and have produced many high quality semiconductor films. The interrupted growth of the MIS heterostructures is performed in two separate Perkin Elmer model 400 MBE systems. Figure 2.1 is a schematic drawing of the ultra-high vacuum MBE system. The II-VI and III-V MBE systems are similar in design and operation but differ primarily in the material content of each machine. The three vacuum chambers are named after their respective functions and are the introduction, analysis and growth chambers. Each chamber contains its own pumping system.

The introduction chamber houses the sample holder and probe arm. A turbo-molecular pump maintains a background pressure of $1x10^{-4}$ Torr and is connected to the chamber by a butterfly valve which allows the chamber to be easily raised to room pressure. Attached to the end of the probe arm is the sample holder that contains a "pancake" heater for thermal heating of the semiconductor up to 700 ° C. The sample holder can be rotated by 360 ° and tilted by 90 ° through its axis. The transport probe is surrounded by a bellows that collapses as the probe arm moves throughout the various chambers. Because the introduction chamber supports a relatively weak vacuum, isolation is required between the introduction and other chambers.

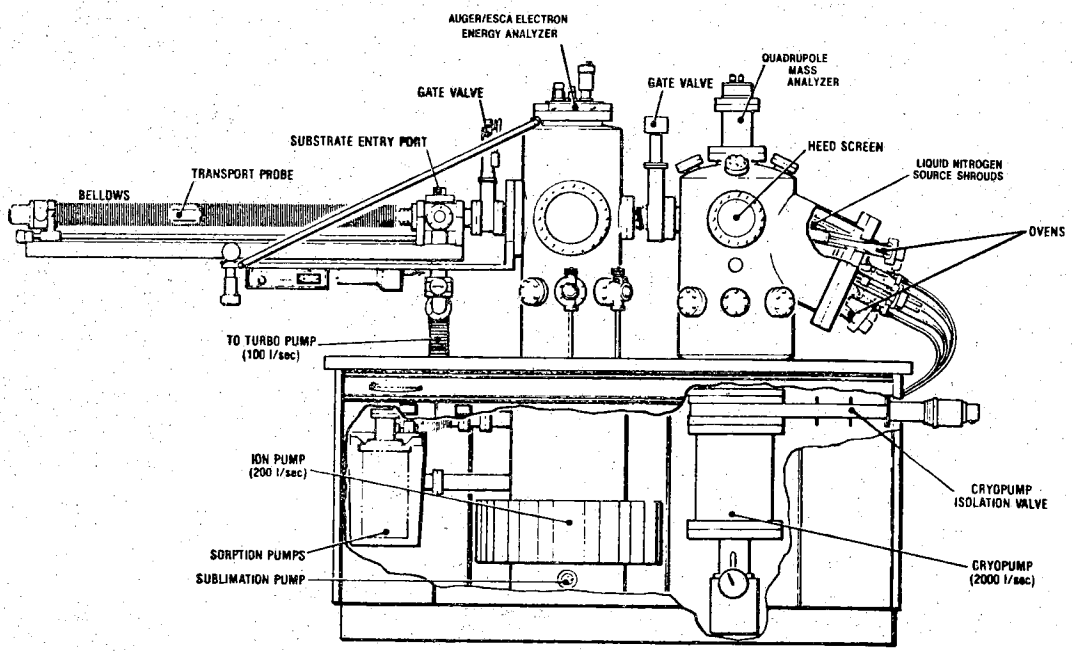


Figure 2.1. Schematic diagram of the Perkin Elmer Model 400 Molecular Beam Epitaxy Machine.

The transport arm slides through a teflon o-ring that isolates the two chambers when the arm is in the ultra-high vacuum. When the arm is fully withdrawn from the system, the chambers are isolated by a pneumatic gate valve.

The starting semiconductor wafer, typically a (100) GaAs substrate, is mounted on a molybdenum (Mo) block by indium solder. Although the indium is molten above 130 °C, the GaAs wafer is held to the Mo block by surface tension. The Mo block is attached to the sample holder with two high purity stainless steel screws. Located at the back of the Mo block in the center of the sample holder is a thermocouple that is used to monitor the temperature of the GaAs substrate. Good thermal contact between the thermocouple and Mo block is very important in order to accurately determine the substrate temperature and is checked by electrical conductivity before each growth.

Both the analysis and growth chambers comprise the ultra-high vacuum portion of the MBE system and maintain a room temperature base pressure of $1x10^{-10}$ Torr. As Fig. 2.1 indicates, the analysis chamber is pumped by a 200 liter/sec ion pump, and the growth chamber is pumped by a 2000 liter/sec closed-cycle helium cryopump. The pressure in each chamber is monitored with nude ion gauges.

The analysis chamber contains several in situ diagnostic tools for evaluating the composition and quality of the semiconductor surface. For example, in the MIS work, the arsenic is desorbed (evaporated) from the GaAs epilayers in the analysis chamber while monitoring the surface with Auger electron spectroscopy (AES). While not used in this research, the analysis chamber also contains an x-ray excitation source for electron spectroscopy for chemical analysis (ESCA) of the surface and an ion sputtering gun for etching the semiconductor surface.

Auger electron spectroscopy is a surface diagnostic measurement that reveals the atomic makeup of a semiconductor surface. Medium energy electrons are directed at the GaAs substrate and cause Auger electrons to be emitted from the atoms near the surface of the semiconductor (within the top 30Å). The Auger electrons are collected by a cylindrical mirror analyzer at the top of the chamber. Each collected electron has an energy which is dependent on the source atom. Hence, an AES plot indicates the constituents of the surface of the semiconductor. AES scans are used in this work to verify the presence of the arsenic passivation layer, to check when

the arsenic layer has been desorbed, and to look for impurities such as oxygen, carbon, and indium on both the GaAs and ZnSe surfaces.

As its name implies, the material deposition takes place in the growth chamber. Like the analysis chamber, the growth chamber contains several in situ diagnostic tools, such as reflection high energy electron diffraction (RHEED) and a quadrapole mass analyzer. The mass analyzer is used in determining the background impurities in the ultra-high vacuum while RHEED, as explained in Chap. 3, is used to evaluate the crystal structure and quality of the growing compound semiconductor. A quartz crystal monitor in the II-VI machine is situated opposite the source ovens near the growth position of the sample and is used to determine the molecular beam fluxes. Also, near the growth position in both machines is a liquid nitrogen shroud for absorbing the excess beam flux and residual background impurities. When the shroud is cold, the pressure in the growth chamber is typically $5x10^{-11}$ Torr.

The source materials are evaporated from effusion ovens, and up to eight different elements or compounds can be evaporated. The material is housed in boron nitride crucibles of two different sizes, 2cc and 20cc. The source material is heated by passing electric current through heater wire that is wrapped around the crucibles. The elements evaporate without melting and form a molecular beam. A thermocouple, in conjunction with a proportional-integral-derivative feedback controller, keeps the oven temperatures (180-1000 °C) at +/- 1 °C of the desired set point. To minimize cross contamination and heating from different ovens, each oven is surrounded by a second liquid nitrogen shroud.

Each source oven has an air actuated shutter over the mouth of the oven that regulates the molecular flux. The shutters allow fluxes to be switched on and off very quickly. In conjunction with the low growth rate, the shutters help realize the growth of ultra-thin semiconductor layers as thin as several monolayers. The same temperature controller can also be used to automatically open and close the source shutters. The ability to control the beam fluxes is one of the many advantages that MBE has over other epitaxial growth systems.

2.2 III-V Epitaxy

The MIS heterostructures consist of ZnSe deposited on different doped or undoped layers of GaAs. Table 1 shows the twelve films grown to date

Table 1. Structure of the 12 MIS samples grown to date. The starting substrates have (100) orientation. The ZnSe is 1000Å thick except for the first film which is 1.3μm thick. (n:n-type, p:p-type, SI:semi-insulating), CV:current-voltage of a MIS capacitor, EM: enhancement-mode transistor, DM:depletion-mode transistor, and SC:solar cell.

No.	Sub	Epi	Doping(cm^{-3})	(μm)	Appl.
1	n+	SI		5.0	
2	n	n	1.0e17	2.10	CV
3	p+	p	1.5e17	1.56	CV
4	n	n	1.0e17	2.10	CV
5	n	n	1.0e17	1.30	CV
6	SI	SI		1.67	EM
7	SI	n	1.5e16	0.40	DM
		SI		1.00	
8	SI	SI		1.37	EM
9	SI	n	3.0e17	0.14	DM
		SI		1.20	
10	SI	SI		1.25	EM
11	n+	p	3.0e18	0.40	SC
		n-	2.0e17	2.00	
		n+	8.0e17	0.50	
12	SI	n	3.0e17	0.10	DM
		SI		1.00	

indicating their structure and electrical device application. The first MIS heterostructure was a 1.3μm ZnSe film grown on undoped GaAs. Films 2 through 5 were 1000Å ZnSe on doped epitaxial layers of GaAs for use in MIS capacitor studies. The next six structures were grown on semi-insulating GaAs substrates for use in transistor devices. Films 7,9, and 12 were doped channel MISFETS and 6,8 and 10 were designed for enhancement-mode transistors. Because of various problems that developed in both epitaxial systems, film 7 was the only successful depletion-mode transistor, and its fabrication and characterization are reported in chapters 4 and 5. Film 11 was a solar cell consisting of a GaAs p-n junction.

The GaAs epitaxy consists of four sequences: (1) sample preparation, (2) oxygen desorption, (3) GaAs deposition, and (4) arsenic passivation. The interrupted MBE growth, beginning with wafer preparation, is performed in one day in order to minimize contamination.

2.2.1 Sample Preparation

The first, and most important step in the MBE growth of MIS structures, is the preparation of the GaAs substrate. The sample preparation has been given elsewhere in detail [19] but is repeated here for sake of clarity. The three main steps in the GaAs substrate preparation are (i) degrease of the tools and sample, (ii) etching of approximately 10μm of GaAs, and (iii) mounting of the substrate on the Mo block with indium.

To begin, both the glassware and stainless steel utensils used in other parts of the sample preparation are cleaned. The metal tools are cleaned with a three part degrease outlined in Table 2. The degrease removes hydrocarbons and other organic materials that are extremely difficult to pump in an ultra-high vacuum. The degrease consists of boiling in trichlorcethane and subsequent ultrasonic cleaning in acetone and methanol. The glassware and teflon articles are purified using an aqua-regia chemical etch. Aqua regia consists of 3:1 HCL to HNO_3 and is orange and bubbly when properly mixed.

Along with the stainless steel wares, the GaAs substrate is also degreased. Both Sumitomo and Ma-Com GaAs substrates are used in this work. After cleaving the wafer, 10mm x 20mm x 450μm, the substrate is degreased using the same procedure outlined in Table 2. Following the methanol cleaning, the sample is rinsed in deionized water (D.I. H_2O) and dryed with nitrogen gas. The sample is now ready to be etched.

Table 2. Degrease procedure for both stainless steel ware and GaAs substrates.

TIME (min.)	SOLVENT	AGITATION
5	TCA	Boiling
5	TCA	Boiling
10	ACE	Ultrasonic
10	METH	Ultrasonic
5	H_2O	Rinse

Approximately 10μm of GaAs material is removed with a 80 second dip in 60 ° C 5:1:1 H_2SO_4 : H_2O_2 : H_2O. The GaAs sample is then rinsed for several minutes in D.I. H_2O. While in the H_2O, a thin layer of oxide is grown on the freshly etched GaAs. Consisting of As_2O_5 and Ga_2O_3, the oxides protect the GaAs surface during mounting and subsequent exposure to room air.

To complete the sample preparation, the GaAs substrate is dryed and mounted on the Mo block with indium. The back side of the wafer is wet by moving the substrate back and forth in the molten indium. After the wafer adheres to the Mo block, the sample is cooled, and the excess indium is removed from the block with a blade. Because of its low vapor pressure, very little indium evaporates during the film deposition.

2.2.2 Oxide Desorption and GaAs Epitaxy

Immediately following the substrate preparation, the Mo block is mounted on the sample holder with the metal screws and the thermocouple is electrically checked to see if it is making good contact to the Mo block. The introduction chamber is then pumped to at least $1x10^{-4}$ Torr.

The GaAs wafer is first transported to the analysis chamber for initial thermal cleaning and characterization of the substrate surface. The wafer is heated to at least 350 ° C in order to drive off water vapor. Even though the GaAs is protected by a thin oxide layer, carbon can sometimes be adsorbed onto the substrate surface. The carbon can be evaporated with the oxide if it is loosely bonded to the GaAs substrate. Chang [20] has shown that adsorbed carbon is weakly bonded at first to the substrate but that exposure to the AES electron beam strengthens the atomic bond if the substrate temperature is below 350 ° C. Therefore, the substrate is analyzed by AES only after the temperature reaches 350 ° C. Typically, an AES scan of the GaAs surface at this point displays large oxygen, gallium, and arsenic peaks. Figure 2.2 is a representative AES plot of a GaAs substrate before the oxygen has been desorbed. The scan indicates the presence of oxygen, gallium and arsenic and are appropriately labeled. To the left of the oxygen peak appears a very small deflection at an electron energy of 272eV, the energy for carbon contamination. The carbon peak is labeled with a small letter c (the blip to the right of the carbon is noise).

Before the sample enters the growth chamber, the source ovens are heated to the appropriate growth temperature. The source ovens used in

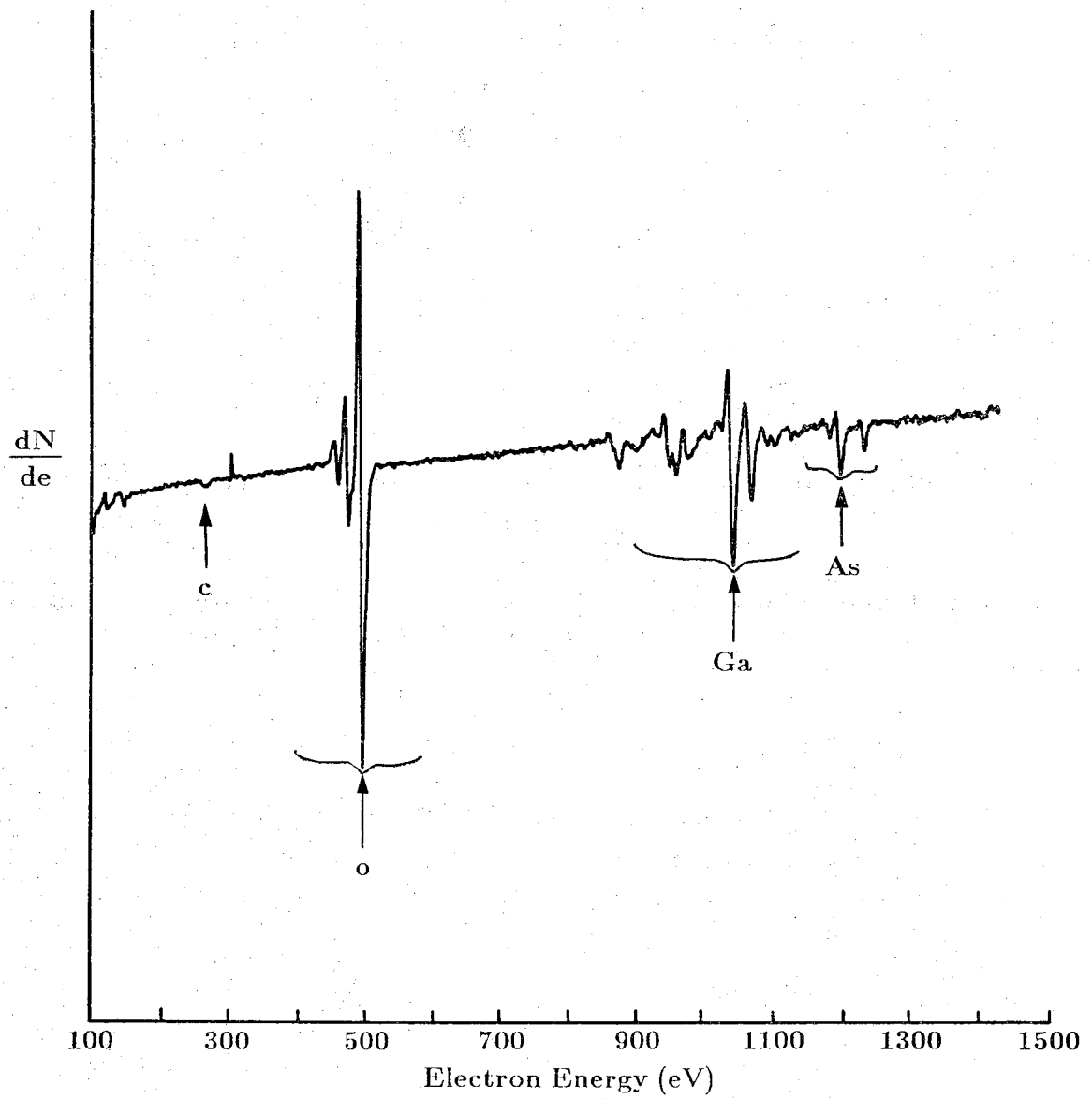


Figure 2.2. An AES scan of a GaAs substrate at 350 ° C prior to oxygen desorption. A small carbon peak is also present.

the III-V deposition are a 20cc gallium, a 200cc arsenic cracker, a 2cc silicon (n-type dopant), and a 2cc beryllium (p-type dopant). The arsenic source oven is termed a cracker because the molecular arsenic flux originating from it consists of As_2 which has been separated or "cracked" from As_4. As_2 bonds to the Ga atoms more efficiently than the tetramer of arsenic.

Once the state of the GaAs surface has been assessed, the GaAs sample is moved to the growth chamber in an overpressure of arsenic. The RHEED image of the crystal is now used to monitor the desorption of the thin oxide layer. (See section 3.3 for a discussion of RHEED) The substrate temperature is raised very quickly towards 580 ° C where the Ga_2O_3 is known to desorb. As_2O_5 comes off well below 580 ° C and is therefore not a consideration at these temperatures. The initial diffraction pattern due to the amorphous oxide appears as a halo with no definite lines or spots. As the oxide comes off, diffraction streaks appear and eventually dominate the pattern. At this point, the substrate temperature is raised by 10-20 ° C to ensure that the growth temperature will be over 580 ° C. GaAs can be efficiently grown from 580-650 ° C.

As soon as the substrate temperature stabilizes, taking about 2 minutes, the gallium shutter is opened, initiating the growth of the GaAs. At this point, the RHEED pattern appears spotty and dim but soon brightens into streaks as monolayers of GaAs are deposited. Usually, reconstruction lines will be seen between the main order diffraction streaks. A 2 x 4 As stabilized surface reconstruction is often observed and preferred for maximum crystal stoichiometry. The typical growth rate for the GaAs is 0.7μm per hour and has been confirmed from RHEED intensity oscillations. The calibration of the growth rate from the intensity oscillations will be discussed in the next chapter.

2.2.3 Arsenic Passivation

Upon completion of the growth of the GaAs layers in the III-V system, the surface is passivated with amorphous arsenic. The GaAs growth is terminated by closing the Ga shutter with the As left open. The sample is now cooled to room temperature. As the substrate temperature is reduced, the arsenic begins to adsorb to the GaAs surface and the RHEED pattern becomes less streaky and more diffuse. At around 100 ° C, the diffraction streaks disappear completely leaving behind a dim halo-like pattern. The sample is cooled to slightly below room temperature 20-25 ° C requiring

approximately 25-30 minutes.

To expedite the cooling process, the sample block can be placed in intimate contact with the MBE system's liquid nitrogen shroud. After closing the Ga shutter, the probe arm is withdrawn by approximately 2cm and tilted by 20-30 ° until it rests on the shroud. It has been shown experimentally that contact with the shroud is not necessary for rapid cooling of the sample. By simply moving the sample holder within the vicinity of the liquid nitrogen shroud, a cooling time of 30 minutes is achieved. It has not, however, been established that the sample must be cooled to room temperature for a sufficiently thick arsenic layer to be deposited. The samples in this work are processed according to Kowalczyk's [16] research where the substrate is cooled to below room temperature. As in Kowalczyk's work, the thickness of the amorphous arsenic layer is suspected to be between 100-1000Å depending on the flux of arsenic and the rate at which the substrate is cooled.

Once the sample reaches 20-25 ° C, the arsenic deposition is terminated and the sample is moved to the analysis chamber. AES of the wafer reveals only an As peak, confirming the presence of the passivating layer. The sample is then withdrawn to the intro chamber. To complete the III-V work, the Mo block with sample is transferred through air to the introduction chamber of the II-VI machine. The sample is quickly mounted with screws and the chamber is pumped to $1x10^{-4}$ Torr. The sample is now ready for the II-VI epitaxy.

2.3 II-VI Epitaxy

The II-VI growth sequence consists of two parts, desorbing the arsenic layer and subsequent epitaxy of the ZnSe. In order to eliminate variables in interpreting device and material characteristics, the ZnSe growth is virtually the same for all but one film. (In film ZOOEG320-5, the sample was not heated above the ZnSe growth temperature after the arsenic layer was desorbed. As pointed out in this section, this was not the case for the other films which were all heated to at least 500 ° C.)

2.3.1 Arsenic Desorption

The first step in preparing the sample for ZnSe epitaxy is thermal cleaning in the analysis chamber. After moving the sample to the AES position, the sample is heated to 200 ° C for 15 minutes in order to evaporate

water vapor. Because the arsenic begins to desorb from the amorphous layer at 270 ° C, an AES scan of the surface is taken at a substrate temperature (Tsub) of 250 ° C. A representative AES plot of the amorphous As layer of ZOOEG320-7 appears in Figure 2.3. Notice in the scan the presence of an arsenic peak but no gallium peak, confirming the presence of the passivating layer. Also note there is no detected oxygen at this point in the structure.

After confirming the presence of the passivating layer of arsenic, the amorphous arsenic is desorbed while monitoring with AES. An AES scan of 800-1300eV permits observation of both the main Ga peak (1070eV) and the main As peak (1228eV). Tsub is increased in steps of 10 ° C every five min. starting at 250 ° C. Around Tsub of 270 ° C, the pressure in the analysis chamber (P_A) increases to the mid 10^{-9} Torr range. Arsenic is believed to be desorbing from the GaAs surface at this temperature but at a very slow rate. Until the gallium peak appears in the AES scan, Tsub is continually raised in intervals of 10 ° C. The gallium peak typically appears around 300-310 ° C with P_A in the low 10^{-7} Torr range. Once the gallium peak is present, the sample is heated at 300-310 ° C for 2 minutes to ensure that the arsenic desorbs completely over the entire wafer.

Tsub is now reduced to 250 ° C and another AES scan is taken. Figure 2.4 depicts the preserved GaAs surface after arsenic desorption for ZOOEG320-7. Notice at this point a small oxygen peak at 503eV. Because oxygen at the GaAs interface can lead to undesirable surface states that cause Fermi level pinning [6], the oxide is desorbed by thermal heating. The oxide desorption is monitored with AES similar to the procedure for desorbing the oxide from the starting GaAs substrate. Preceding the disappearance of the AES oxygen peak, the analysis chamber pressure rises to the 10^{-8} Torr range and then quickly falls to the mid 10^{-9} Torr range. To completely desorb the oxide over the entire wafer, the sample is heated at 500-510 ° C for 2 minutes. Tsub is then lowered and the sample is moved into the growth chamber.

The presence of the oxygen at the GaAs epilayer surface might suggest that the arsenic layer is not protecting the GaAs surface during the transfer between MBE systems. However, it has been experimentally determined that the oxygen is most likely introduced before the sample is removed from the III-V system. (A GaAs epilayer was passivated with arsenic and then desorbed without removing the wafer from the III-V system; in this case

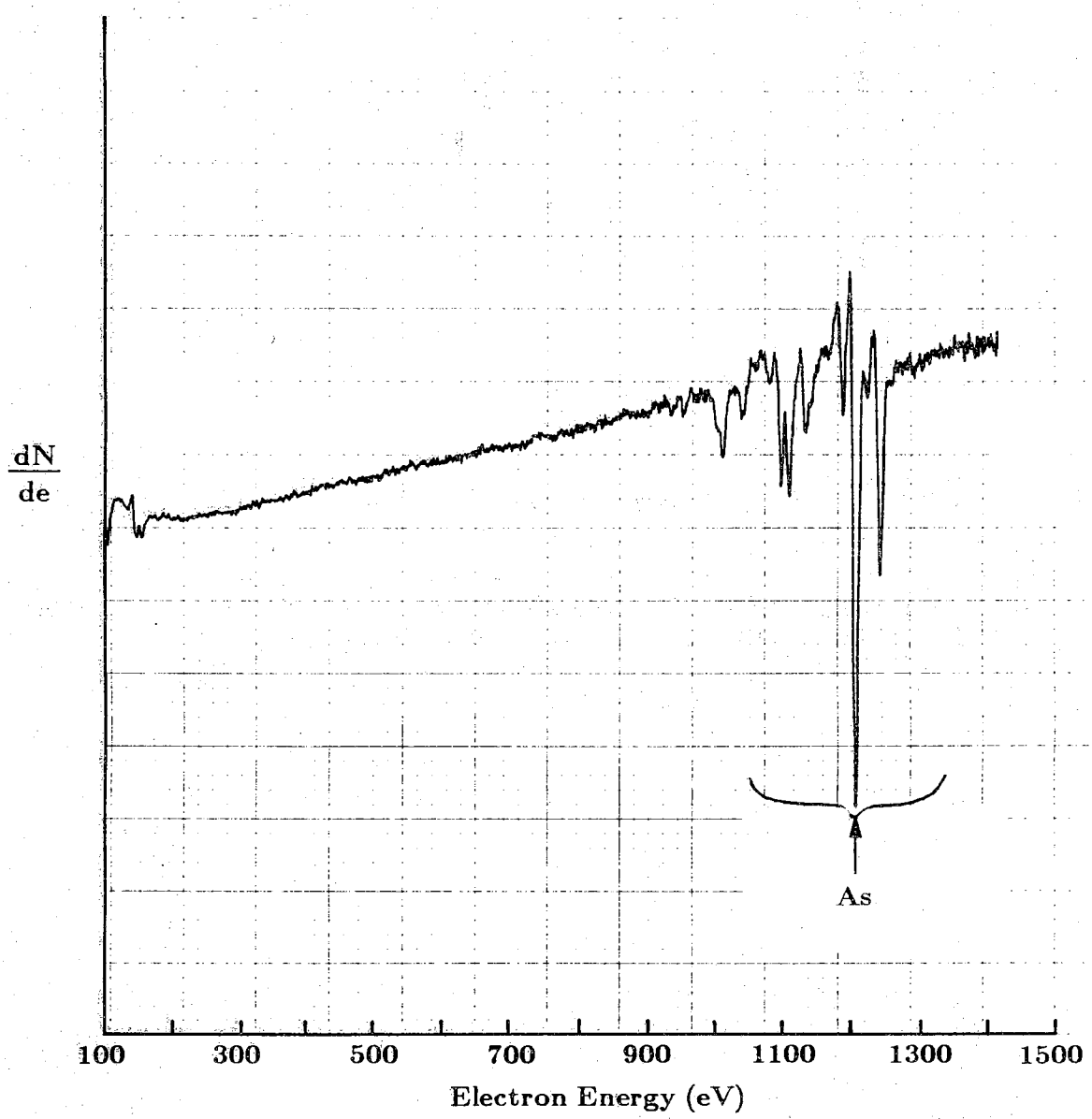


Figure 2.3. An AES scan of the arsenic passivated GaAs epilayer after the transfer from the III-V MBE machine. The scan is taken at 250 ° C and shows no gallium, oxygen, or carbon.

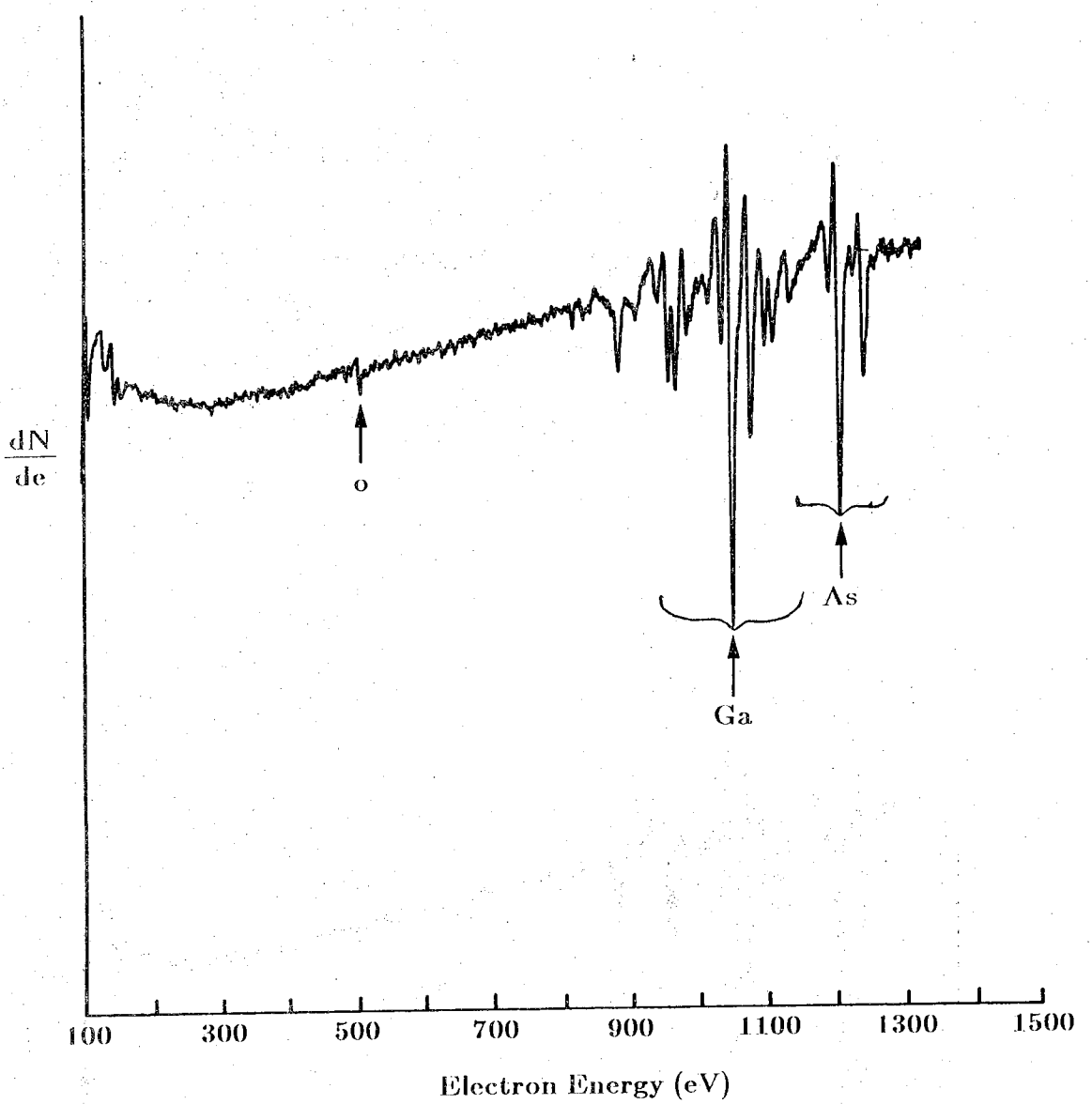


Figure 2.4. The AES scan of the GaAs epilayer after the arsenic layer is desorbed displaying a small amount of oxygen.

oxygen was still observed on the surface of the GaAs.) The oxygen is believed to enter through leaky shutter mechanisms in the III-V MBE system and adheres to the GaAs following the termination of the growth and prior to the formation of the arsenic overlayer. After repair of the leaks in the III-V machine and as the oxygen is gettered during repeated use of the machine, the size of the AES oxygen peak decreases. However, in the manner used in this work, AES does not give reliable quantitative information on surface species but only confirms the presence of a contaminant. Even if no oxygen peak appears on AES, there may be enough contamination to damage the interface electrically.

2.3.2 ZnSe Growth Parameters and Epitaxy

The 20cc selenium and 20cc zinc source ovens are heated to the deposition temperatures before the sample enters the vacuum system. Typically, the Se is heated to 180 - 185 ° C while the Zn is heated to 300 - 305 ° C. At these respective temperatures, a beam flux of 3.0×10^{14} atoms/cm^{2}sec is measured by a quartz crystal monitor which is located near the growth position. The resonant frequency of the quartz crystal decreases as material deposits on the crystal. By calculating the rate at which the resonant frequency decreases with respect to the rate at which material is deposited on the crystal, the molecular fluxes can be determined. The molecular fluxes are related to the rate of change of the resonant frequency of the quartz crystal by two constants, 1.17×10^{14}atoms/cm^{2}Hz for Zn and 9.71×10^{13}atoms/cm^{2}Hz for Se. The Zn and Se molecular fluxes are both set at 3.0×10^{14} atoms/cm^{2}sec in order to give a Se-to-Zn flux ratio at the substrate of approximately one. At unity flux and a substrate temperature of 320 ° C, the ZnSe grows at approximately 1Å/sec.

The ZnSe growth parameters are chosen based on successful film growth at Purdue [12] and at other laboratories (Yoneda) [3]. Using these growth parameters, high resistivity films have been grown at both laboratories. As emphasized in Chapter one, high resistivity ZnSe is essential for insulating applications. In the work by Yoneda [3], the ZnSe of resistivity $10^4 \Omega$cm was grown at a GaAs substrate temperature of 320 ° C and a Se-to-Zn flux ratio of two. Yoneda attributed the high resistivity of the ZnSe to the use of multiple distilled selenium source material. Research at Purdue agrees with this result. In our laboratory, both the zinc and selenium source material are purified by multiple distillation. Thin film, undoped ZnSe (2μm) grown with distilled source material at a flux ratio of one and temperature of

320 ° C has demonstrated a resistivity at least greater than $10^4\Omega$cm. Work by Yao has produced low resistivity (1Ωcm) undoped ZnSe grown at 320 ° C and unity beam flux [2]. We believe that in Yao's work low resistivity ZnSe is obtained because of the purity of the starting source materials and not because of the growth conditions.

The early stages of the ZnSe deposition is monitored by RHEED and is fully discussed in Chapter 3. The substrate is heated to 320 ° C before nucleation. Because the arsenic overlayer desorbs around the expected value of 270 ° C, the sample thermocouple is considered somewhat calibrated at 320 ° C. Once the sample is at the growth temperature, the ZnSe growth is initiated by opening the Zn and Se source shutters. Because the growth rate is 1Å/sec, the film is deposited for 1000 seconds. The growth chamber pressure is typically 7.3 - 7.5 $x10^{-9}$ Torr during the ZnSe epitaxy. The growth is terminated by closing the Zn and Se shutters, and the sample is moved unheated to the analysis chamber.

A final AES plot of the ZnSe at Tsub=250 ° C, Figure 2.5, shows both Zn and a Se peaks. The impinging electrons result in observable bright blue cathodeluminescence from the ZnSe. No oxygen or carbon are seen in the final AES scan. The MIS structure is now complete and the film is moved to the introduction chamber for removal from the system.

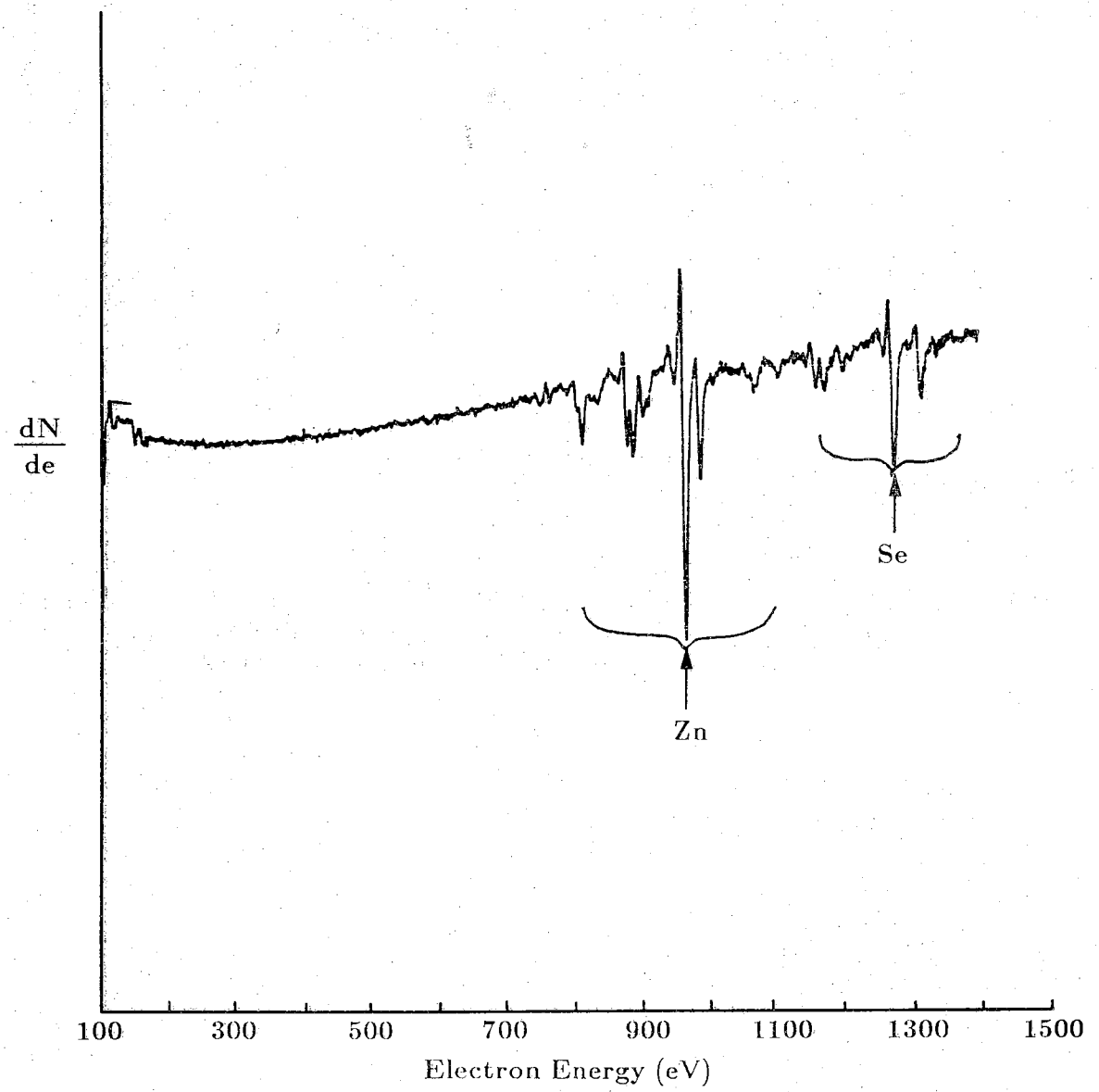


Figure 2.5. The final AES plot showing the presence of Zn and Se peaks, confirming the growth of ZnSe on the GaAs epilayer. No carbon or oxygen are detected.

CHAPTER 3
MATERIAL CHARACTERIZATION

3.1 Nucleation Studies by RHEED

The early stages of ZnSe growth on GaAs epilayers has been studied using reflection high energy electron diffraction (RHEED). RHEED is an excellent in situ diagnostic tool because it can be used to monitor the epitaxy without disturbing the film growth. RHEED is performed by impinging a medium energy electron beam (10KV) onto the semiconductor surface with a glancing angle of 1-2°, as illustrated in Figure 3.1. The diffracted electrons illuminate a phosphor coated screen on the inside wall of the growth chamber forming a diffraction pattern which can be observed exterior to the vacuum. In this work, we are primarily concerned with two different patterns that are typically seen on the screen, streaks and spots. Reflection electron diffraction from planar, smooth surfaces produces a streaked diffraction pattern, while diffraction from rough, non-planar surfaces results in circular spots [21]. By observing the diffraction pattern and its evolution with time, the nature of the ZnSe nucleation on the GaAs surface is determined.

The evolution of the RHEED pattern during nucleation of ZnSe on MBE GaAs epilayers contradicts what is typically observed by various research groups [22,23,24] using bulk GaAs substrates. In most II-VI epitaxy, ZnSe is nucleated on GaAs substrates that are thermally cleaned at 580-600 °C to desorb the GaAs oxides. Without an overpressure of As, this type of thermal cleaning results in the loss of arsenic from the surface creating a transition structure between an As-stabilized and a Ga-stabilized surface. A Ga-rich surface will result for excessive high temperature heating of the GaAs substrate. When ZnSe is nucleated on these various surfaces, the RHEED pattern becomes very spotty for several minutes. The appearance of the diffraction spots suggests that the initial ZnSe surface is rough, consisting of islands of ZnSe that have been nucleated by a three dimensional growth mechanism. As the ZnSe islands coalesce forming a

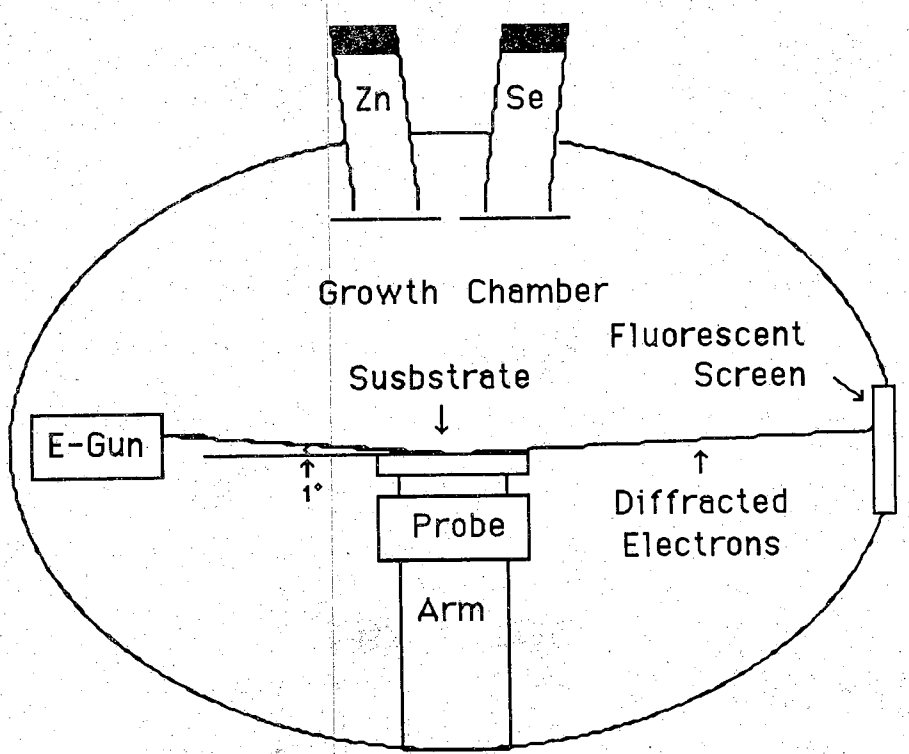


Figure 3.1. Schematic diagram of the RHEED setup in the growth chamber of the MBE. The impinging electrons with a glancing angle of 1-2° are diffracted from the semiconductor and terminate on a fluorescent screen resulting in a diffraction pattern that can be monitored during the film growth.

smoother growth front, the diffraction streaks will again appear. To summarize, ZnSe that is nucleated on GaAs substrates nucleates three dimensionally, causing the RHEED pattern to consist of fuzzy spots for several minutes into the epitaxy.

The evolution of the RHEED pattern for ZnSe nucleated on a GaAs epilayer (ZOOEG320-2) appears in Figure 3.2. The beginning diffraction pattern of the GaAs epilayer surface in a [110] azimuth, Fig. 3.2(a), shows bright integral order diffraction streaks. Often, the diffraction pattern of the GaAs epilayers is brighter and more distinct than that of a GaAs substrate. Upon nucleation of the ZnSe, the pattern dims briefly but quickly returns to streaks with very little spottiness. The observation of the strongly streaked RHEED pattern and the early presence of reconstruction lines ($\simeq$ 9sec.) suggest a more two dimensional (2D) ZnSe growth mechanism [12]. In the case of two dimensional growth, the ZnSe essentially completes one layer of atoms before the next layer of atoms becomes incorporated. The surface front of the ZnSe nucleated on the GaAs(epi) is atomically smooth, unlike the nucleation of ZnSe on the GaAs substrate where the surface is rough because of the initial island formation.

Nucleation studies by Tamargo [25] have recently observed both two-dimensional and three-dimensional nucleation of ZnSe on GaAs. In this work, ZnSe was deposited on four types of GaAs surfaces; Ga-rich GaAs substrates and epilayers and As-rich GaAs substrates and epilayers. The films were grown in a modular MBE system where multiple growth chambers were connected by a single ultra-high vacuum transfer tube. For ZnSe nucleated on Ga-rich GaAs, both substrates and epilayers, fuzzy RHEED spots, that lasted for several minutes were observed, suggesting a three-dimensional nucleation behavior. On the other hand, the ZnSe nucleated on As-rich GaAs showed a more two-dimensional growth mechanism with the RHEED pattern displaying almost no spottiness. Tamargo suggested that the critical parameter to obtain two-dimensional nucleation was the type of surface termination of the GaAs. Our results are partially consistent with these findings because the GaAs epilayers used in our work were typically As-stabilized. However, layer-by-layer growth has been observed for ZnSe nucleated on the transitional GaAs surfaces where the surface was neither Ga or As rich.

The two-dimensional growth of ZnSe on GaAs epilayers is further confirmed by the observation of intensity oscillations in the RHEED pattern. In MBE grown GaAs films, oscillations in the intensity of the diffraction

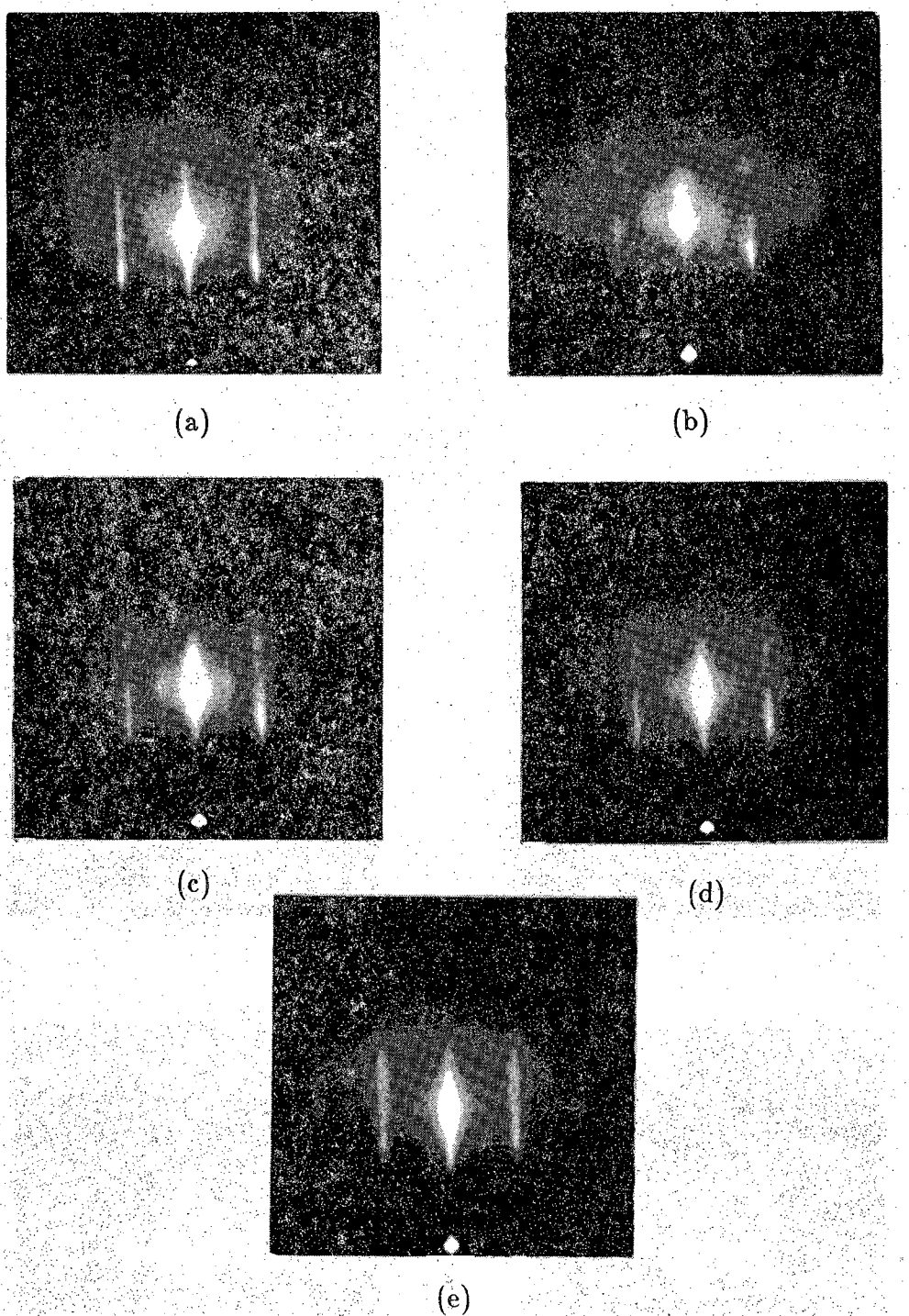


Figure 3.2. Evolution of the RHEED pattern for the nucleation of ZnSe on a GaAs MBE-grown epilayer for (a) t=0s, (b) t=9s, (c) t=29s, (d) t=150s, and (e) t=15min. The [110] azimuth is shown with the substrate at 320 ° C.

pattern [26] has been associated with a layer-by-layer growth mechanism. The variation in the intensity of the RHEED pattern is related to changes in surface roughness. In layer-by-layer growth, the smoothness of the surface is believed to vary periodically as is illustrated in Figure 3.3 (reproduced from ref. 26). Neave and Joyce [26] have defined a parameter Θ which represents the fractional layer coverage of the GaAs surface. For Θ equal to zero and one, the GaAs surface is at maximum smoothness and reflectivity. The minimum reflectivity occurs when the layer is half complete such that Θ equals one-half. Consequently, as Θ oscillates between zero and one in the layer-by-layer deposition, the intensity of the diffraction pattern also oscillates. Each oscillation represents the growth of one monolayer of GaAs. (A monolayer is defined as one layer of Ga atoms and one layer of As atoms which is equivalent to half of a unit cell of GaAs.) Oscillations in the RHEED pattern have previously been observed at Purdue for the II-VI compounds ZnSe and MnSe [27].

The RHEED intensity oscillations (RIOs) are observed by converting the light from the fluorescent screen into an electrical signal. The RIO setup is illustrated in Figure 3.4. First, the fluorescence is collected by an optical fiber that is mounted on a x-y stage on the focal plane of a Hasselblad 100C camera. A precision 500μm aperture is placed on the end of the optical fiber. The collected light is converted into an electrical signal by a photomultiplier tube having an S-10 photocathode. The electrical signal from the multiplier is then amplified and displayed on a time base chart recorder.

The intensity variations for ZnSe on GaAs epilayers, showing the layer-by-layer growth mechanism, appear in Figure 3.5. These 120 oscillations are detected from the specular spot in the [210] azimuth for ZOOEG320-7. In our case, the period of the oscillations represents the growth of one monolayer of ZnSe. From the period of the oscillations, a growth rate of approximately 1Å/sec is calculated ($g=a_o/(2T)$). The 120 oscillations represent layer-by-layer growth for over one-third of the ZnSe growth duration. The damping of the oscillations is attributed to additional ZnSe layers (three molecular monolayers) forming before completion of the underlying monolayers [26].

In contrast to the intensity oscillations seen in Figure 3.5, the nucleation of ZnSe on a GaAs substrate results in very little intensity variation. Shown in Figure 3.6, the specular spot in this case initially decreases, rises, and then decays to some average value. This type of

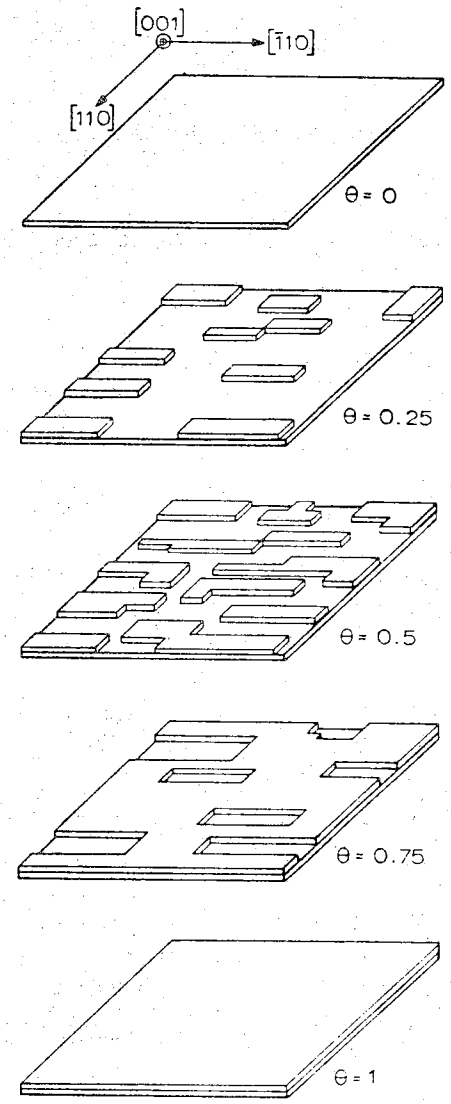


Figure 3.3. Illustration of how layer-by-layer growth causes a periodic variation in the surface reflectivity [26]. For Θ (percent surface coverage) of 0 and 1, the surface is at maximum reflectivity while at Θ of 0.5, the surface reflectivity is at a minimum.

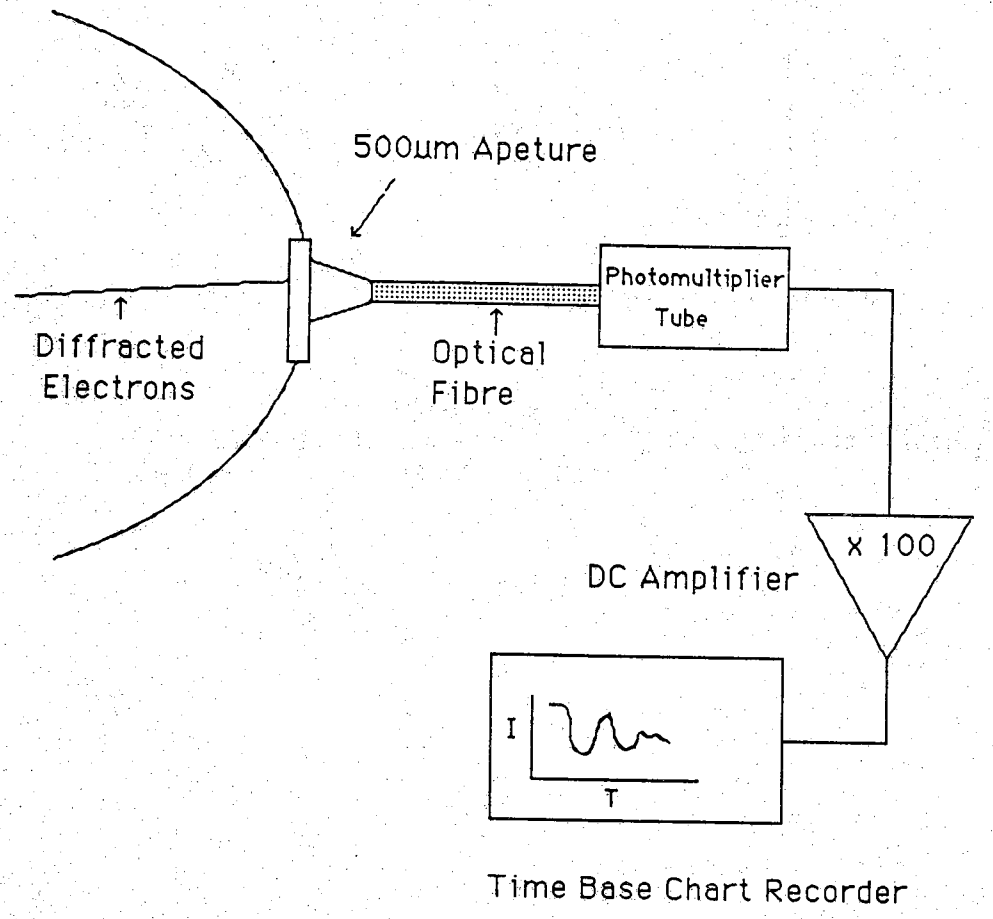


Figure 3.4. Schematic diagram of the detection system for monitoring the oscillations in the RHEED pattern.

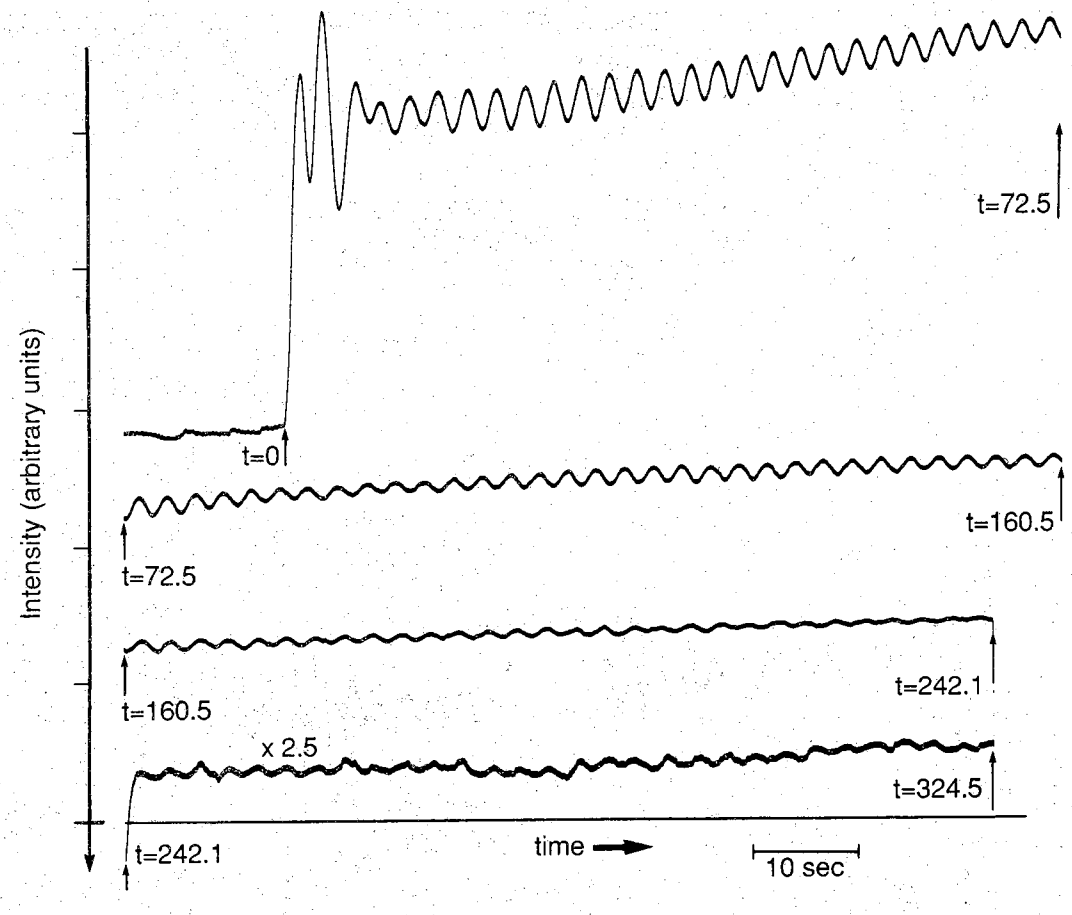


Figure 3.5. RHEED oscillations observed in the [210] during the nucleation of ZnSe on a GaAs epilayer at 320 ° C substrate temperature. Intensity increases downward in this plot.

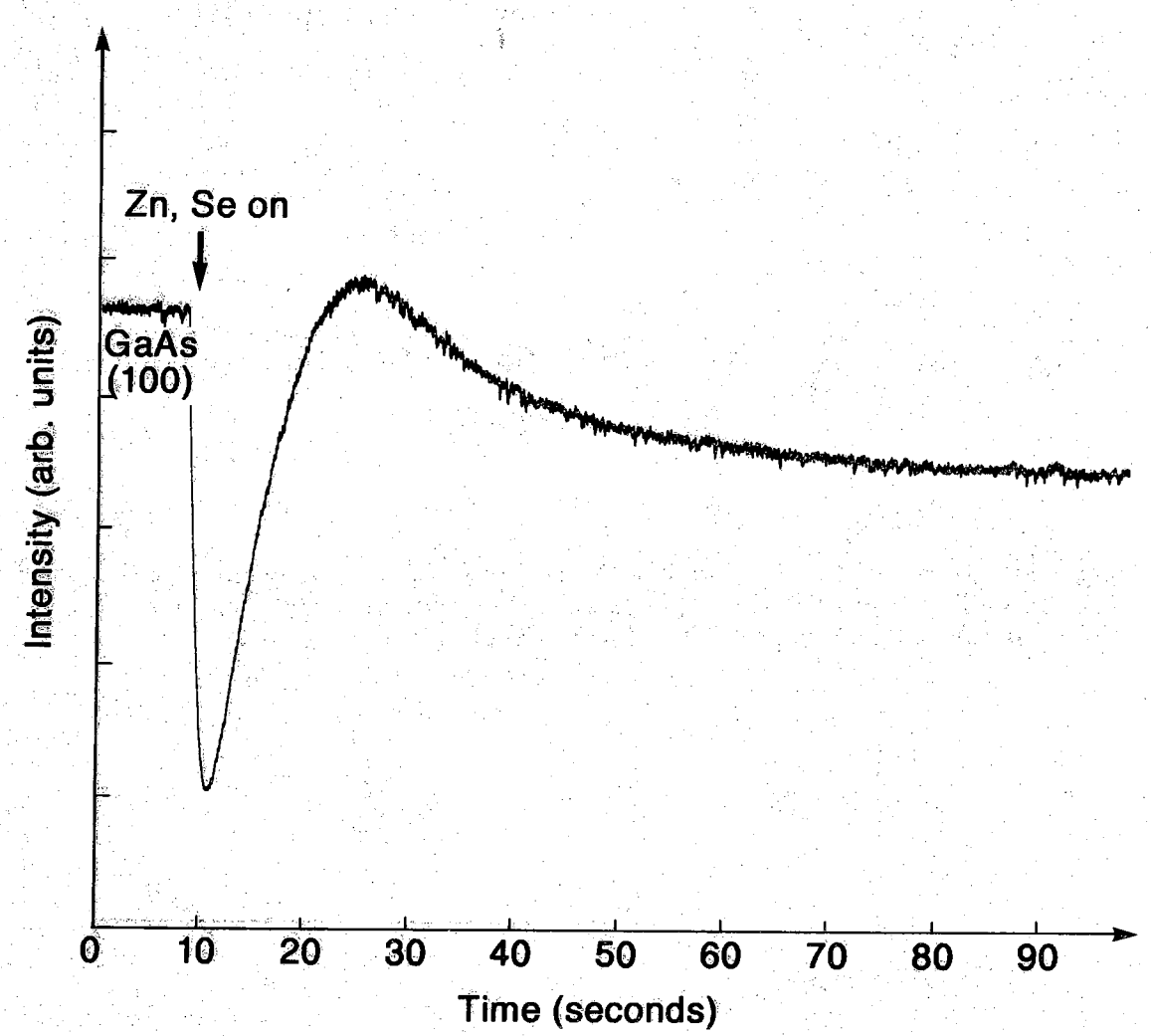


Figure 3.6. Intensity variation of the specular spot observed during the nucleation of ZnSe on a GaAs substrate at 400 ° C. The higher substrate temperature would be expected to favor two dimensional nucleation.

variation in the beam intensity is observed when InGaAs grows three dimensionally on GaAs epilayers [28] and agrees with the manner in which the RHEED pattern evolves under observation with the naked eye as previously discussed.

In summary, the evolution of the RHEED pattern for ZnSe on GaAs epilayers indicates a layer-by-layer growth mechanism where streaks are seen in the pattern after only a few seconds. RHEED intensity oscillations of the specular spot also confirm that ZnSe nucleates two-dimensionally on As-stablized GaAs epilayers. In contrast, ZnSe nucleated on Ga-rich GaAs substrates show three-dimensional growth behavior where ZnSe island formation leads to a dim spotty pattern and a lack of intensity oscillations.

3.2 Microstructure Analysis of ZnSe on GaAs(epi)

The following is a summary of the microstructure analysis of the ZnSe/GaAs(epi) heterostructure performed by C. Choi and N. Otsuka at Purdue [29]. Choi and Otsuka use transmission electron microscopy (TEM) to look at the interface between the two materials and also to study dislocations and defects in the heterostructure.

X-ray measurements of the lattice parameter of ZnSe grown on GaAs as a function of film thickness have revealed a substantial increase in the perpendicular lattice parameter for ZnSe film thicknesses below 2000Å. Because ZnSe and GaAs have different lattice spacings (ZnSe(bulk) = 5.66942Å, GaAs(bulk) = 5.6533Å, 0.25% lattice mismatch), very thin ZnSe layers suffer tetragonal distortion to accommodate the lattice mismatch. As the ZnSe in-plane lattice constant is reduced to match the lattice constant of the GaAs, the perpendicular or normal lattice constant of ZnSe expands. The expansion can be visualized as two different size boxes becoming adjoined at one side. If the total area of each box remains fixed, as the larger box reduces its width, its length must accordingly expand. The ZnSe is the larger box, obviously, and remains as a distorted semiconductor until the distortion is relaxed by the generation of misfit dislocations. The film thickness where the misfit dislocations occur is called the critical thickness.

In the x-ray data given by T. Yao [30], one sees the effect of the compressive strain on the normal lattice constant of ZnSe, Figure 3.7. The dark circles and the dashed line represent the normal and bulk ZnSe lattice constants, respectively. According to the figure, as the ZnSe film thickness approaches 2000Å, the normal lattice constant decreases dramatically. This

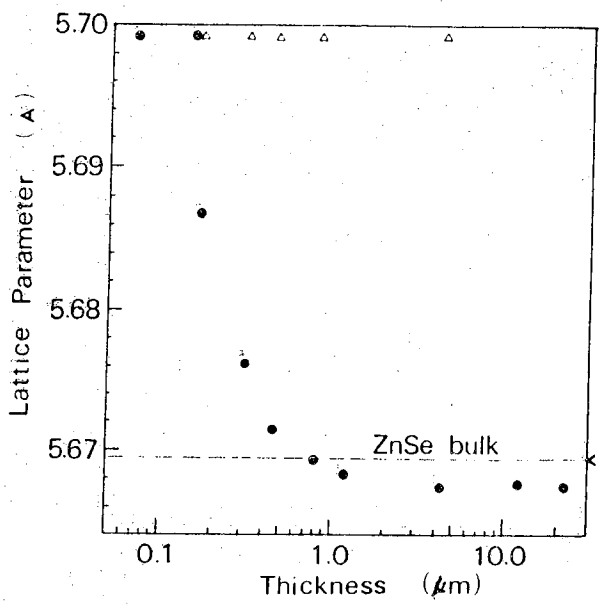


Figure 3.7. Lattice spacing normal to the ZnSe epilayer as measured by x-ray diffraction [30]. The dark spots are the main diffraction peaks while the dashed line is the bulk ZnSe lattice constant.

data is interpreted as the ZnSe film thickness for which the strain is being relieved by misfit dislocations. After the strain is relieved, the lattice constant becomes close to that of bulk ZnSe and decreases for ZnSe greater than 1μm. The reduction of the normal lattice constant at this point is thought to result from the difference in thermal expansion coefficients between ZnSe and GaAs which are reported to be 6.8×10^{-6}/K and 5.7×10^{-6}/K, respectively [30].

Because the ZnSe film thickness in the MIS devices is approximately 1000Å, the ZnSe is expected to be "pseudomorphic" such that the parallel atomic spacing of the ZnSe and the GaAs are the same. In this case, misfit dislocations are not expected to be present in the ZnSe which implys that the interface between the two materials should be coherent and free of defects. To confirm the pseudomorphic nature of the ZnSe, the heterostructure is examined with cross-sectional transmission electron microscopy. TEM monitors the transmission of high energy electrons through a very thin slice of the semiconductor and produces an image of the atomic lattice. Because TEM utilizes very high energy electrons (200KV), the measurement can detect atomic arrangements with a resolution as small as 2.3Å.

Figure 3.8 shows a cross-sectional bright field image of the 1000Å ZnSe epilayer grown on the MBE-grown GaAs epilayer. The interface appears as a sharp straight line with the epilayers free of the evidence of threading dislocations, thus confirming the pseudomorphic nature of the ZnSe. In contrast, Figure 3.9 shows a plan-view dark field image of a 1.3μm ZnSe film grown on a GaAs epilayer, ZOOEG320-1. A network of strain-relieving misfit and threading dislocations is clearly seen. In this film, dislocations are expected because the ZnSe is much thicker than the critical thickness of 1500Å-2000Å.

Even more interesting, a high resolution electron microscope (HREM) image of the pseudomorphic ZnSe/GaAs (epi) interface shows a coherent atomically sharp interface, Figure 3.10. The arrow in Fig. 3.10 indicates the location of the interface. It is almost impossible to observe any difference between the two sides of the picture, indicating that the pseudomorhpic ZnSe/GaAs(epi) interface is coherent. On the other hand, the ZnSe/GaAs(substrate) interface does not appear coherent and featureless in a HREM image [11]. The interface contains wavy, step-like boundary images which indicate the presence of small pits and steps. Because GaAs substrates are mechanically polished and chemically etched, these types of

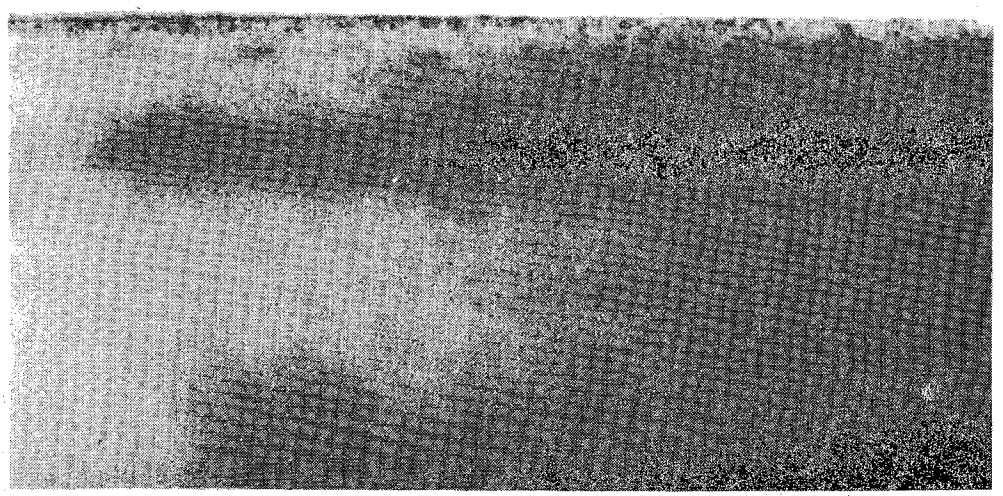


Figure 3.8. A cross-sectional bright field TEM image of a 1000Å ZnSe film on a GaAs epilayer showing the absence of threading and misfit dislocations.

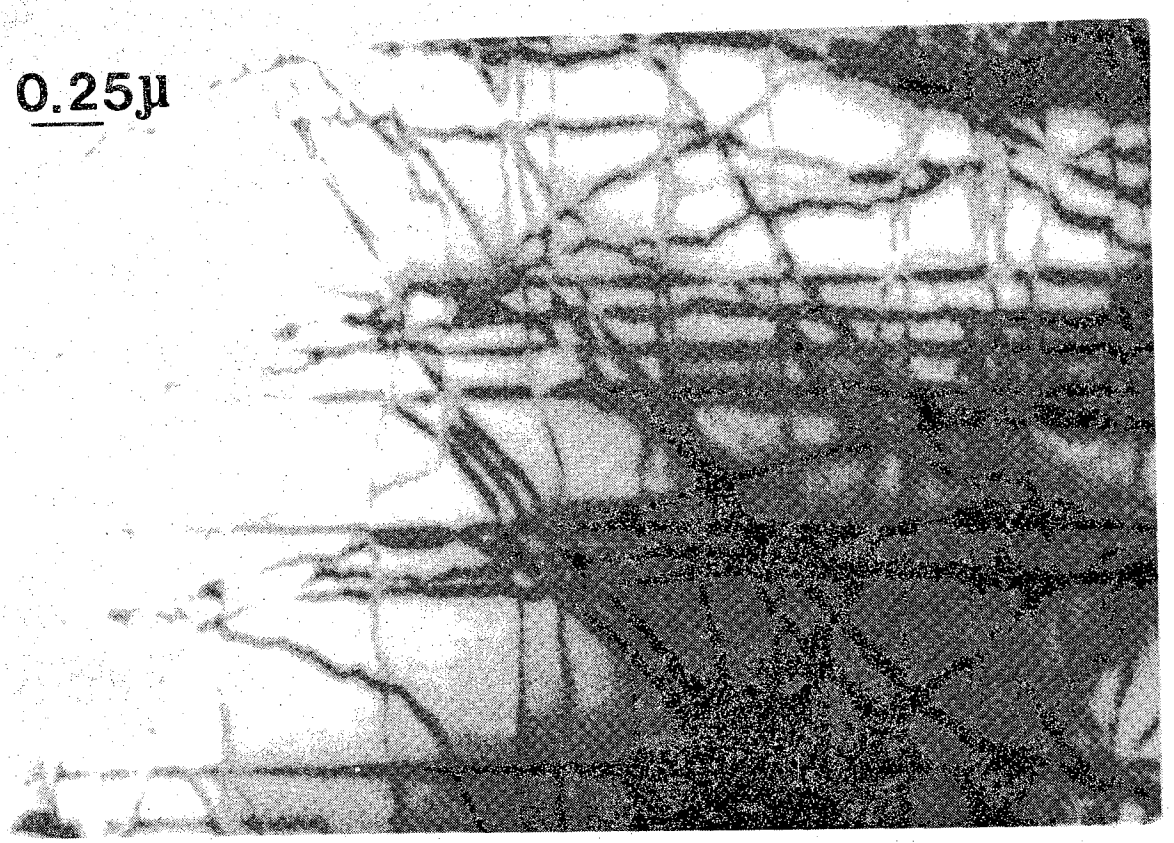


Figure 3.9. A plan view dark field image of the ZnSe/GaAs interface showing a network of misfit dislocation. The ZnSe layer thickness is 1.3μm.

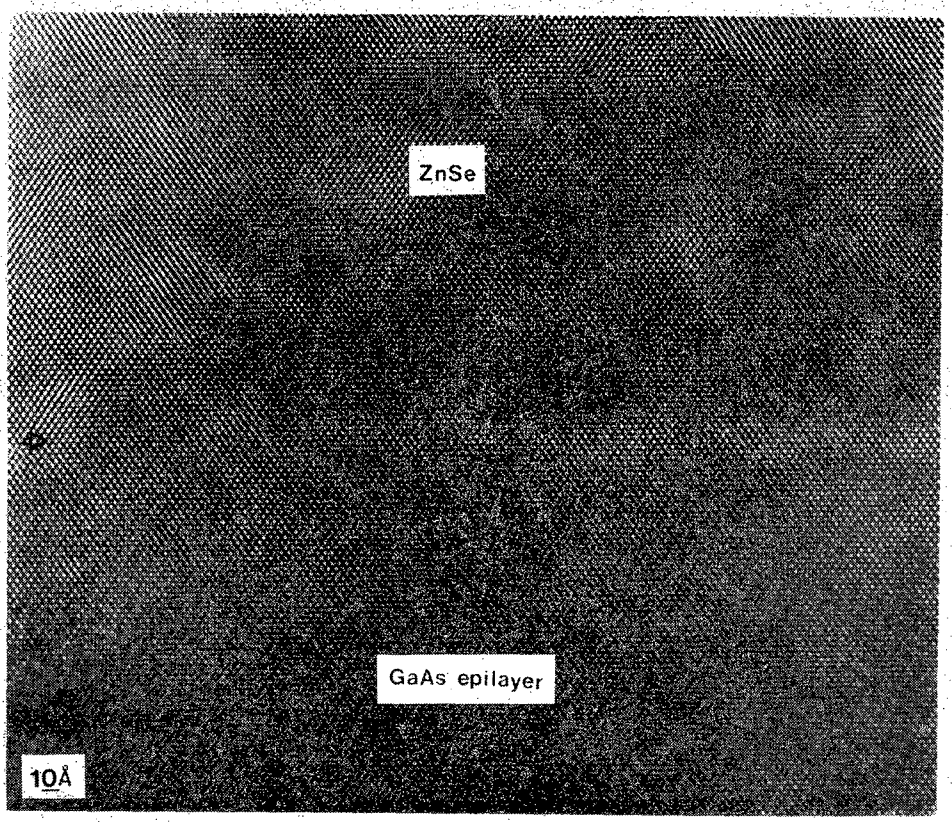


Figure 3.10. A high resolution electron micrograph of the ZnSe/GaAs epilayer interface showing coherent contact between the two crystals. The arrow indicates the heterostructure interface.

defects are expected. It is thought that these surface imperfections are potential nucleation sites where ZnSe can form islands during the initial nucleation on the GaAs substrate.

Hence, TEM analysis of the 1000Å ZnSe grown on GaAs epilayers reveals a coherent interface and a misfit dislocation free heterointerface. In this case, the ZnSe is a pseudomorphic layer with the same in-plane atomic spacing as the underlying GaAs. For ZnSe film thicknesses greater than the critical thickness, threading and misfit dislocations are observed.

3.3 Photoluminescence of Pseudomorphic ZnSe

Photoluminescence (PL) measurements, like TEM, reveal information about the strained nature of the 1000Å ZnSe/GaAs (epi) heterostructures. Not only does the lattice mismatch between the ZnSe and GaAs cause the lattice to distort, it also causes changes in the ZnSe energy bands. PL experiments use laser light to study the nature of these changes.

Typically, photoluminescence is performed by exciting valence band electrons into the conduction band with photons from a laser source. When the electrons recombine to the valence band, they emit light (luminescence) at particular wavelengths; it is the analysis of this luminescence that gives information about the changes in the energy band structure of the pseudomorphic ZnSe. The electrons are excited well above the band gap of the ZnSe and quickly relax to lower energies. The excited electrons couple with a hole before recombining to form a "particle" called an exciton which behaves like a hydrogen atom. Excitons have a binding energy below the conduction band edge given by the equation $E_x = m_r q^4/(2h^2\epsilon^2 n^2)$ where m_r is the effective reduced mass and n is an integer $\geqq 1$. The $n=1$ exciton is the farthest away from E_C with $n=\infty$ representing a free electron. Excitons can also be bound or attracted to impurities which places the exciton binding energy further into the bandgap.

In ZnSe PL studies, the ultraviolet line of the argon laser is used to excite the electrons above the 2.7eV band gap. The PL spectrum of a pseudomorphic film appears in Figure 3.11. The plot consists of intensity versus wavelength and was taken at 8 °K. At these temperatures, three distinct features are observed at 2.8178eV, 2.8064eV, and 2.7997eV. This portion of the spectrum represents the band edge luminescence with each peak originating from a separate exciton. The excitation density of the laser was 3.5W/cm^2, but identical data was observed at excitation levels

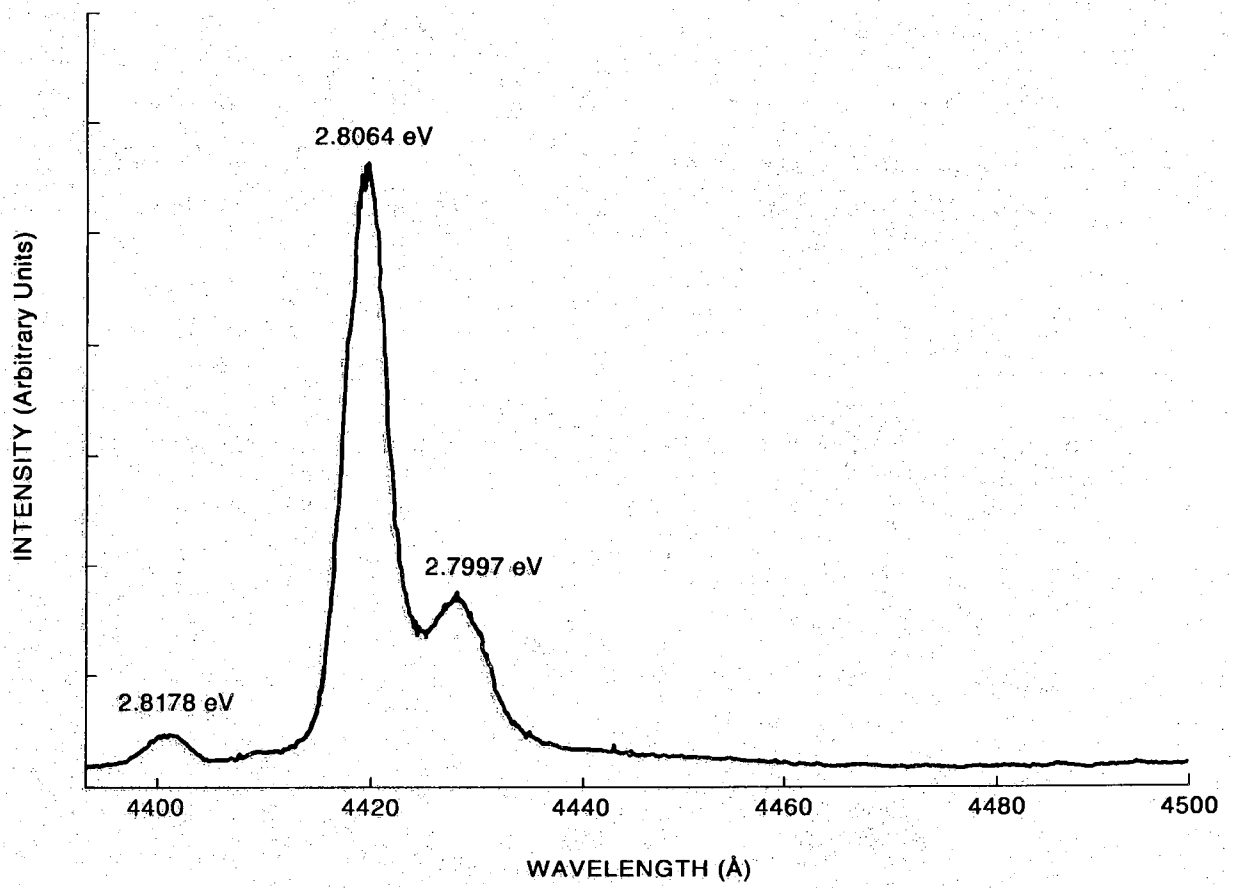


Figure 3.11. Photoluminescence spectrum of a 1000Å ZnSe epilayer on a 1.5μm GaAs epilayer taken at 8 °K. The excitation density was 3.5W/cm^2.

down to 75mW/cm^2.

Noteworthy in Fig. 3.11 is the dominance of the feature at 2.8064eV which is attributed to the n=1 free exciton [11,30]. The free exciton is shifted upwards by 4.4meV from the bulk transition energy. The shift is attributed to the 0.25% lattice mismatch between the ZnSe and the GaAs epilayers, and the sense of the shift agrees with the normal lattice constant value given in Figure 3.7. As the strain is relieved for thicker films and the in-plane lattice constant of the ZnSe approaches the bulk value, the n=1 exciton shifts to lower energies. For film thicknesses greater than 1μm, the free exciton appears at energies below its ZnSe (bulk) value.

The feature at 2.7997eV is attributed to a neutral donor bound exciton. According to Yao [31], the relative strength of this feature known as the I_x line increases with increasing layer thickness and eventually dominates over the entire spectrum. Like the free exciton, the I_x line shifts to lower energies for thicker films. It appears at 2.7984eV in a 2800Å thick ZnSe layer [31].

The origin of the high energy peak can be twofold, either the n=2 free exciton or n=1 free exciton to valence band transition. Because of the strain on the lattice in the pseudomorphic film, the heavy-hole (hh) and light-hole (lh) valence bands separate and allow for transitions to both bands (the uniaxial strain component causes the splitting of the lh and hh bands) [32]. The 11.4meV difference between the two high energy peaks is in the range for both the n=2 to hh and n=1 to lh transitions. The relative amplitudes of the two features at 77 °K as well as the comparable oscillator strengths revealed in modulated reflectance spectra [12] appear more consistent with the oscillator strength for light and heavy hole transitions than the n=2 excited exciton state. Theoretical strain calculations based on this premise (n=1 to lh rather than n=2 to hh) support this result and have recently been reported [33]. It should be noted that in 1.0μm ZnSe, the high energy feature is 15meV higher than the n=1 free exciton at a bulk value of 2.802eV and in this case represents the n=2 excited state to heavy-hole transition [31].

In summary, the PL data support the pseudomorphic nature of the 1000Å ZnSe/GaAs(epi) heterostructure where the lattice mismatch between the layers causes changes in the energy band structure of the ZnSe. A shift in the excitonic features by 4.4meV to higher energies is observed. More interesting is the presence of a n=1 to light hole transition which is not normally observed in PL spectra of thick ZnSe.

CHAPTER 4
DEVICE FABRICATION

4.1 Layout and Design

Three photolithographic mask levels are used to fabricate the doped channel metal/ZnSe/n-GaAs field-effect transistors. The processing steps are device isolation, source-drain contacts, and gate metalization. The mask plates are designed with the computer-aided-design program CMASK and fabricated on a Gyrex machine.

A composite layout of a single die appears in Figure 4.1. The die contains eight transistors with gate lengths of 2μm, 5μm, 10μm, 20μm, 45μm, 50μm, and 90μm. Planar open geometry is the predominant transistor configuration with a device width of 50μm. The contact spacings are 20 x 20μm^2, and the source-drain to gate spacing in these devices is typically 15-20μm. The largest area device is a closed geometry box FET. In this transistor, the drain is a 100μm x 100μm square surrounded by a gate ring of circumference 800μm. The source then surrounds the gate on three sides.

The final three devices on each die are a test resistor, a pad for probing source and drain contacts, and a dynamic memory (not used in this work). The test resistor is 50μm wide with contacts separated by 30μm, 60μm, and 120μm and is used for calculating series and contact resistances.

4.2 Transistor Fabrication

4.2.1 Device Isolation

The first fabrication step is called device isolation and is required primarily for depletion-mode transistors. (A depletion-mode transistor contains a conducting channel at 0V gate voltage, whereas an enhancement-mode transistor does not have a channel at a gate voltage of 0V.) The doped channel FETs ZOOEG320-7,9,12 are considered depletion mode transistors ,because the top most epilayer in each of these

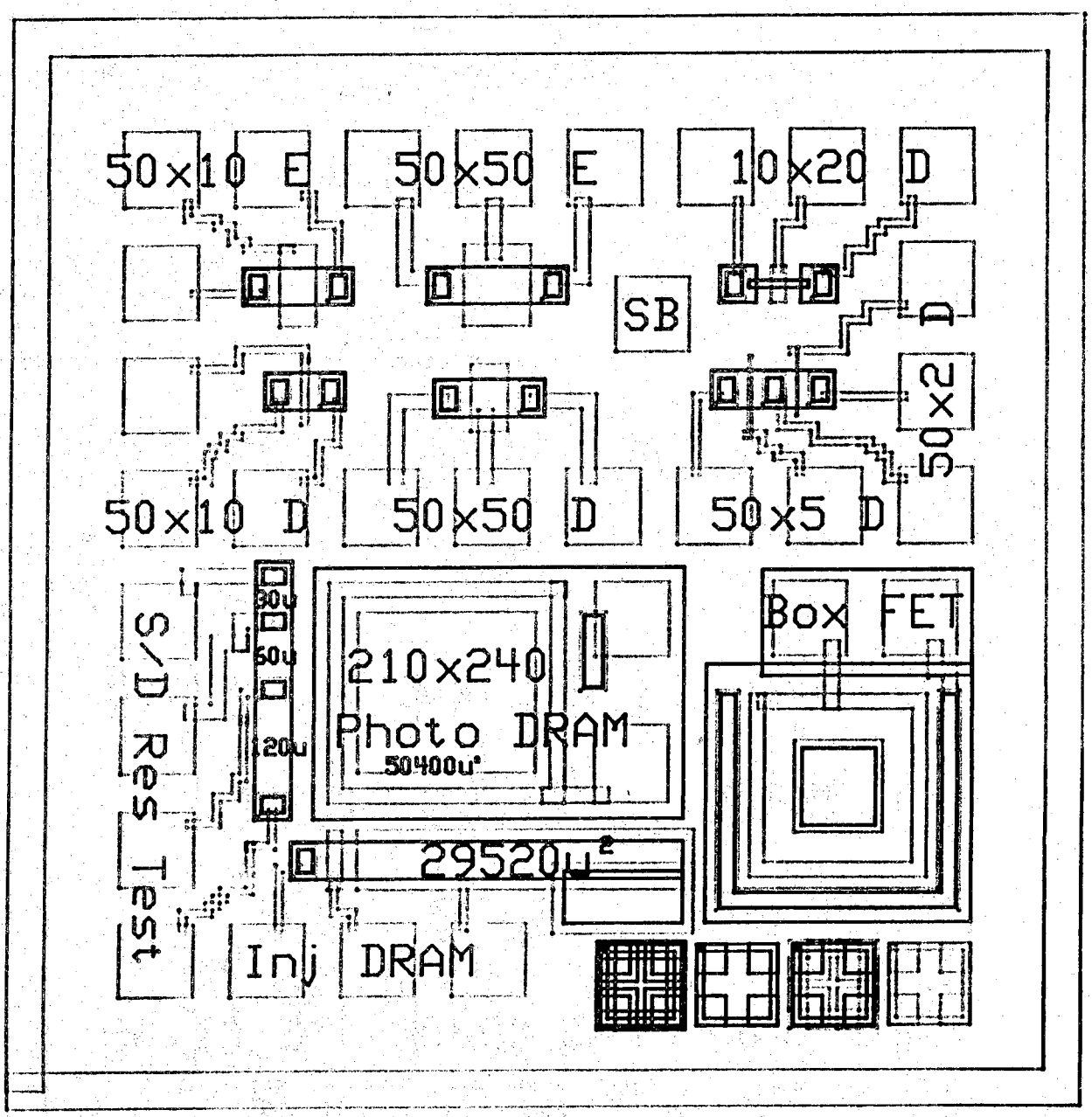


Figure 4.1. Top layout of the MISFET die. Transistor dimensions are given as width by length in units of μms.

heterostructures is conducting (n-GaAs). Device isolation consists of etching the doped semiconducting layer down to the underlying semi-insulating semiconductor to create insulating box-like mesas. The device mesas in our material system consist of a n-type GaAs channel surrounded by semi-insulating GaAs on the bottom, air on all four sides, and insulating ZnSe on the top. In this configuration, the conducting carriers are confined to a single transistor channel and must propagate underneath the gate electrode. Without isolation, current can flow outside of the gate region through the doped channel causing an unwanted source of drain current termed stray conductance. Because this current is outside of the gate region, stray conductance limits the modulating power of the gate voltage.

(Please see Appendix A for the doped channel field-effect transistor run sheet.)

To begin, the ZnSe/GaAs wafer (4mm x 4mm) is mounted on a silicon wafer (dia=2in.) in a "piggyback" manner in order to facilitate the handling of the sample during subsequent processing steps. Both the silicon and ZnSe/GaAs wafers are degreased according to Table 2. After a thorough degrease, the Si wafer is etched in 1:1 H_2SO_4 : H_2O_2 for ten minutes to ensure cleanliness. The Si wafer is then rinsed in deionized (D.I.) H_2O and dried in a 120 ° C oven. The MIS sample is also rinsed in H_2O but dryed with nitrogen (N_2) gas. When dry, the sample is mounted on the Si wafer using AZ1350J-SF positive photoresist (PR). The PR is hardened by heating the sample at 120 ° C for 15 minutes. PR is preferred as a mounting "glue" over black wax and indium because black wax evaporates under heat treatment and indium is etched by the photoresist developer.

After mounting, positive photoresist is applied to the top of the sample with a photoresist spinner. Positive photoresist is used at all times during the device fabrication and is always applied with a spin speed and time of 5000 r.p.m. and 60 sec., respectively. At these settings, a very uniform PR 1μm thick film is deposited. Because small samples are used in this work, spin speeds below 5000 r.p.m. result in thick photoresist at the sample edges. Structures defined under the thick PR will not develop properly. In the isolation procedure, the PR is prebaked at 90 ° C for 10 min. prior to alignment and exposure.

A Kasper mask aligner is used with the photographic mask plates to align and expose the mesa areas. The aligner uses ultraviolet (UV) radiation to expose the light sensitive PR while the sample is in intimate contact with

the patterning mask. With positive PR, areas of exposure become weak and are etched away by the developer. The sample is aligned with translation stages while viewing with a built in microscope. After bringing the sample in contact with the mask, the PR is exposed for 13.0 units ($\simeq$ 1min., 30sec). The aligner has a radiation integrator that calculates the total exposure that the PR receives. As the UV radiation intensity decreases due to aging of the bulb, the exposure time is automatically increased to maintain the same amount of total exposure.

The exposed sample is developed in 1:1 H_2O : AZ developer for 30-45 seconds. With proper exposure, the PR should be fully developed after 45 seconds. The sample is rinsed for 2 min. in D.I. H_2O, dried and then inspected under the microscope. If necessary, the PR can be developed again, although the effectiveness of the developer diminishes after the first immersion. The developed PR is hardbaked at 120 ° C for 10min.

The sample is now etched using two separate etches, one for the ZnSe and a second for the GaAs. The ZnSe is selectively etched at a calibrated etch rate of 100Å/sec with 400ml D.I. H_2O : 4ml HNO_3 : 0.2g $K_2Cr_2O_7$. The ZnSe layer is typically removed in 10-13 minutes. The fresh GaAs appears clear under a microscope. The success of the ZnSe etch depends on the cleanliness of the beakers and agitation of the sample during the etching process. (The beakers are cleaned with aqua-regia.) The GaAs is removed with 400ml D.I. H_20 : 12ml H_3PO_4 : 3ml H_20_2 that has a calibrated etch rate of 380-400Å/min. The GaAs is stripped at least 1000Å beyond the end of the doped channel.

The device isolation is completed by removing the PR with acetone. A schematic of the isolated transistor structure appears in Figure 4.2. The mesas appear as light green against the cream-gray color of the GaAs (naked eye). After rinsing in acetone, the sample is rinsed in methanol, H_2O and dried with N_2 gas.

4.2.2 Source-Drain Ohmic Contacts

The second processing level for the depletion mode FETs is defining source and drain contacts to the n-GaAs epilayer. After patterning, contact openings are etched in the ZnSe followed by an evaporation of a gold-germanium (Au/Ge) alloy (88% Au to 12% Ge). The metals are coevaporated on top of both the GaAs epilayer and protective PR. The PR is then removed with acetone which in turn lifts the Au/Ge off the entire

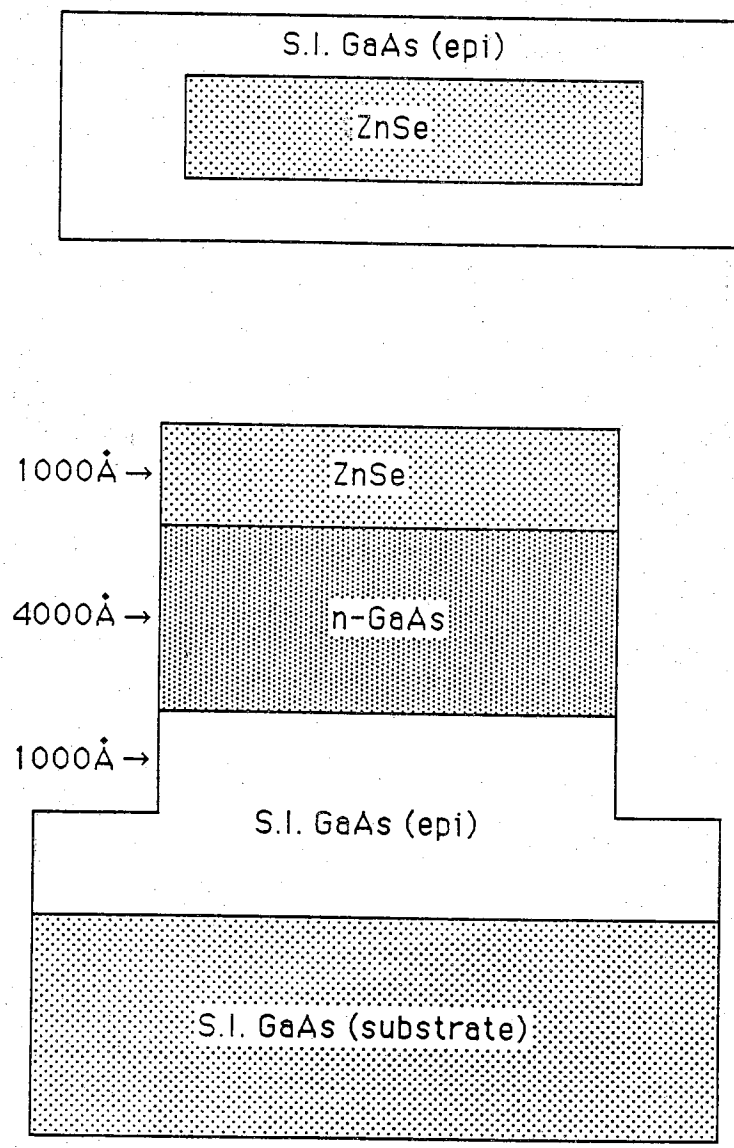


Figure 4.2. Schematic diagram of the MISFET after device isolation.

device except for the contact regions. This method for defining metals is known as a photoresist liftoff procedure.

The sample is then heated (annealed) causing the alloy metal to melt. The Ge atoms diffuse into the GaAs and replace some of the underlying Ga atoms. As a result, the source-drain n-GaAs becomes heavily doped n-type because Ge is a type IV element with four valence electrons and Ga is a type III element with only three valence electrons. The depletion width for the n+ GaAs/Au metal is small and hence permits quantum mechanical tunneling of carriers in both voltage directions; the Ge doping of the GaAs thus is a significant factor in forming ohmic contacts to n-GaAs in a field-effect transistor.

To begin the second level of processing, positive photoresist is applied to the sample using the PR spinner. After PR application, the sample is prebaked at 70 ° C for 10min. In a liftoff procedure, the sample should never be heated above 70 ° C. The sample is aligned in the Kasper aligner and exposed for 17.0 units (2.5min.).

The most critical step in the liftoff procedure is developing the photoresist. The sample is first soaked in xylene or chlorobenzene for 3 minutes. The xylene soak hardens the upper part of the PR. When the sample is developed (1:1 for 30 sec.), the PR near the sample etches faster than the hardened PR at the top which leaves a PR lip, Figure 4.3. During the liftoff of the metal alloy, the photoresist lip allows the acetone to penetrate the PR underneath the overlying metal. From Figure 4.3, it is obvious that the metal thickness can not exceed the PR thickness.

After patterning, the ZnSe is etched down to the n-GaAs as in the isolation procedure. The same ZnSe etch is used with a similar etch duration. The cleanliness of the etch is very important at this stage because residues left on the n-GaAs surface inhibit the diffusion of the Ge into the GaAs. The contact squares appear clear when properly etched. Prior to loading into the metal evaporator, the wafer is dipped in dilute ammonia hydroxide 400ml H_2O : 40ml NH_4OH for 40 sec. in order to strip residual GaAs oxides on the n-GaAs surface. The sample is quickly rinsed, dried and loaded into the metal evaporation system. Once the sample is etched, the wafer should be placed into the evaporator within five minutes in order to limit exposure of the n-GaAs epilayer surface to the air.

The Au/Ge alloy is evaporated in a NRC vacuum system. The NRC is pumped with a diffusion-mechanical pump system and can maintain a

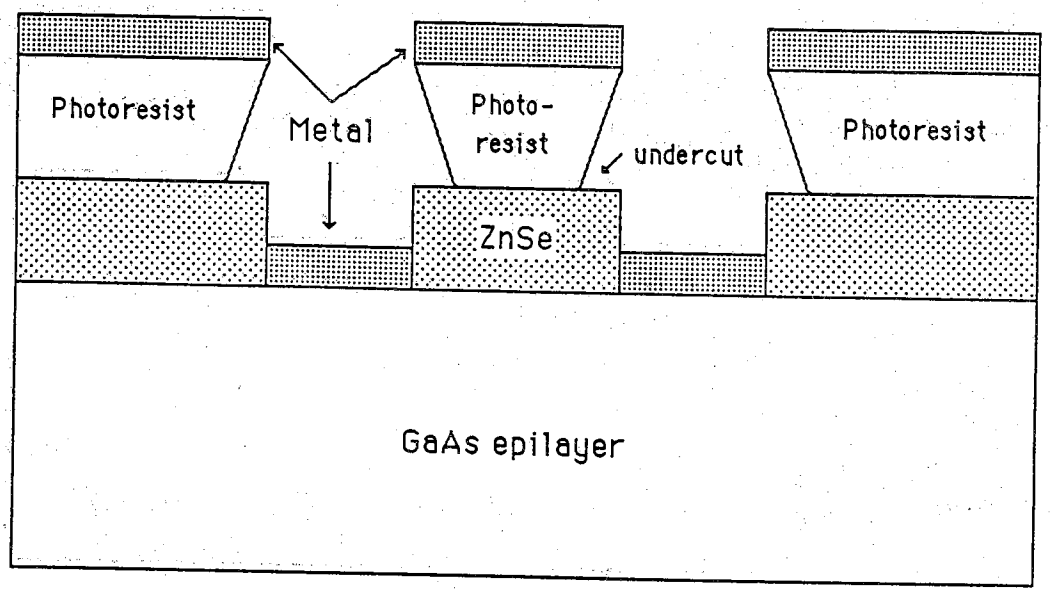


Figure 4.3. Illustration of the undercut photoresist in a liftoff procedure. After evaporation of the contact metal, the photoresist is removed and subsequently "lifts" the metal away from the protected semiconductor.

vacuum of $5x10^{-7}$ Torr. Three metallic pellets consisting of 88%Au-12%Ge are the source material and provide a 3000Å thick metallic layer when fully evaporated. The pellets are loaded into a titanium (Ti) boat that rests between two metal electrodes. The sample is placed vertically above the pellets with the exposed GaAs facing the metal. The entire system is housed in a glass bell jar. The metal is melted and evaporated by resistive heating (5V,6A) where the gold evaporates first followed by the germanium. When properly performed, the Ti boat should be completely empty at the end of the evaporation.

After deposition of the metal alloy, the Au/Ge is lifted off by rinsing in acetone. The liftoff can be enhanced by lightly squirting the sample with acetone. If the PR does not come off, the PR can be removed by one of the following steps; boiling and ultrasonic cleaning in acetone or lightly brushing with a cotton swab dipped in acetone. (These steps are not a preferred means for removing photoresist because they tend to damage the wafer.)

Immediately following the liftoff, the metal is heated at 450 ° C for 90 sec. in a Marshall oven. The sample is loaded on a hot quartz boat and placed in the center of the oven. The 90 sec. period begins when the boat reaches the center of the oven. The sample is annealed in the presence of flowing nitrogen gas. After 90sec., the sample is removed and inspected under the microscope. The Au/Ge metal appears bright gold in color and smooth in texture under the microscope prior to heating but looks dark brown, bubbly and balled up after the anneal is complete. If the metal does not look rough, then the Ge did not diffuse into the GaAs. The diffusion process can be inhibited if either the composition of the two metals on the GaAs is not 88%Au to 12%Ge and-or there is some type of thin residual film between the metal and the n-GaAs.

Anneal of the Au/Ge alloy metal is commonly performed in a temperature range of 356-450 ° C [34]. The parameters 450 ° C and 90sec. were chosen based on successful ohmic contact research at Purdue. The balling up effect of the gold tended to increase with longer anneal times. The balling up effect can be reduced by including a layer of nickel with the Au and Ge. Nickel will also help the Ge atoms to diffuse into the n-GaAs and is used in industrial GaAs applications to achieve ohmic contacts with very low contact resistances [35]. (Contact resistance is further discussed in section 5.2.1.)

A cross section of the MIS device after ohmic contact alloy appears in Figure 4.4. The ohmic contacts are tested by electrical probing. For improper diffusion of the Ge metal, the I-V curve as illustrated in Figure 4.5(a) is characteristic of two back-to-back Schottky diodes. No matter what source-drain voltage is applied, one of the two Schottky diodes is always reversed biased. Current will flow between the contacts when the reversed biased diode breaks down due to avalanche multiplication. Because avalanche breakdown (discussed in section 5.2.3) is inversely related to background doping, a higher breakdown voltage means that less Ge has been incorporated into the n-GaAs. As more Ge dopes the source-drain regions, current flows at a smaller drain-source voltage. Eventually, the depletion width in the n-GaAs becomes small enough that quantum mechanical tunneling dominates over thermionic emission and current flows in both voltage directions even for very small voltages.

4.2.3 Top Metal

The final processing step is to pattern aluminum as the gate metal of the transistor. The aluminum (Al) is defined in the same fashion as the Au/Ge using a PR liftoff procedure. The top metal not only serves as the gate but also contacts the source-drain gold metal and branches off into bigger pads that are used for ultrasonic bonding. Aluminum is preferred as the top metal because it is easier to bond to Al than to Au.

The top metal liftoff procedure is identical to the source-drain metalization. After exposure and development of the PR, the sample is loaded into the NRC system with aluminum source material. Five aluminum bars, 0.062in. in dia. and approximately 1in. long, are inserted into a tungsten filament. The filament is place between two electrodes, and the sample is again suspended above the metal. The evaporation takes place at a background pressure of $5x10^{-7}$ Torr. The aluminum is melted with a 10V power supply at a current of 6A in approximatley 2-3 min.

After the evaporation, the PR is lifted off by squirting with acetone as mentioned before. With 5 bars of aluminum, the top metal is approximately 3000-5000Å thick, and hence the Al liftoff is harder than the Au/Ge. The finished device as illustrated in Figure 4.6 is mounted in a 24 pin dual-inline-package (DIP) with indium solder. The pads are connected to the DIP by ultrasonic bonding with aluminum wire.

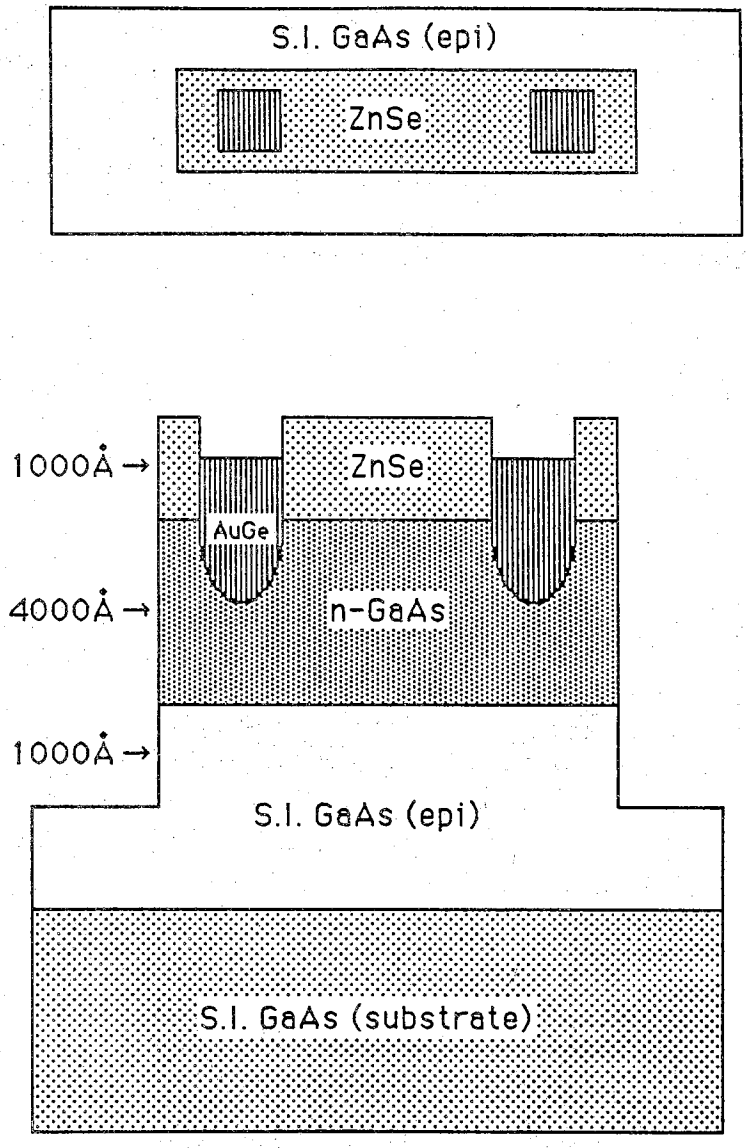
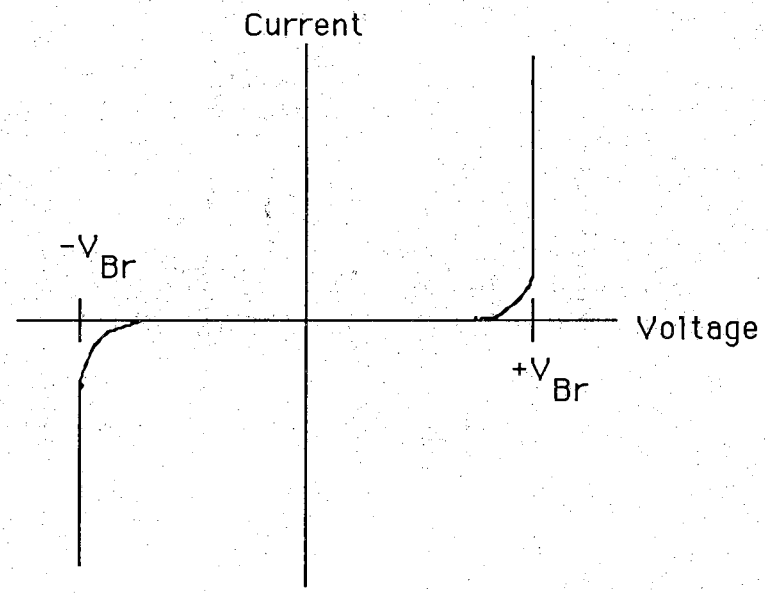
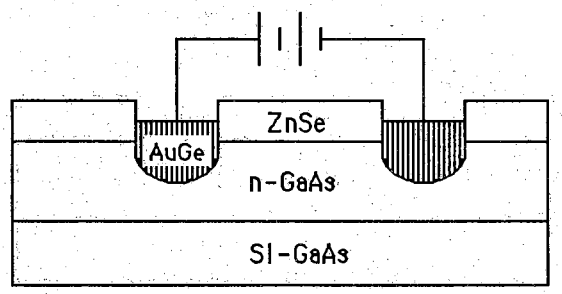


Figure 4.4. Schematic diagram of the MISFET after Au/Ge evaporation, liftoff and anneal.



(a)



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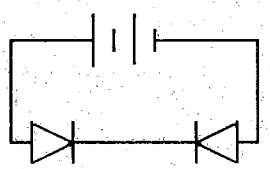

(c)

Figure 4.5. IV relationship (a) for an improperly alloyed ohmic contact. The source-drain contacts (b) appear as two diodes (c) in series. Current flows when the reverse biased diode breaks down due to avalanche multiplication.

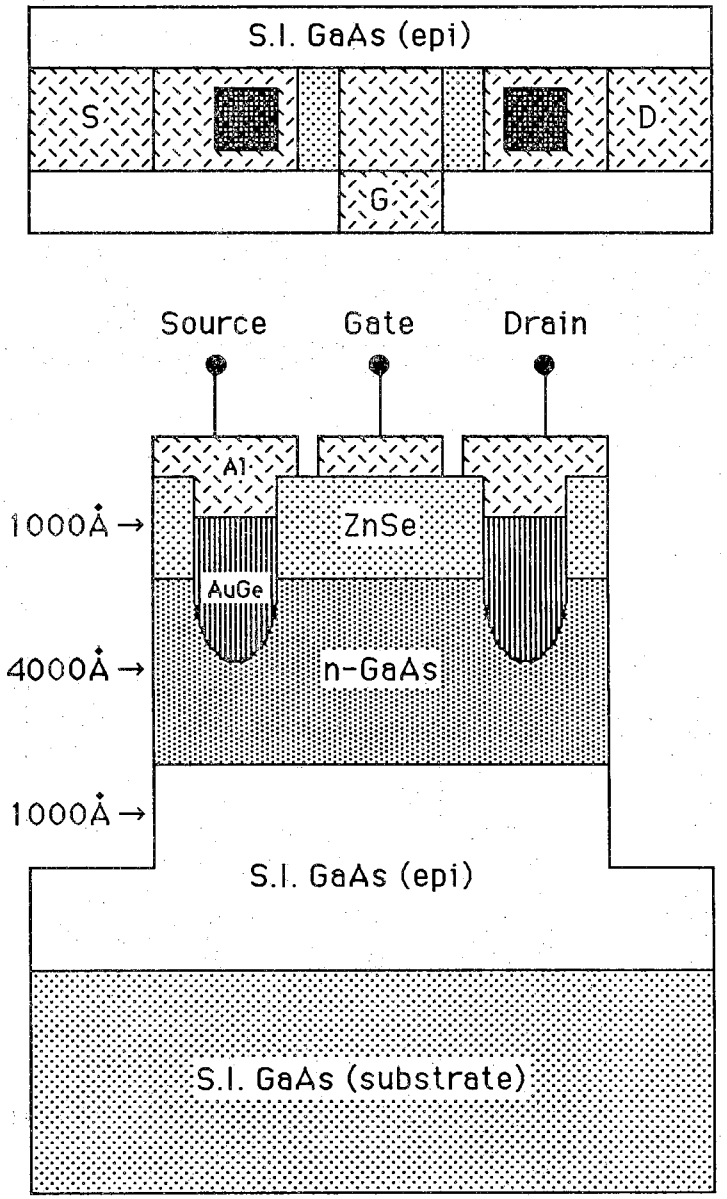

Figure 4.6. Schematic diagram of the completed ZnSe/n-GaAs depletion mode field-effect transistor.

CHAPTER 5
ELECTRICAL CHARACTERIZATION

In this chapter, we present the electrical characteristics of the ZnSe/n-GaAs heterostructure. The current-voltage (IV) and capacitance-voltage (CV) relationships for an MIS-capacitor are briefly examined. Second, the transistor characteristics of a n-channel depletion-mode device are given. The MISFET evaluation is divided into three sections, a study of long channel devices, short channel devices, and the gate region.

5.1 ZnSe/n-GaAs Capacitor

This section is a summary of the experimentation carried out by Dave Munich on the electrical characterization of the ZnSe/GaAs(epi) capacitor. It is included for completeness and to properly orient the reader relative to the MIS properties of the field-effect transistors given later. The reader is referred to reference 36 for additional details.

The MIS capacitor consists of an aluminum gate on top of a ZnSe/GaAs(epi) heterostructure, Figure 5.1. The gate metal is defined by a photoresist liftoff procedure similar to the process described in section 4.2.3. The GaAs epilayer is doped either n or p type throughout the entire MBE grown structure including the GaAs substrate. Ohmic contact is made to the GaAs substrate with indium solder. The capacitance of the heterostructure is measured using a Hewlett Packard LCR bridge which evaluates the rate of change of charge with respect to a small A.C. voltage applied to the capacitor, $C=dQ/dV$. The A.C. voltage (15mV RMS and 1MHz for example) is superimposed on a D.C. voltage that is swept at a very slow rate from one gate bias level to another resulting in a continuous plot of the differential MIS capacitance versus the gate voltage.

The capacitance versus gate potential at 77 °K of ZOOEG320-4 ($N_D=1x10^{17}cm^{-3}$) is shown in Figure 5.2.

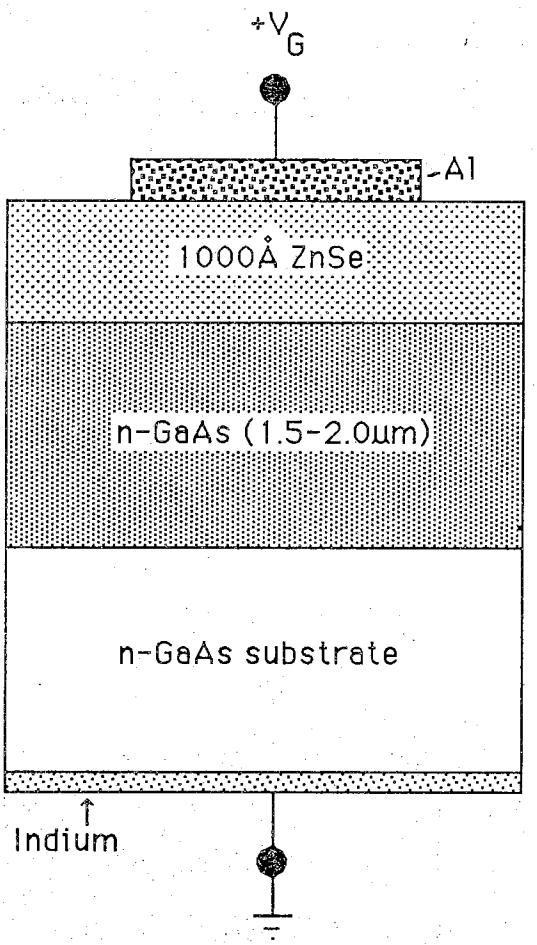

Figure 5.1. Schematic diagram of the ZnSe/n-GaAs MIS capacitor.

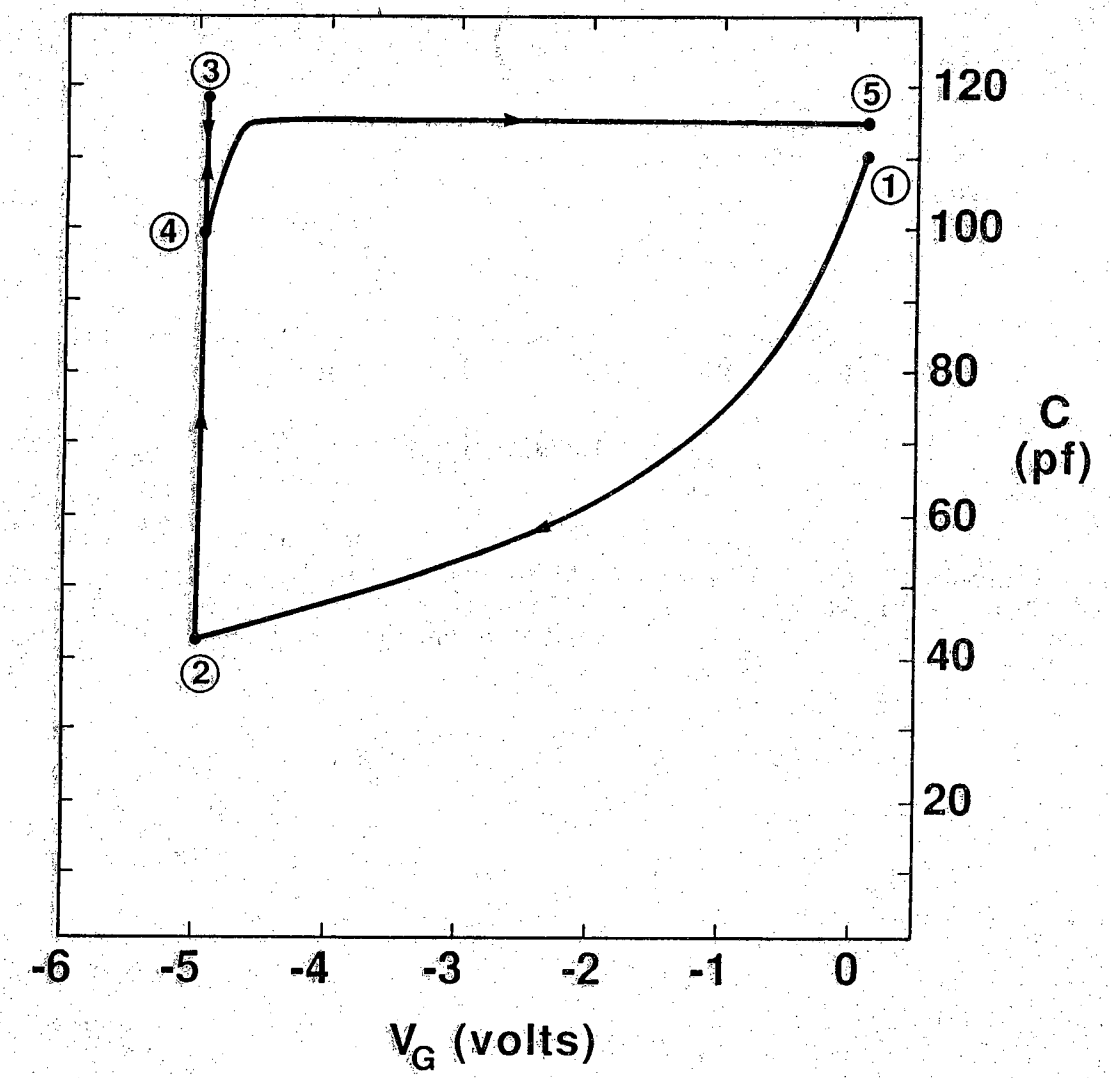

Figure 5.2. Capacitance versus voltage plot for the MIS capacitor in the dark at 77°K. The D.C. sweep rate is 500mV/sec and the sampling frequency is 1MHz.

This curve was taken at a sampling frequency of 1MHz, a D.C. sweep rate of 500mV/sec, and with no initial illumination. The C-V plot shows capacitance decreasing with negatively increasing V_G which is typical of a MIS-C in depletion and deep depletion. The gate capacitance in depletion is given by the series combination of the insulator capacitance (C_o) and the semiconductor capacitance (C_s). The measured capacitance is related to the two series capacitances by equation 5.1. Equations 5.2-5.6 also define quantities pertinent to the MIS-C. Equations 5.2 and 5.3, for example are the oxide and semiconductor capacitances, respectively. Equations 5.4 and 5.5 relate the semiconductor surface potential to the ideal applied gate voltage and equation 5.6 relates this same surface potential to the depletion width in the semiconductor. The reader is referred to reference 37 for an excellent overview of MIS capacitors and field-effect devices.

$$C_G=\frac{C_sC_o}{C_s+C_o} \tag{5.1}$$

$$C_o=\frac{K_o\epsilon_oA}{x_o} \tag{5.2}$$

$$C_s=\frac{K_s\epsilon_oA}{W(V_G')} \tag{5.3}$$

$$V_G'=\phi_s+\sqrt{2V_o\phi_s} \tag{5.4}$$

$$V_o=\frac{qN_DK_s\epsilon_o}{C_o^2} \tag{5.5}$$

$$W=\left(\frac{2K_s\epsilon_o\phi_s}{qN_D}\right)^{1/2} \tag{5.6}$$

The parameter definitions are summarized in Table 3.

Table 3. Parameter definitions for MIS devices. The values pertain to the n-channel FET described in section 5.2.

Symbol	Definition	Value
C_o	$K_o\epsilon_o/x_o$	$7.97x10^{-8}F/cm^2$
C_s	$K_s\epsilon_o/W$	
K_o	ZnSe dielectric constant	8.8
K_s	GaAs dielectric constant	12.95
x_o	Insulator thickness	1000Å
x_o'	$K_s x_o/K_o$	1,577Å
W	GaAs Depletion Width	
ϵ_o	Permittivity	$8.854x10^{-14}F/cm^2$
q	Electron charge	$1.6x10^{-19}C$
n_i	intrinsic conc. (GaAs)	$1.79x10^6cm^{-3}$
kT/q		0.259eV (300K)
ϕ_s	Surface Potential	
N_D	Donor Density	$1.5x10^{16}cm^{-3}$
μ	Electron Mobility	$4000cm^2/Vsec$
Z	Gate Width	$50.0\mu m$
L	Gate Length	$90.0/45.0\mu m$
a	Channel thickness	4000Å
g_m	Transconductance	
v_s	GaAs- sat. velocity	$1.2x10^7cm/sec$
V_o	$qN_DK_s\epsilon_o/C_o^2$	
V_δ	$-qK_s\epsilon_oN_D/2C_o^2$	-0.22V
V_G'	Ideal Gate Voltage	
V_{FB}	Flatband Voltage	0.348V
V_D	Drain Voltage	
V_T	Threshhold Voltage	
V_P	Pinchoff Voltage	

Under equilibrium conditions, the maximum depletion width occurs when the surface potential ϕ_s is approximately equal to $2\phi_f$ where $\phi_f = (kT/q)\ln(N_D/n_i)$. At a surface potential of $2\phi_f$ the GaAs semiconductor is said to be at the onset of inversion where the semiconductor polarity type effectively reverts to the opposite type. In this case, the n-GaAs would begin to look p-type at the ZnSe/GaAs(epi) interface. The voltage at which the GaAs semiconductor reaches the onset of inversion is called the threshhold voltage (V_T), and for $|V_G| > |V_T|$, the depletion region W is theoretically fixed at a maximum value W_T given by equation 5.7.

$$W_T = \left(\frac{2K_s\epsilon_o 2\phi_f}{qN_D} \right)^{1/2} \tag{5.7}$$

Using equations 5.1 - 5.6, a threshhold voltage of -4.0V is calculated for the capacitor in Figure 5.2. Notice, however, that C_G continues to decrease beyond V_T which indicates that the depletion region in the n-GaAs is still increasing. (For a fixed oxide capacitance, a continually decreasing gate capacitance indicates that the semiconductor capacitance is decreasing. From equation 5.3, it is apparent that for C_s to decrease W must increase.) This C-V characteristic suggests that the capacitor is in deep depletion where W is greater than W_T. Deep depletion occurs in a MIS/MOS capacitor when either the sweep rate of the D.C. voltage is greater than the generation rate of the minority carriers and-or the minority carriers, holes in this case, leak away from the insulator/semiconductor interface faster than they are generated. The ZnSe/GaAs capacitors go into deep depletion in this manner at both 77 ° K and room temperature.

The low temperature C-V characteristic (Figure 5.2) is identical in shape to the characteristic of a conventional MIS capacitor but can also be interpreted as a heterostructure containing a very high concentration of interfacial traps at the insulator/semiconductor interface. Experimentation with charge coupled devices has shown that positive charge at the ZnSe/n-GaAs interface is not mobile which gives evidence that the ZnSe/GaAs(epi) heterostructure does have a high concentration of surface states. The C-V profile in Figure 5.2 can thus be explained as follows. The gate capacitance begins at point 1 with V_G equal to 0V and the capacitor sitting in the dark. Next, the curve is swept into reverse bias 1 -> 2 where the depletion width exceeds W_T. At gate voltage 2, the capacitor is illuminated with a bright microscope light causing C_G to rise toward C_o. Photogenerated holes drift

to the interface, allowing trapped electrons to recombine. The reduction in trapped electrons causes the depletion width in the n-GaAs to shrink towards the value it had at 0V and hence C_G also approaches its 0V value. Now the light is turned off and the gate voltage is swept towards 0V resulting in a "linear-sweep" type of characteristic, 4 -> 5. As the negative charge on the Al gate is reduced the empty interface traps begin to capture electrons from the n-GaAs. Arriving at 0V, the charge nature of the interface is the same as at point 1, and the C-V cycle can be repeated.

Further evidence for the presence of surface states at the ZnSe/GaAs interface is observed in several capacitor structures that display a dispersion of the C-V curves with frequency. As the frequency of the small signal A.C. voltage is reduced, the measured capacitance C_G rises near zero bias. This capacitance dispersion is caused by surface states responding to the low frequency A.C. voltage and is observed in GaAs devices that have a high level of interface states [6].

The gate voltage bias range over which the MIS-C can be measured is quite limited, as indicated in the C-V characteristic. The current-voltage characteristic is plotted in Figure 5.3 showing an operating voltage range of 0V to -6.0V. The I-V data is taken on a HP4140B picoammeter in the dark at 77°K. The gate voltage polarity is similar to the capacitance measurement with the gate electrode positive with respect to the ohmic contact. The current characteristic is similar in shape to the rectifying behavior usually observed in a metal-semiconductor Schottky barrier.

The reverse bias current appears to originate from thermionic emission of electrons over the ZnSe/GaAs conduction band barrier. The current increases slightly from 0V to -6.0V indicating a lowering of the energy barrier with increasingly negative gate bias. At -6.0V the GaAs is apparently breaking down due to avalanche multiplication or impact ionization. As is expected for a semiconductor heterostructure, there is substantial electrical current flowing through the gate electrode for positive gate voltages. As discussed in reference 36, the forward bias current is thought to be dominated by electrons tunneling through the ZnSe as aided by the surface states. Considerable interface charge may cause the ZnSe conduction band to be sharply bent under forward bias permitting quantum mechanical tunneling of electrons. Obviously, the large forward bias current at 0V is not desired and has not allowed the operation of the MIS capacitors in the accumulation region.

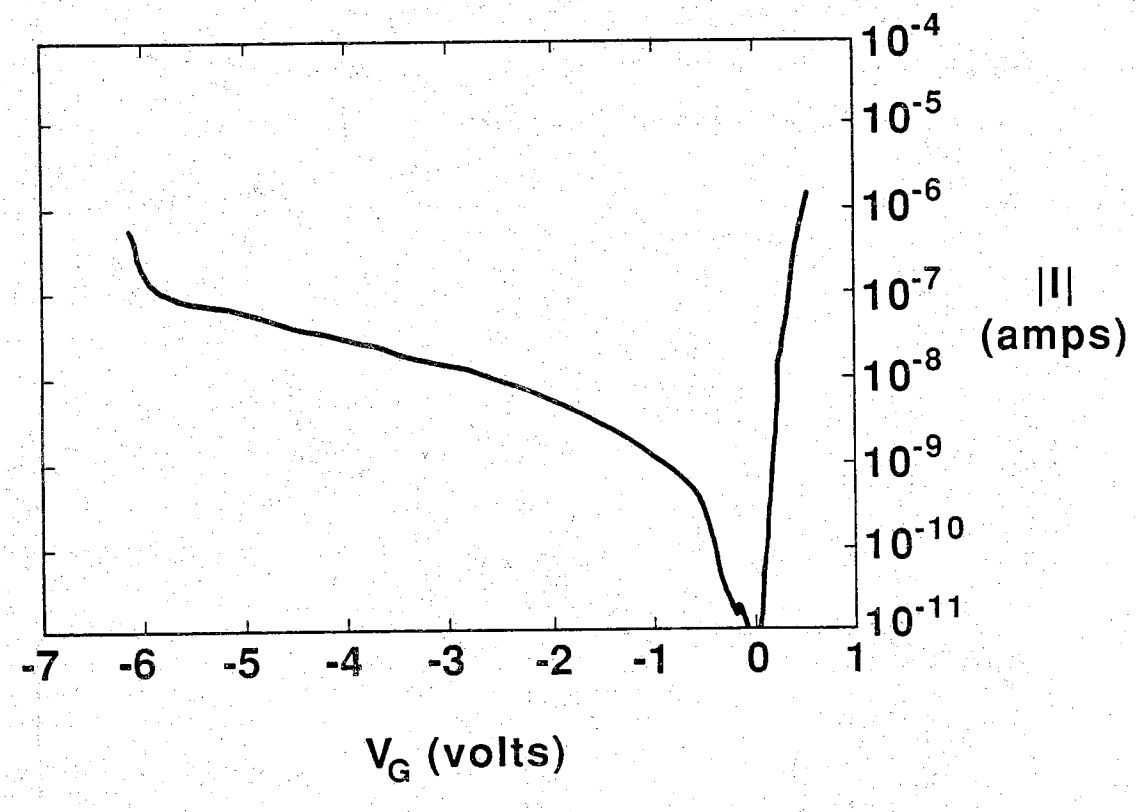

Figure 5.3. Current-voltage relationship for the MIS capacitor at 77 ° K.

5.2 ZnSe/n-GaAs Field-Effect Transistors

The following sections describe the transistor characteristics of the doped channel field-effect transistor ZOOEG320-7 (4000Å channel with $N_D=1.5x10^{16}cm^{-3}$). The other two doped channel field-effect transistors were unsuccessfully fabricated. ZOOEG320-9 (1500Å, $N_D=3x10^{17}cm^{-3}$) could not be isolated because both the semi-insulating GaAs substrate and buffer layer were conducting. Because the GaAs in ZOOEG320-12 (1000Å, $N_D=3x10^{17}cm^{-3}$ with a buried GaAs super lattice) apparently contained a large quantity of non-stoichiometric defects, it was impossible to make ohmic contact to the n-type channel. The I-V relationship of the source-drain contacts without any metal gate appeared as an open-circuit.

5.2.1 Long Channel Devices

The field-effect transistors in this work are similar to the junction field-effect transistor (JFET), the metal oxide semiconductor field-effect transistor (MOSFET), and the very popular metal-semiconductor field-effect transistor (MESFET), where an electric field perpendicular to the channel modulates a current of carriers flowing from a source to a drain. The source is the supplier of carriers which are electrons in these devices and is always referenced as the grounded terminal. The drain is biased at a more positive potential, Figure 5.4, creating the potential gradient under which electrons propagate. The gate is the third terminal of the transistor, and the gate voltage is also referenced with respect to the grounded source.

The gate region in the doped channel field-effect transistor consists of an insulator sandwiched between a metal electrode and the doped channel. This gate structure is similar to the silicon MOS design except that the dielectric insulator in this case is not a native oxide of the host semiconductor GaAs. As in all field-effect devices, the gate in this FET modulates the carrier density (n) by an applied gate voltage V_G. Electrons at the gate metal cause the depletion width in the GaAs to widen which subsequently narrows the conducting channel and reduces I_D. For small voltages the field-effect transistor behaves like a voltage controlled resistor.

The derivation of the current equations for the doped channel FET is similar to the GaAs based MESFET. In this analysis, some of the gate potential is "dropped" across the ZnSe and does not effect the electron density in the n-GaAs. This voltage drop is taken into account in deriving the current equations. (In the MESFET derivation, the modulating gate

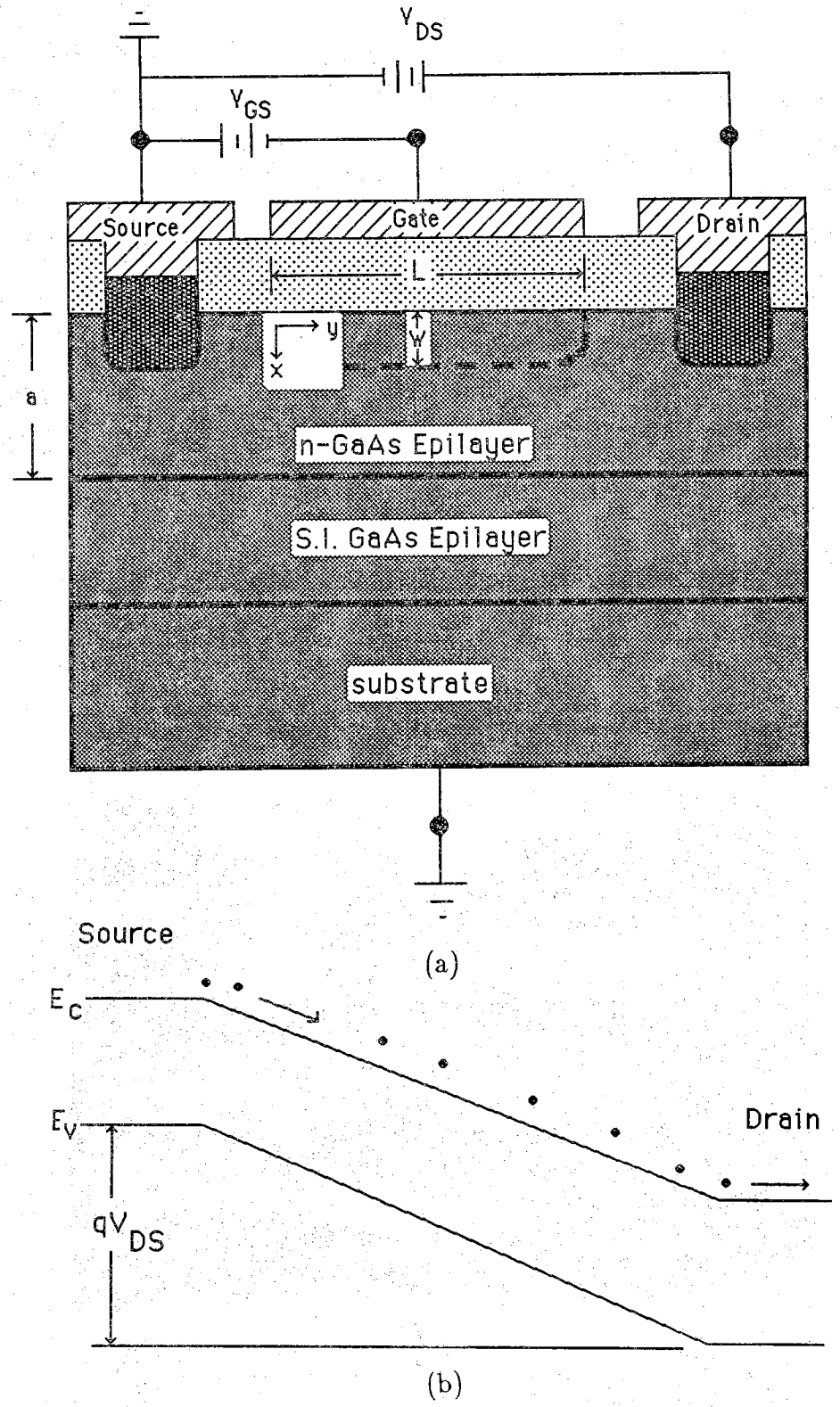

Figure 5.4. Cross sectional schematic of a MISFET showing (a) the voltage polarities of the source, drain, and gate. Part (b) shows the energy band bending from the source to the drain under a positive V_{DS}.

voltage is applied through a Schottky barrier. The effect of the barrier is taken into account by the incorporation of a built-in potential V_{bi} into the current equation. In the JFET, the same built-in voltage exists, but in this case, (V_{bi}) is caused by a p-n junction.) Because of the results of the MIS-C experimentation, it can be assumed that the depletion region under the gate in the ZnSe/n-GaAs FET is either in depletion or deep depletion. This assumption simplifies the analysis because it is not necessary to worry about the presence of an accumulation layer of electrons or an inversion layer of holes.

The derivation of I_D and other parameters for the long and short channel devices is given in appendix B with only the highlights recorded here. The derivation begins with the well known drift current equation, eqn. 5.8.

$$J=-q\mu_n N_D \frac{dV}{dy} \qquad 5.8$$

The symbols and their corresponding values are listed in Table 3. Here, we are only concerned with the current flow of electrons due to an electric field and can ignore the diffusion of minority carriers. The current density is assumed to be constant for any value of y. (x and y are the directions perpendicular and parallel to the interface, respectively.) Based on this assumption, the current is obtained by integrating the current density over the cross-sectional area of the device. The double integration results in equation 5.9.

$$I_D=Zq\mu_n N_D[a-W(y)] \qquad 5.9$$

W(y) (eqn. 5.10) represents the depletion region in the GaAs at a particular ideal gate voltage and drain voltage V(y). The drain current derivation is performed assuming an ideal gate voltage is applied across the MIS region, or in other words, that there is no initial energy band bending in the n-GaAs due to a metal-semiconductor work function difference or charges throughout the heterostructure. Non-idealities in the MIS region are taken into account by a flatband voltage as explained later on in the text.

$$W(y)=x_o'\left[1-\left(\frac{1+V_G'-V(y)}{V_\delta}\right)^{1/2}\right] \qquad 5.10$$

To simplify the current equation, equation 5.10 is substituted into equation 5.9 and then integrated over V(y). [V(0)=0V, the voltage at the source end of the gate and V(L)=V_D, the voltage at the drain end of the gate] The drain current for the transistor in the linear region of operation appears in equation 5.11.

$$I_D=\frac{Zq\mu N_d}{L}\left\{(a+x_o')V_D+\frac{2}{3}x_o'V_\delta\left[\left(1+\frac{V_G'-V_D}{V_\delta}\right)^{3/2}-\left(1+\frac{V_G}{V_\delta}\right)^{3/2}\right]\right\} \quad 5.11$$

$$V_D \geqq 0$$

$$V_P < V_G'-V_D < 0$$

V_P is defined as the voltage at the drain end of the gate required to cause the depletion region W(y=L) to equal the channel thickness (a). Although derived for a doped channel FET in deep depletion, equation 5.11 is remarkably similar to the I-V relationship found for other field-effect transistors [37]. The primary difference in the doped channel I-V equation is the presence of x_o' and V_δ which both arise due to the dielectric insulator (see Table 3).

When $V_G'-V_D$ is less than or equal to V_P, the conducting channel is pinched off at the drain end of the gate and the drain current saturates and ideally remains at a constant value for any further increase in V_{DS}. I_{Dsat} is found by substituting $V_{Dsat} = V_G'-V_P$ into equation 5.11 and simplifying.

$$I_{Dsat}=\frac{Zq\mu N_D}{L}\left\{(a+x_o')(V_G'-V_P)+\frac{2}{3}x_o'V_\delta\left(\frac{a+x_o'}{x_o'}\right)^3-\frac{2}{3}x_o'\left(1+\frac{V_G'}{V_\delta}\right)^{3/2}\right\} \quad 5.12$$

$$V_G'-V_D < V_P$$

In the saturation region, the parameter of interest is not so much the actual value of I_{Dsat} but rather how I_{Dsat} changes with V_G' (the small signal gain of the transistor). The transconductance is found by taking the derivative of equation 5.12 with respect to the ideal gate voltage; i.e.,

$g_m = \delta I_{Dsat} / \delta V_G'$.

$$g_m = \frac{Zq\mu N_D(a+x_o')}{L}\left[1-\frac{x_o'}{a+x_o'}\left(1+\frac{V_G'}{V_\delta}\right)^{1/2}\right] \qquad 5.13$$

Equations 5.11, 5.12, and 5.13 are derived assuming that the MIS gate is an ideal one with no initial band bending due to work function difference and-or the presence of charges at the interface or throughout the heterostructure. Because detailed information on surface state density is not known, the non-idealities that cause initial band bending in the GaAs are taken into account by including a flatband voltage in the ideal equations. V_{FB} is determined experimentally in this work and is incorporated in the transistor equations by replacing V_G' with V_G - V_{FB}, where V_G is the actual gate voltage applied to the device. Also, it should be noted that this expression for g_m is only valid if the surface state occupancy does not change significantly over the bias range of interest. At this point, we are ready to examine the experimental curves.

The I_{DS} versus V_{DS} characteristics for the 90μm and 45μm devices appear in Figures 5.5 and 5.6, respectively. These curves were taken using a Tektronix curve tracer with the transistor at room temperature in the dark. The curve tracer sweeps through each trace on the display at a frequency of 60Hz. The gate voltage begins at 0V and is stepped -0.5V per curve. As is seen in the figures, both curves show current saturation and complete cutoff of the channel. The pinchoff voltage for both transistors is between -2.0 and -2.5V.

Figures 5.7 and 5.8 are plots comparing the theoretical g_m of equation 5.13 and the experimental g_m versus V_{GS}. Notice in these diagrams, the gate-source voltage is plotted on the x axis as a positive quantity whereas the actual V_{GS} is a negative number. The experimental points are taken from the transistor curves at a V_{DS} of 16/10V for the 90μm/45μm devices, respectively.

Two important variables in equation 5.13 are the electron mobility and flatband voltage. The mobility parameter causes the transconductance curve to translate in the y direction (the more mobile the carriers, the larger g_m becomes) while the flatband voltage causes a translation in the x direction (the more positive V_{FB}, the less gate voltage is required to pinch off

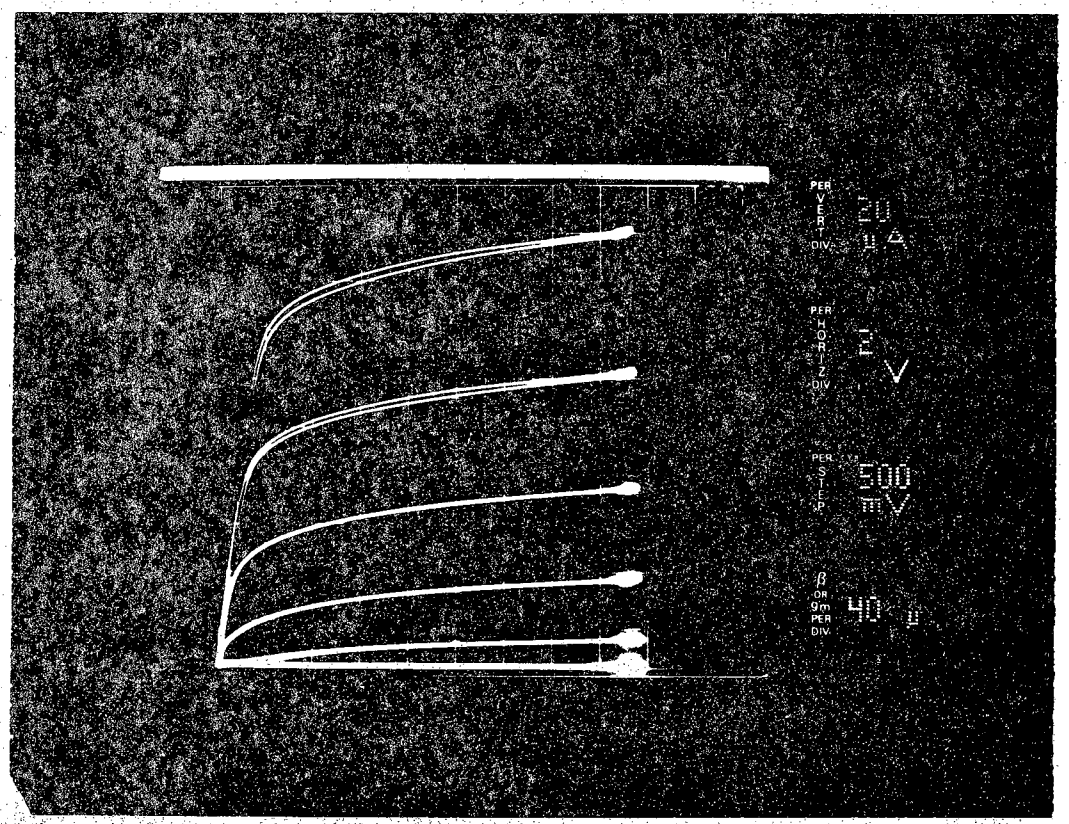

Figure 5.5. Room temperature I-V relationship for a 90μm MISFET in the dark. The gate bias is decreased by 0.5 volts per trace starting at 0V.

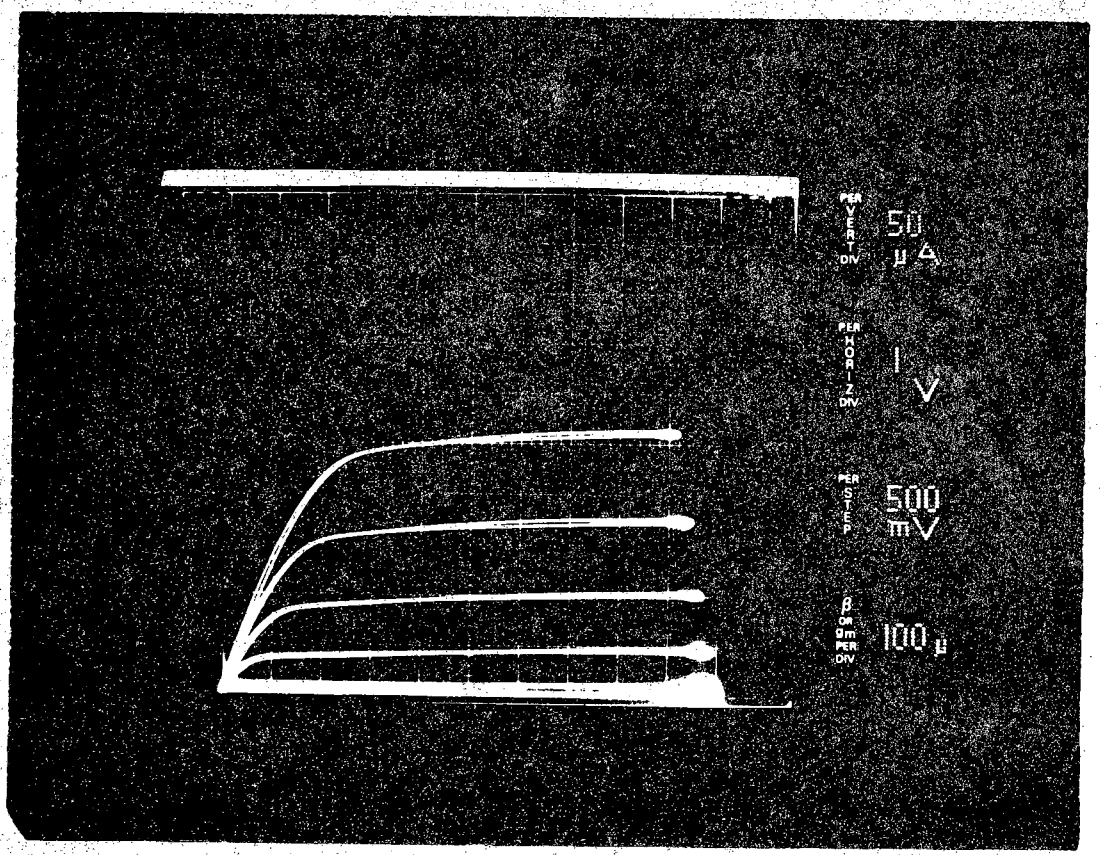

Figure 5.6. Room temperature I-V relationship for a 45μm MISFET in the dark. The gate bias is decreased by 0.5 volts per trace starting at 0V.

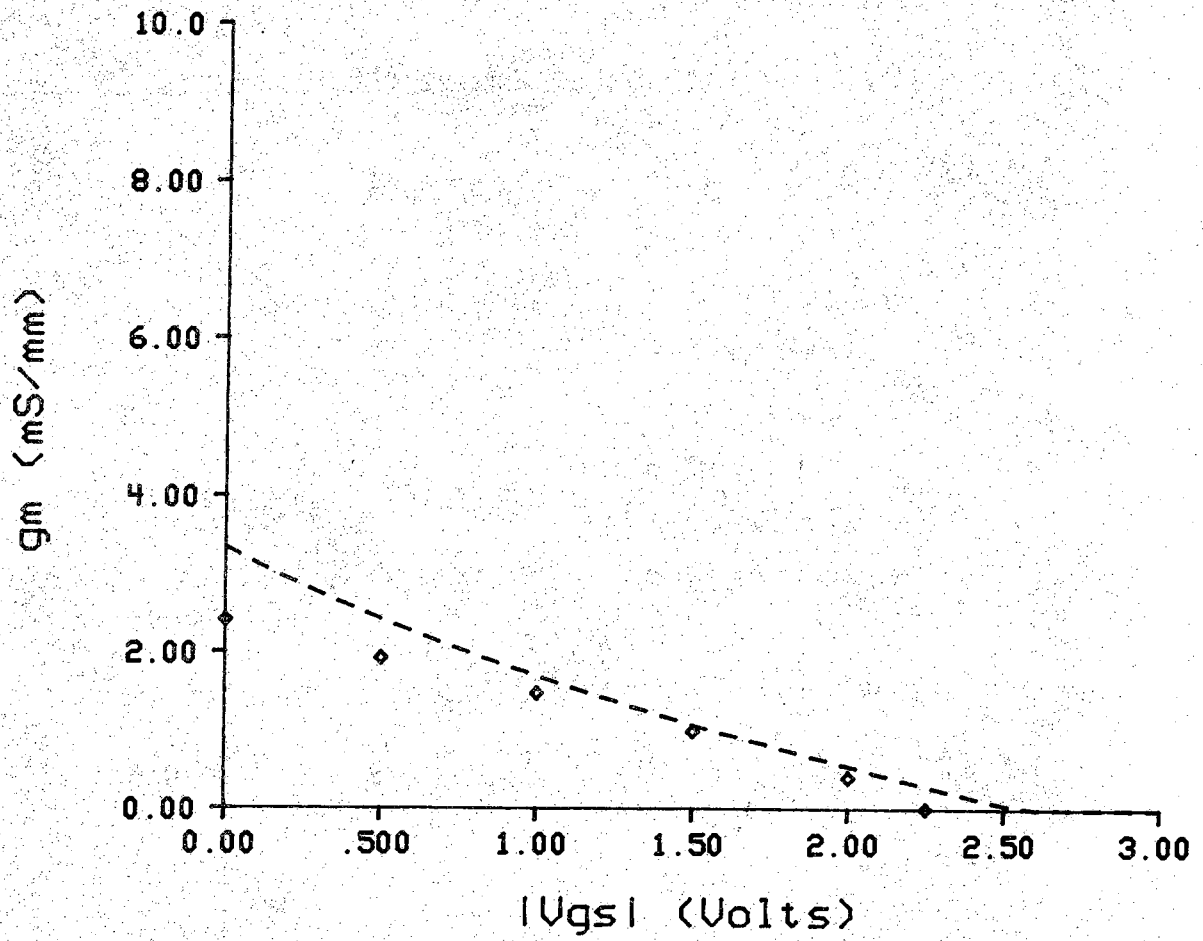

Figure 5.7. Transconductance versus V_{GS} for the 90μm device. The dashed line is the theoretical variation.

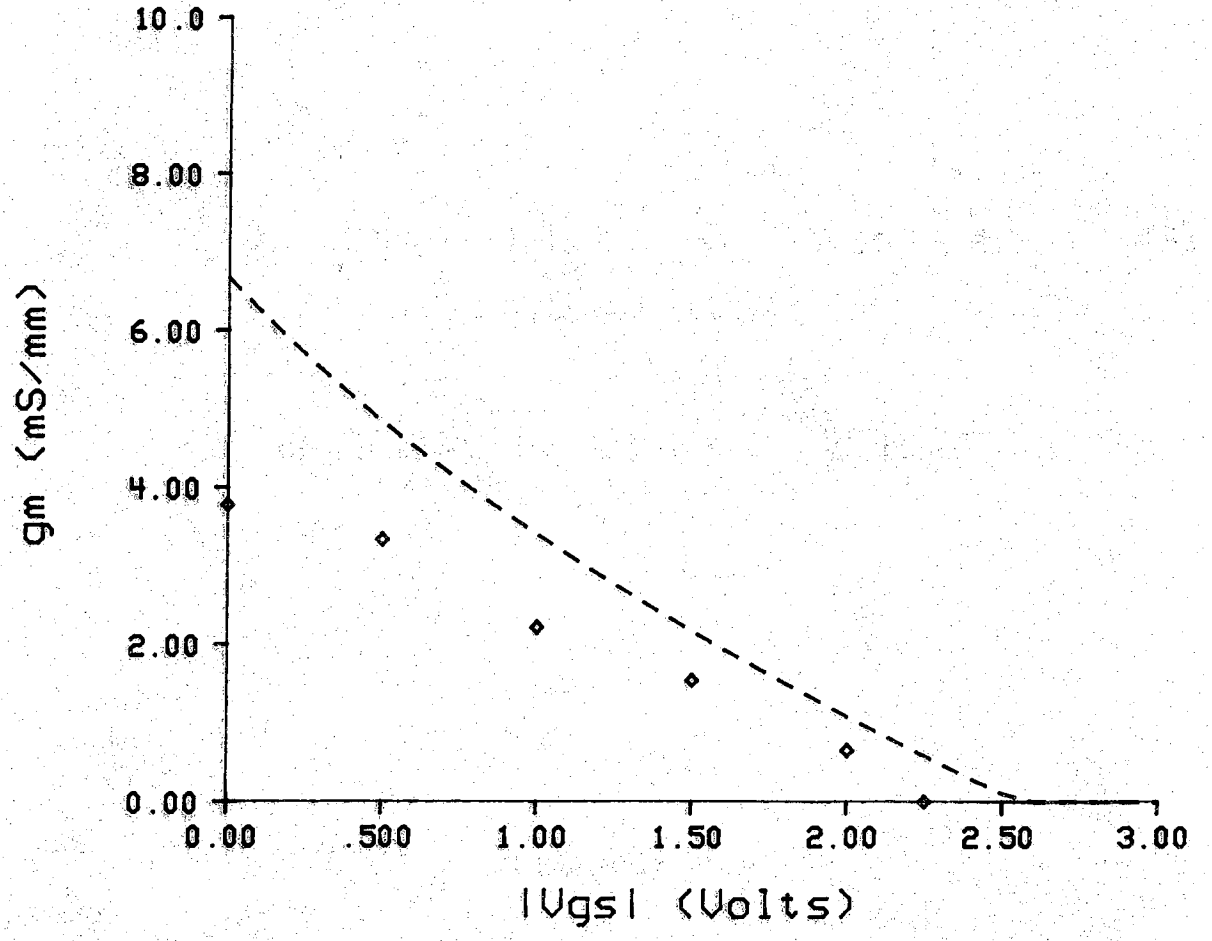

Figure 5.8. Transconductance versus V_{GS} for the 45μm device. The dashed line is the theoretical variation.

the channel.) The electron mobility is estimated from the background donor density of the n type GaAs epilayer. N_D is obtained from a $1/C^2$ vs V_{GS} plot using the formula,

$$N_D = \frac{2}{qK_s\epsilon_o}\left[\frac{-1}{d(1/C^2)/dV}\right] \qquad 5.14$$

The electron mobility is estimated from a μ versus N_D plot for GaAs given in reference 38. For N_D= 1-2x10^{16}cm^{-3}, the observed range of mobilities in commercially available GaAs is typically 3,200-4500cm^2/Vsec. (The mobility was estimated rather than measured due to difficulties in the experimental measurement. Fortunately, the theoretical transconductance curve agreed fairly well with the measured transconductance using the estimated mobility.)

The flatband voltage is calculated from a C-V characteristic of the gate capacitance appearing in Figure 5.9. The gate capacitance is measured with the Hewlett Packard LCR meter similar to the work cited in section 5.1. In this application, the source and drain contacts are tied together for the ohmic connection to the capacitor. The data in Figure 5.9 is taken in the dark at room temperature with the oscillator set at 15mV RMS and a frequency of 1MHz. The C-V curve shows depletion characteristics from +1.0V to -2.0V and then a rapidly decreasing C_{GS}. At -2.0V, the depletion region in the n-GaAs is beginning to contact the semi-insulating GaAs buffer layer, as is also observed in the cutoff characteristics in the FET curves. To calculate V_{FB}, equations 5.1-5.6 are first used to derive the width of the depletion region in the n-GaAs at zero bias (970Å). Next, V_G' in equation 5.10 is replaced with $V_G - V_{FB}$, V_G and V(y) are set equal to zero, and W(y) is replaced with 970Å. The ensuing solution of equation 5.13 results in a flatband voltage of 0.348V. The flatband voltage has a positive sign indicating that the energy bands in the GaAs are already bent into depletion at zero gate voltage. This value of V_{FB} is understood to be a very crude estimate because C_{GS} at 0V is very dependent on both the stray capacitance in the C-V measurement and the charge nature of the surface states at the ZnSe/n-GaAs interface.

The other parameters in equation 5.13 are Z, L, a and x_o. The channel dimensions Z and L are determined by microscope evaluation. Because of overetching, the channel width is 5μm smaller than the mask specification, but the gate length is the same as specified on the mask, Figure 4.1. The

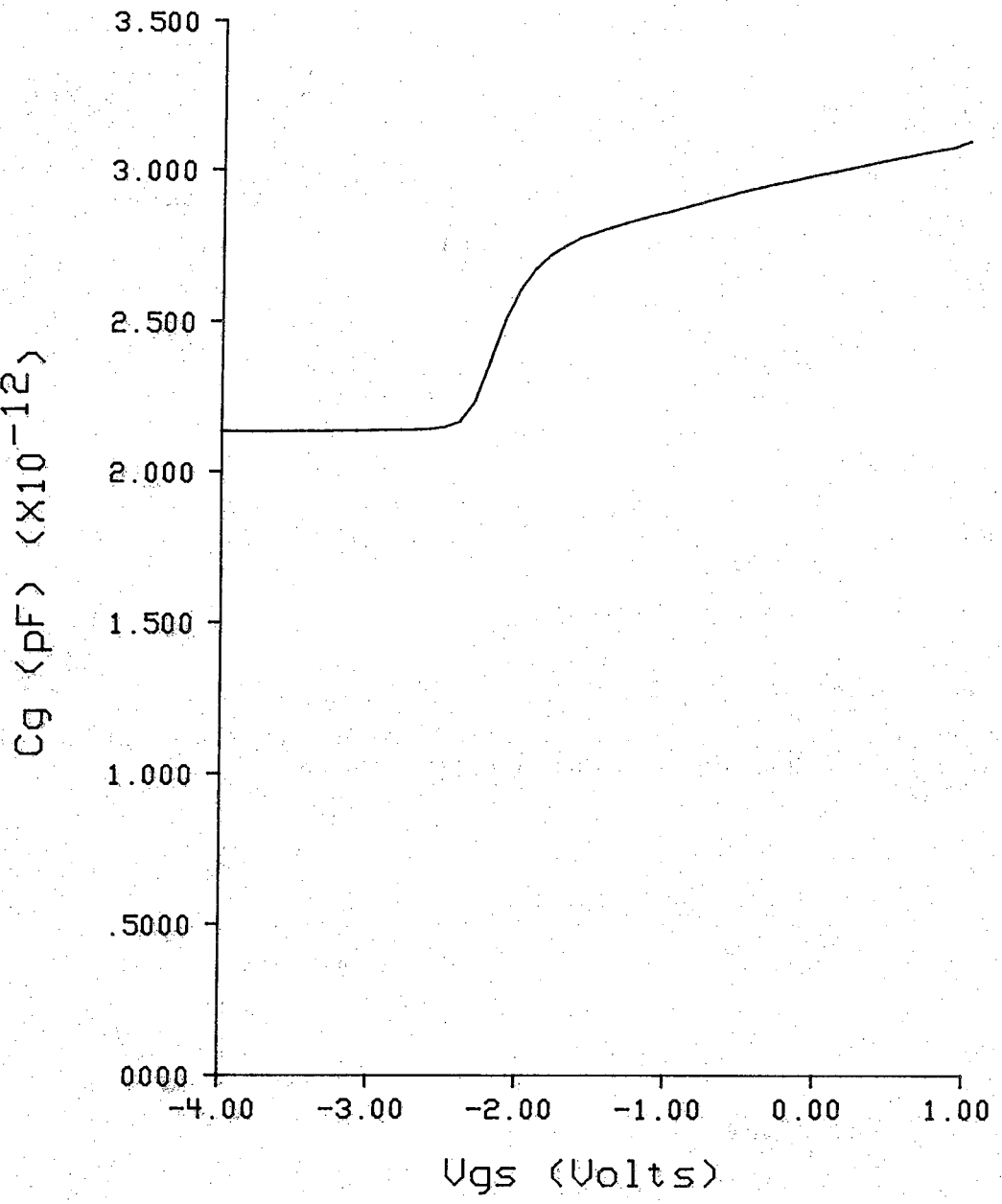

Figure 5.9. Gate capacitance ($4.5x10^{-5}cm^2$) measured at 1MHz in the dark showing depletion characteristics and pinchoff to the S.I. GaAs at -2.25V.

built-in channel thickness (a) and the ZnSe thickness (x_o) are estimated to be 4000Å and 1000Å, respectively, from the known MBE growth conditions. The ZnSe thickness has also been confirmed from cross-sectional TEM images.

The theoretical g_m calculated using these parameters as summarized in Table 3 agrees fairly well with the measured transconductance for both devices. Moreover, a portion of the discrepancy between the measured and theoretical g_m's can be accounted for by the series resistance of the transistors. Because these transistors have large source-drain to gate spacings of 20μm, much of the drain-source voltage appears outside of the gate region. If the n-GaAs resistance is known, the intrinsic transconductance g_m' can be deduced from equation 5.15 [39].

$$g_m' = \frac{g_m}{1 - R_s g_m} \qquad 5.15$$

where R_s is the resistance between the gate and the source. The theoretical transconductance in equation 5.13 does not include series resistance and therefore, should be compared to g_m' instead of g_m.

The total series resistance of the GaAs as a function of channel length is given in Figure 5.10. This curve is found experimentally using the test resistors on the die. The figure shows two curves, the maximum and minimum series resistance of all the resistors tested. R_s includes the contact resistance R_c which can be estimated from extrapolating Figure 5.10 to L=0 and calculating R_c from equation 5.16.

$$R_s = 2R_c + R_\square \frac{L}{W} \qquad 5.16$$

$R_\square$ is the sheet resistance of the n-GaAs. The y intercept of the maximum R_s versus L plot is 650Ω. Hence, R_c is 325Ω or in units of ohms times the gate width, R_c = 16.25Ωmm. Typical values of ohmic contact resistance for n-GaAs are 0.1-5Ωmm [40]. The transistors in this work frequently had poor ohmic contacts with high contact resistances, especially for devices with small contact dimensions. In several fabrication runs, only the largest source-drain contact spacings showed ohmic conduction with most of the small contacts displaying rectifying behavior similar to Figure 4.5. The failures appeared to be caused by thin film residues left by the ZnSe chemical etch that inhibited the diffusion of Ge during the Au-Ge alloy. In

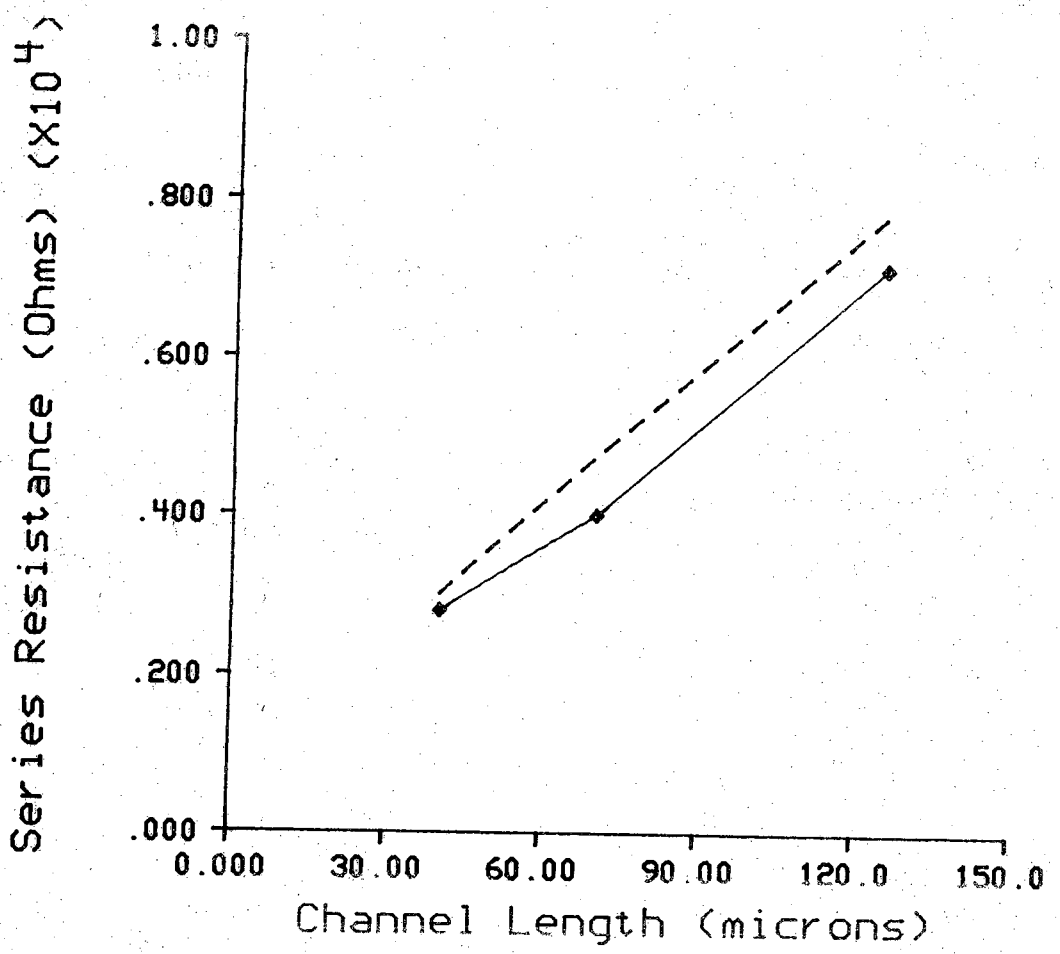

Figure 5.10. Series resistance vs. channel length for the n-GaAs. The dashed/solid lines are the max/min experimentally determined resistance values.

the final fabrication run yielding the transistors reported here, the devices had a very clean source-drain etch which resulted in the highest number of successful devices of all the fabrication attempts. Hence, as is discussed in Chapter 4, the source-drain etch followed by the Au-Ge evaporation and alloy appear to be the most critical steps in the successful fabrication of field-effect devices. Also, to minimize contact resistance (R_c) most GaAs ohmic contacts are made with layers of gold, germanium and nickel. The nickel apparently helps in the diffusion of Ge into the GaAs [35]. The use of Au-Ge-Ni layers for ohmic contacts is not necessary for exploratory device fabrication as is reported here but is essential for obtaining the optimal device performance.

Both the long channel devices have source-gate spacings of 20μm which were also confirmed from microscope examination. From Figure 5.10 a series resistance of 2000Ω is deduced which is expected for the doping and channel thickness of the device. Figure 5.11 and 5.12 show plots of g_m' versus V_{GS} for the 90μm and 45μm devices, respectively. Notice a close agreement between theory and the corrected g_m for the 90μm device. As the gate length gets smaller, the series resistance plays a larger role in reducing the transconductance which possibly explains the variance in the parameters for the 45μm device. Furthermore, it is apparent in Figure 5.13 that the corrected transconductance does not vary smoothly with the gate voltage which possibly implies that the surface state occupancy may be changing with the gate potential.

Another factor that could contribute to a lowering of the transconductance is parallel conduction in the ZnSe. A conductive insulator contributes a component to the drain current that is primarily independent of the gate potential. The stray leakage current in the insulator diminishes the modulating effect of the gate since this current originates outside of the n-GaAs channel. However, parallel conduction in the ZnSe is not considered as contributing to the low transconductance, though because resistivity measurements of thick epitaxial ZnSe, grown under similar conditions (Chapter 2), have demonstrated resistivity parallel to the interface greater than $10^4\Omega$-cm. A simple calculation of $I=V/R$ with $R=\rho L/x_o W$ results in a ZnSe current of 9nA at a V_{DS} of 16V for the 90μm device. Compared to the zero bias saturation current of the device (180μA), the parallel conduction current in the ZnSe appears to be negligible.

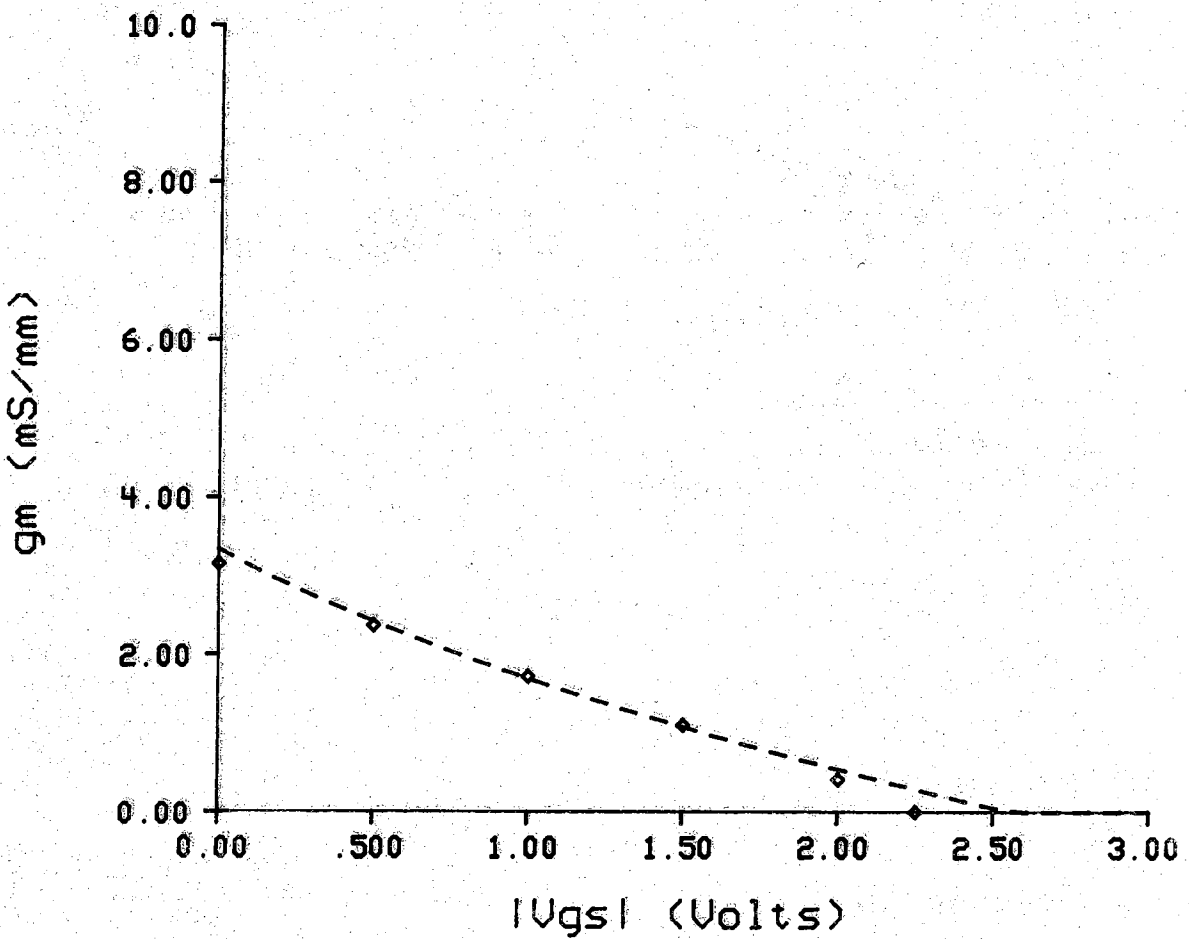

Figure 5.11. The transconductance versus V_{GS} for the 90μm transistor taking into account the series resistance between the source and the gate.

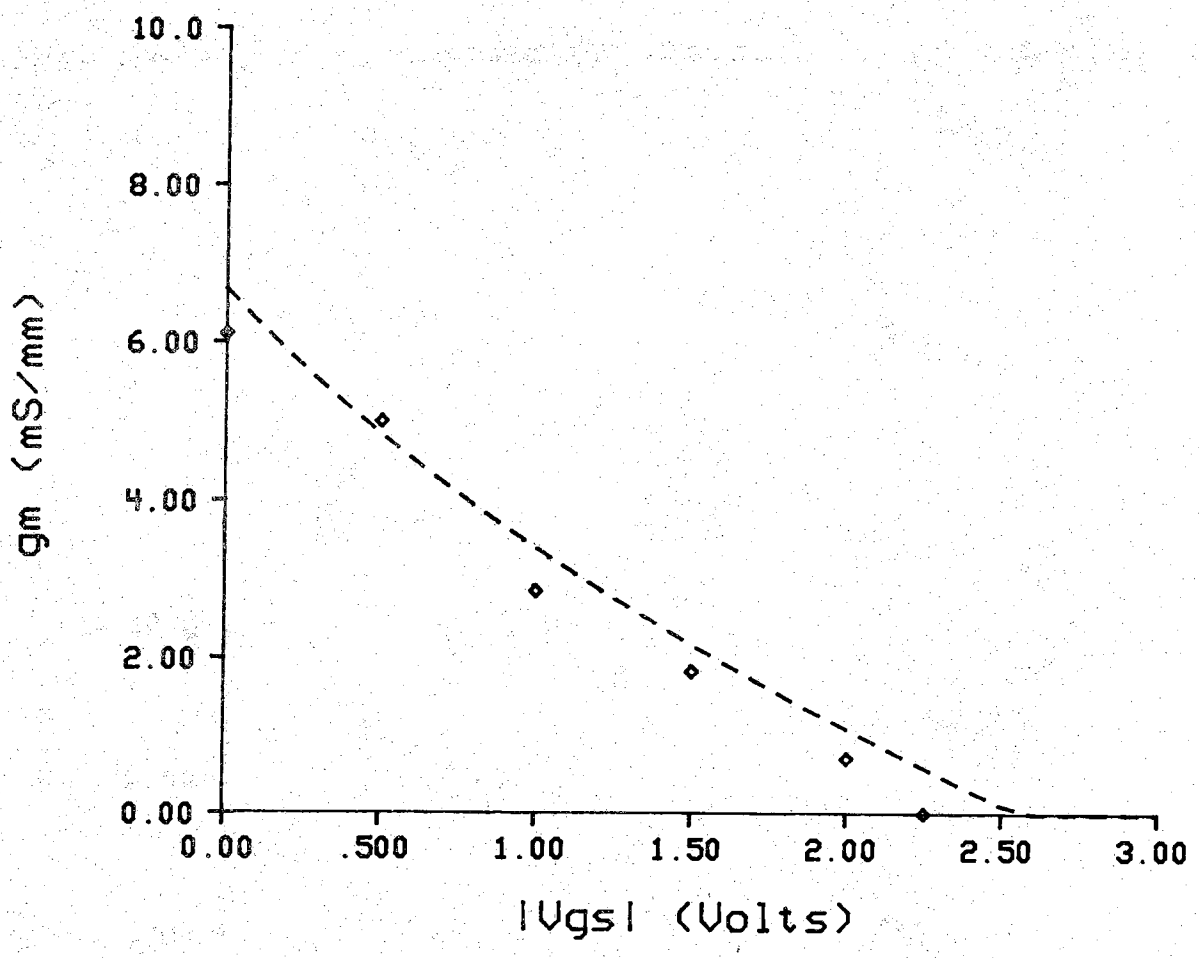

Figure 5.12. The transconductance versus V_{GS} for the 45μm transistor taking into account the series resistance between the source and the gate.

5.2.2 Short Channel Devices

As the gate length in a FET decreases, the electric field across the channel increases. Even with no metal gate, the drain current will level off because the velocity of the carriers saturates [41]. In a short channel transistor, the drain current saturates not because the channel is pinched off under the gate but rather because the velocity of the carriers reach a maximum value under the high electric fields (for GaAs, $v_{max}= 2x10^7$cm/sec at an electric field of approximately 3500V/cm). The gate voltage still modulates the carrier density in the GaAs somewhat, but the maximum drain current is primarily limited by the rate at which electrons can move through the channel.

A modified I_D versus V_{DS} equation describes the saturation drain current in the limit of high electric fields. For total velocity saturation under the gate,

$$I_{Dsat}=qv_sZ(a-W)N_D \qquad 5.17$$

where v_s is the saturation velocity of the electrons in the GaAs. To calculate g_m versus V_{GS}, $V_{Dsat} = \mathscr{E}_{cr}L$ is substituted into the equation for W and the derivative with respect to V_{GS} in eq. 5.17 is again performed resulting in equation 5.18.

$$g_m=v_sZC_o\left[1+\frac{V_{GS}-V_{FB}-V_{Dsat}}{V_\delta}\right]^{-1/2} \qquad 5.18$$

The transconductance for an inversion channel MOSFET under velocity saturation is given by v_sZC_o which is essentially the same as the transconductance given in equation 5.18. The square root term remains very close to one because V_{Dsat} is a relatively small voltage in the velocity saturated transistor. Hence, the velocity saturated transistor shows an almost constant g_m and will display a family of I-V curves that are evenly spaced.

Equations 5.17 and 5.18 are applicable to a transistor with total velocity saturation under the gate which is not the case for the transistors fabricated in our laboratory. (Most researchers consider the above equations valid for gate lengths less than 2μm or less [41]. The smallest gate length in this work is 2μm.) This assumption gives a rough estimation, though, of the behavior of g_m in the presence of high electric fields and helps in distinguishing the difference between long and short channel devices.

The I_D versus V_{DS} curves for the 20μm, 5μm, and 2μm devices appear in Figures 5.13, 5.14, and 5.15, respectively. Notice that in each device, the change in I_D for various gate potentials is almost the same from curve to curve. One would not expect the 20μm device to be velocity saturated; it may exhibit constant g_m characteristics because of current crowding at the drain. The 0V g_m for the 20μm and 5μm devices are 6.0mS/mm and 6.7mS/mm, respectively. The intrinsic transconductance, corrected for series resistance for the 5μm gate length device, is 16.7mS/mm. In the smaller devices, the source-to-gate spacing is two to three times larger than the gate length and hence can dramatically effect the intrinsic transconductance. By changing R_s in equation 5.15, g_m' can be varied considerably. In future small channel devices the gate to source-drain spacings should be minimized in order to better characterize the gain of the ZnSe/n-GaAs transistor.

A plot of g_m' vs V_{GS} for the 2μm device appears in Figure 5.16. The two dashed curves represent the theoretical plot of g_m versus V_{GS} using the long channel approximation (top) and the velocity saturation model (bottom). Notice that the two theoretical curves intersect, showing that the transistor operates in both modes depending on the gate biases. The experimental points do not display a smooth variation and possibly indicate again that charge trapping in the heterostructure may affect the transconductance.

5.2.3 MIS Interface and Gate Considerations

Some of the most important information concerning the operation of a field-effect transistor may be found by studying the electrical characteristics of the gate region. The parameters of interest are the structure of the energy bands in the heterostructure (E_C, E_V, and E_F), the current conduction in the gate region, the breakdown of the heterostructure under high electric fields, and the nature of charge trapping throughout the MIS device. This section discusses these characteristics by examining the capacitance-voltage and current-voltage profiles of the gate capacitor and by further examination of the FET curves.

As in the MIS-C experiments in section 5.1 and detailed in reference 36, the gate of the field-effect transistor may be treated as a capacitor and the corresponding C-V and I-V characteristics may give information about the structure of the energy bands in the n-GaAs. Figure 5.9 is typical of the gate capacitance for the ZnSe/n-GaAs FETs. From the 0V capacitance measurement, an initial depletion width in the n-GaAs of 970Å is calculated

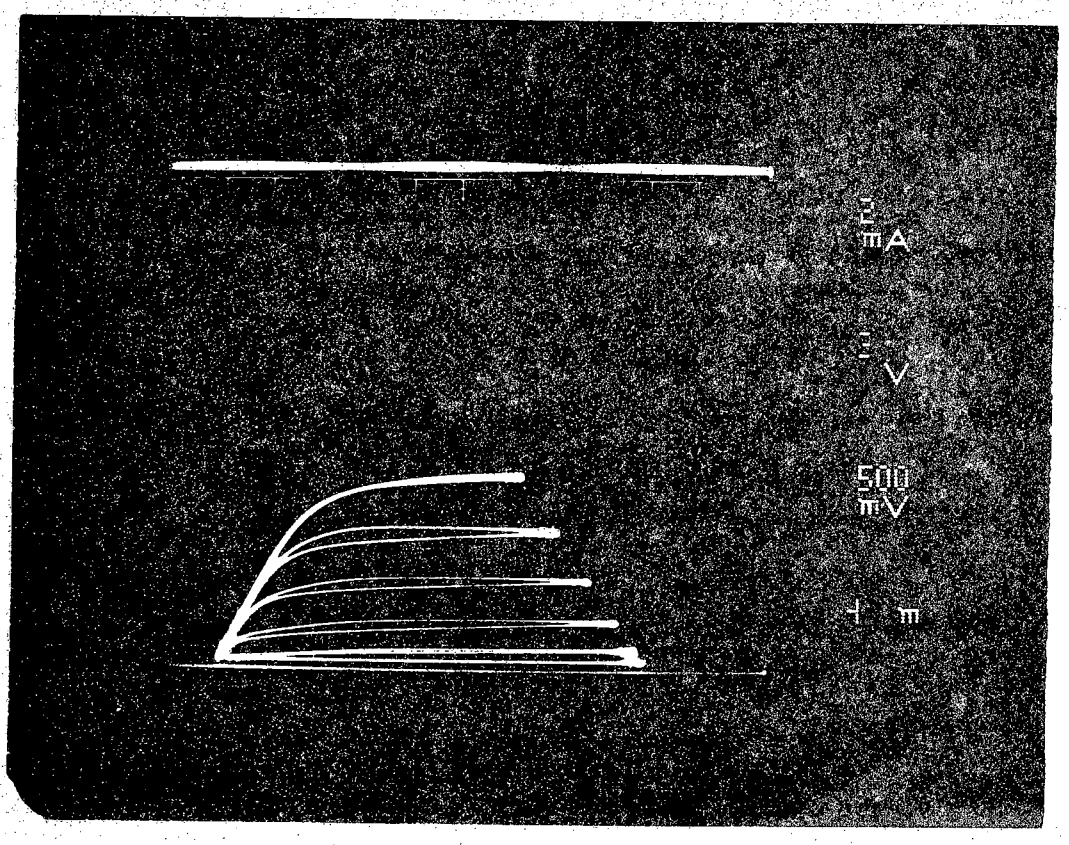

Figure 5.13. Room temperature I-V relationship for a Box FET with a gate length of 20μm. The gate bias is decreased by 0.5 volts per trace starting at 0V.

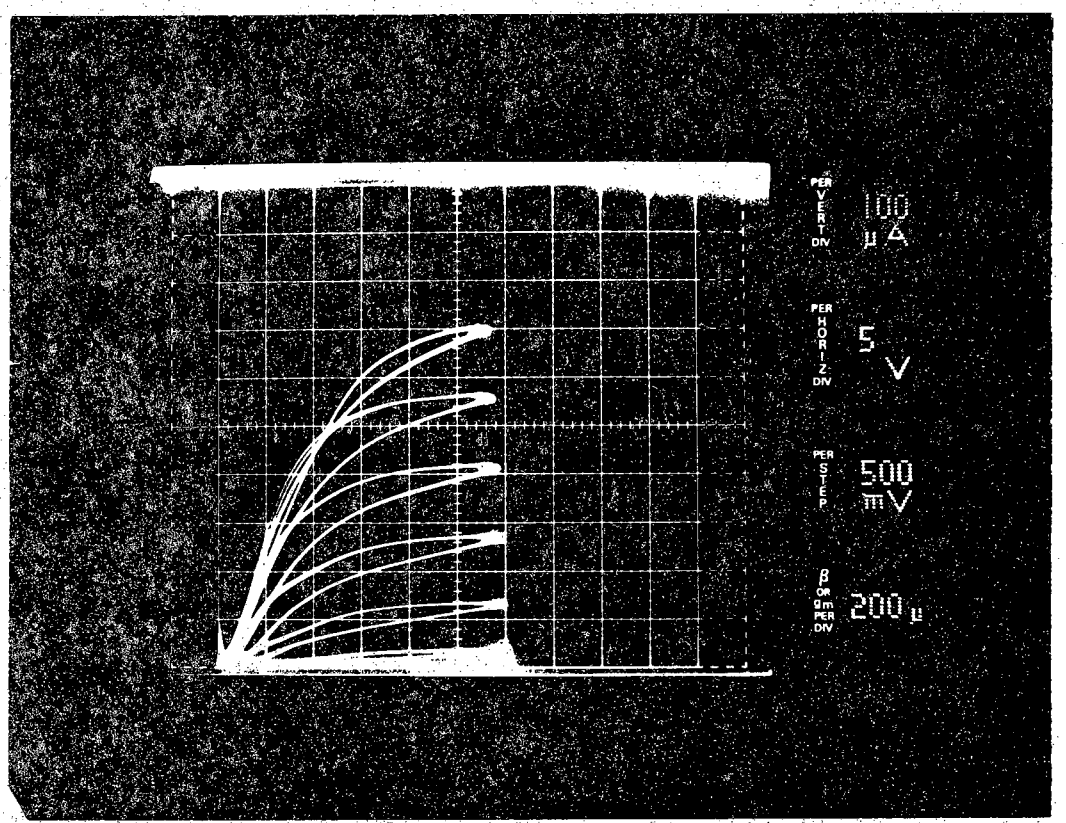

Figure 5.14. Room temperature I-V relationship for a 5μm device showing device operation out to V_{DS} of 30V. The gate bias is decreased by 0.5 volts per trace starting at 0V.

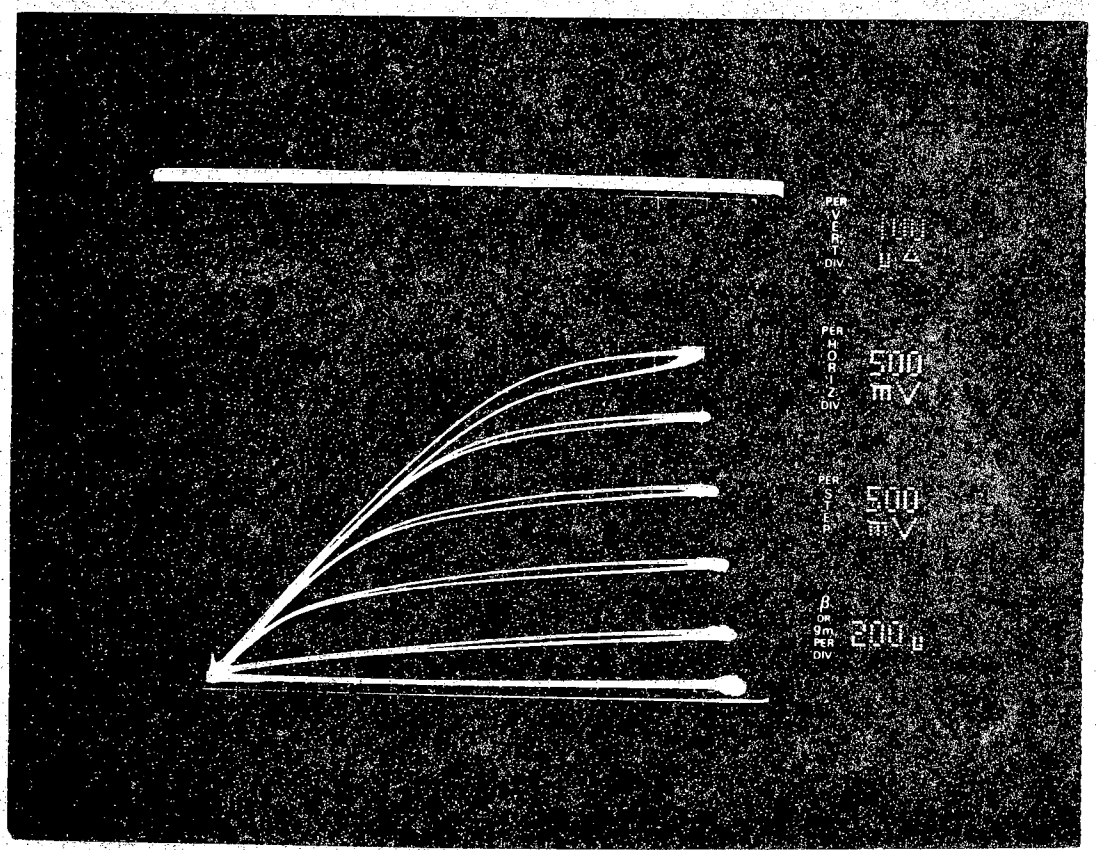

Figure 5.15. Room temperature I-V relationship for a 2μm device. The gate bias is decreased by 0.5 volts per trace starting at 1.0V.

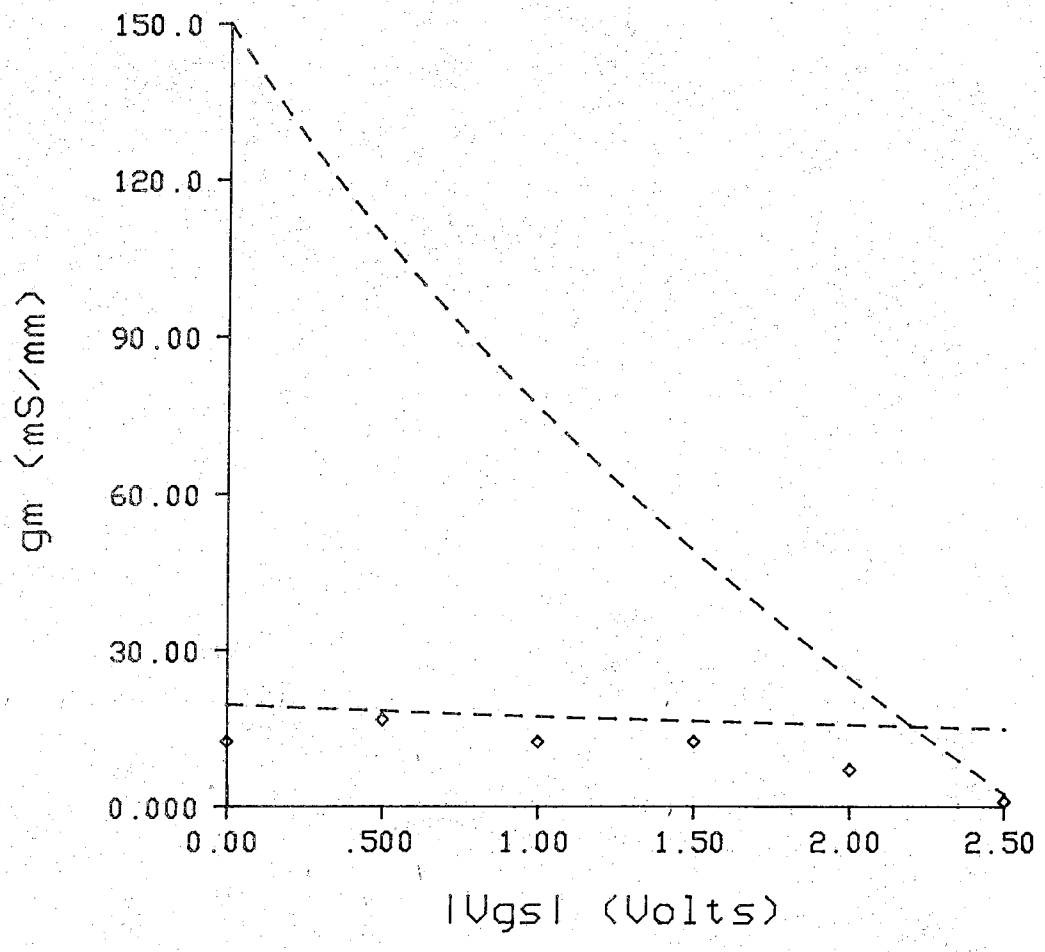

Figure 5.16. Transconductance versus gate voltage for the 2μm device. The top dashed line represents the theoretical calculation using a constant mobility model while the bottom curve uses a saturated velocity model.

in section 5.2.1. Using equation 5.6, the position of the surface potential at the ZnSe/n-GaAs interface is determined to be 0.1V. (As a reminder, the surface potential $q\phi_s$ is the value of the intrinsic energy level at the interface with respect to the value of the intrinsic energy level in the bulk of the GaAs. In effect, $q\phi_s$ represents how much the energy bands are bent at the insulator-semiconductor interface.)

As the capacitor is swept by a negative gate voltage, the energy bands in the n-GaAs are bent until $q\phi_s$ is at least equal to two times $q\phi_f$ (section 5.1). $2q\phi_f$ is used as the final position of the surface potential for comparison reasons. As soon as the capacitor goes into deep depletion ($q\phi_s > 2q\phi_f$), the device is no longer in equilibrium and the Fermi level moves upward in the GaAs band gap at the interface. We want to compare the beginning and ending $q\phi_s$ values with respect to the same stationary Fermi level and therefore must evaluate the MIS-capacitor in equilibrium. The value of $2\phi_f$ for this device is calculated to be approximately 1.1V. Subtracting the initial and final values of $q\phi_s$ indicates that the surface potential and correspondingly the conduction and valence bands are bent by approximately 1V during the sweeping of the gate voltage.

The above calculations indicate that the surface potential is modulated over most of the GaAs band gap during the operation of the device. This calculation is a preliminary evaluation and should be considered in this regard. The initial and final positions of the surface potential are suspect to the accuracy of the capacitance measurement. A field-effect transistor is not designed to be studied as a MIS-capacitor. The equivalent model for this measurement is actually the two capacitors of the heterostructure in series with a voltage controlled resistance. Since the LCR bridge measures the total impedance and reports the imaginary part as the capacitance, the changing series resistance will affect the C-V curve. As is evident in Figure 5.9, the depletion part of the curve does not look like a typical capacitor in depletion, and this distortion may be explained by the varying series resistance. Nontheless, the capacitance-voltage and transistor characteristics both suggest that the Fermi level at the ZnSe/n-GaAs interface can be modulated over the middle portion of the GaAs band gap [13] which is a very encouraging result.

The second gate parameter of concern is the flow of current through the heterostructure for different gate voltages. The current-voltage curve of the gate region for the 45μm device ($A_G = 2.25 \times 10^{-5} cm^2$) appears in Figure 5.17.

This curve is taken in the dark at room temperature using the Hewlett Packard picoammeter. J_F represents the forward bias current and J_R represents current observed under negative voltages which is the voltage range of interest in the doped channel transistor. Figure 5.17 shows that the reverse bias gate current is less than or equal to 3nA for the operating voltage of the transistor suggesting that gate leakage in these devices is minimal. As is expected in a semiconductor heterostructure, the gate carries substantial current in forward bias. The turn on voltage for the devices reported here are typically between 0.5V to 1.75V. The variance in the turn on voltage and the nature of the forward bias current is not well understood and the reader is referred to reference 36 for a more in-depth discussion.

Another important gate parameter in a field-effect transistor is the reverse bias voltage across the gate-drain region that causes substantial current to flow from the gate to the drain. This phenomenon known as the gate-drain breakdown is characterized by a voltage V_{GDBR} and is similar to the reverse bias breakdown of a p-n junction under high electric fields called avalanche multiplication. In the gate breakdown of the transistor, the electric field in the n-GaAs at the drain end of the gate becomes very large (KV/cm) under the combined influence of the negative gate voltage and the positive drain voltage. Electrons entering from the gate (the 3nA leakage current, perhaps) are accelerated by the high electric field and gain kinetic energy greater than the energy of the band gap. When these "high energy" electrons scatter with the atoms in the n-GaAs, bound electrons in the atoms are knocked free and are consequently added to the current. The gate current rises quickly as more and more electrons collide with atoms releasing free electrons, hence multiplying the current from the gate to the drain.

The gate-drain breakdown voltage is important because it determines the maximum voltage that can be applied to the transistor and, ultimately, the maximum output power of the device ($P = IV$). The concern in field-effect transistor design is how to maximize this output power. Two possibilities exist; increase the channel conduction and-or increase the gate-drain breakdown. The easiest parameter to change is to increase the channel conduction. In MESFET technology, however, both theoretical analysis [42] and device experimentation [43] have shown that the breakdown voltage is inversely proportional to the product of the doping level (N_D) and the active layer thickness (a), i.e. the channel conduction (N_Da). Hence, a dilemma exists when trying to increase the power. The

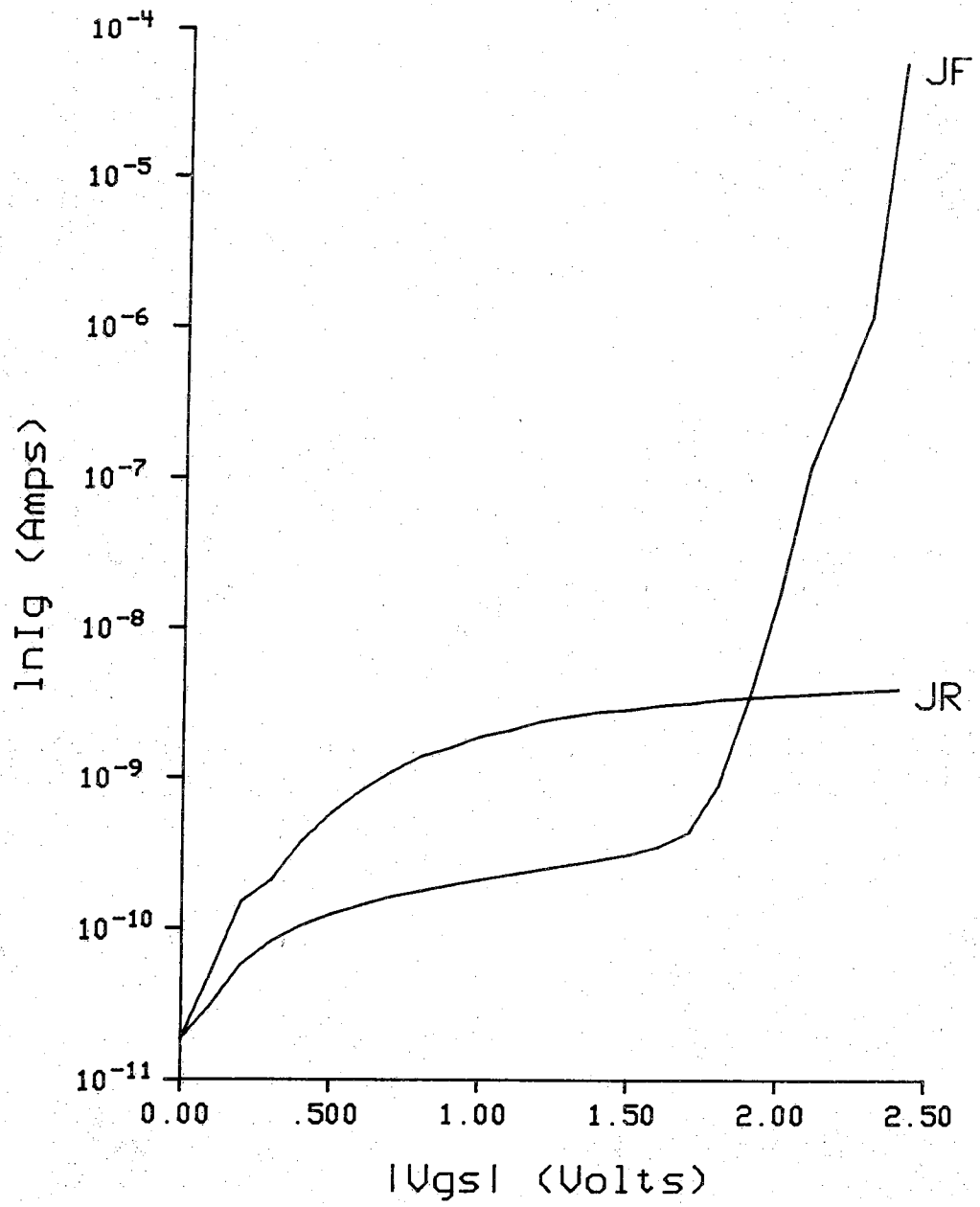

Figure 5.17. The gate current for the 45μm device (A_G=2.25x10^{-5}cm^2) at room temperature in the dark. J_F/J_R are the forward and reverse bias currents, respectively.

current may be increased by increasing N_D or a but these changes in turn lower V_{GDBR}. The output power, as a result, increases very little.

The second alternative is to increase the gate-drain breakdown which can be done by using an insulating dielectric between the semiconductor and the gate electrode. Because electric field decreases with distance, by moving the gate charge farther away from the charge in the GaAs channel (N_D^+), the electric field at a given operating voltage can be reduced. The same channel conduction can be maintained while increasing V_{GDBR}, hence increasing the power. For very good insulators as is the case in the silicon MOS transistor, the improvement in breakdown voltage is so significant that the channel conduction can also be increased which further increases the output power of the device.

The gate-drain breakdown voltages for six different transistors appear in Table 4. The breakdown voltage is measured in the dark at room temperature except for the 2μm device which was measured at 77 °K. The breakdown voltage is determined by first biasing the transistor with a complete I-V family of curves. Next, the drain to source voltage is increased until the bottom curve begins to carry a substantial amount of current (the breakdown is usually very sudden with the bottom trace breaking down first). The gate-drain breakdown voltage is then equal to $V_{GD}=V_{DS}-V_{GS}$. Since $V_{DS} > 0$ and $V_{GS} < 0$, the voltage across the gate-drain region is the positive sum of the absolute values of the pinchoff voltage and V_{DS} at breakdown. (In this device, it is simply V_{DS} plus at least 2.0V.)

As is seen in Table 5, the breakdown voltages range from 30-42V at room temperature. Except for the 45μm device, the breakdown voltages tend to decrease as the gate width decreases. As the dimensions between the gate and drain shrink, the electric field increases for the same gate potential.

The gate-drain breakdown voltages seem very high, but when compared with a theoretical curve of V_{BR} vs N_D for a one-sided abrupt p-n junction, V_{GDBR} seems reasonable. The reverse bias voltage in a p-n junction for avalanche breakdown is approximately 40-50V for $N_D = 1.5\text{-}2\text{x}10^{16}\text{cm}^{-3}$ [41].

Because the channel conduction in the transistor reported in this work is very small, it is difficult to compare these breakdown voltages to the breakdown voltages reported for GaAs transistors that use other insulators. For example, (Al,Ga)As/GaAs has demonstrated a gate-drain breakdown of

Table 4. Gate to drain breakdown voltages for various gate lengths.

Gate Length (μm)	V_{BRGD}
90	35
45	42
20	35
10	32
5	30
2	25

19-20V with $N_D=3.5x10^{17}cm^{-3}$ at a channel width of 2000Å [9]. In this work, the channel was highly doped in order to maximize the output power through both an increase in channel conduction and V_{GDBR}. MESFET research has also produced experimental data for GaAs transistors. For channel conduction of $7x10^{12}cm^{-2}$ (N_Da) typical breakdown voltages are 8-15V [43]. (The N_Da product gives a channel conduction assuming that the doping is uniform throughout the channel. This assumption is rarely the case, and as a result the N_Da formula is only meant as an approximation in order to give a means of comparing different field-effect transistors. To calculate the channel conduction exactly, the donor density profile $N_D(x)$ is integrated over the channel length.) Compared to the transistor in reference 9 where N_Da is approximately the same, the gate-to-drain breakdown voltage has apparently improved with the use of the (Al,Ga)As as a GaAs "insulator". The N_Da product for ZOOEG320-7 is $6x10^{11}cm^{-3}$ which is over ten times less than the conduction in the (Al,Ga)As/GaAs transistor and is also too low to compare with the work in reference 43.

The final consideration of the electrical properties of the ZnSe/n-GaAs heterostructure is a discussion of the looping observed in the FET characteristics. Both the small and large channel devices exhibit looping in the I_D versus V_{DS} curves indicating the presence of some charge trapping. The hysteresis occurs because the occupancy of charge storing traps changes during the operation of the device. For example, suppose electrons in traps somewhere in the heterostructure recombine as the transistor is swept from 0V out past V_P. When the drain voltage is reduced towards 0V, the reduction in negative charge causes the depletion width in the n-GaAs to widen increasing the drain current for the same V_{DS} and V_{GS}.

The source of charge trapping in the ZnSe/n-GaAs heterostructure is relatively unknown at this point of experimentation. One would first suspect the ZnSe/n-GaAs interface because the fabrication of this heterostructure involves an interrupted growth, and we did observe an oxygen peak on the n-GaAs epilayer surface. Also, the MIS-C work has some evidence supporting the presence of surface states at the ZnSe/n-GaAs interface. However, the n-GaAs/S.I. GaAs interface as well as the GaAs and ZnSe layers themselves should also be considered as sources of traps. There were substantial GaAs growth difficulties during the production of these films, as is evident from the unsuccessful fabrication of the other two depletion mode devices because of problems with the GaAs. The details of charge trapping is

not well understood at this time but a few of its characteristics with regards to the doped channel FETs can be noted.

As is expected, when the transistor is swept at a higher frequency the looping in the I-V curves disappears. For sampling rates above 60Hz (the normal sweep rate of the curve tracer is 60Hz with the next setting being 120Hz), the looping is not present. The surface states apparently can not fill or empty at high frequencies as is also observed in the MIS-capacitor work. I-V looping is rarely discussed in the literature because many FETs are operated in the MHz frequency range where the charge trapping is not a consideration. The ZnSe/n-GaAs doped channel FETs could also work very well in microwave applications where the frequency of the A.C. signal is high enough to keep the occupancy of the traps fixed.

When the heterostructure is cooled to 77 °K, the looping is not present in the dark. Figure 5.18 shows the FET curve for the 2μm device at 77 °K in the dark. The I-V display shows no looping suggesting that the traps are frozen out at 77 °K. For low temperatures in the dark, the trapped electrons do not have enough energy to escape the states and no photo or thermally generated holes to recombine with in order to neutralize their charge. If light is now applied to the sample, Figure 5.19, the looping again appears. Holes are now present for the trapped electrons to capture, changing the charge content of the heterostructure. Also, the spacing between the I-V curves is reduced suggesting that some of the gate voltage is now being terminated on holes at the interface rather than positive donors in the channel and hence, reducing the transconductance.

The characterization of the electrical nature of the ZnSe/GaAs interface is in its infancy. The results of the doped channel field-effect transistors are very encouraging showing modulation of the Fermi level at the interface for both long and short channel devices. Although looping is present in the I-V curves, it is not anymore prevalant than looping seen in other GaAs based transistors [44] and hopefully, with improved growth techniques, the traps that are contributing to the charge storage can be eliminated.

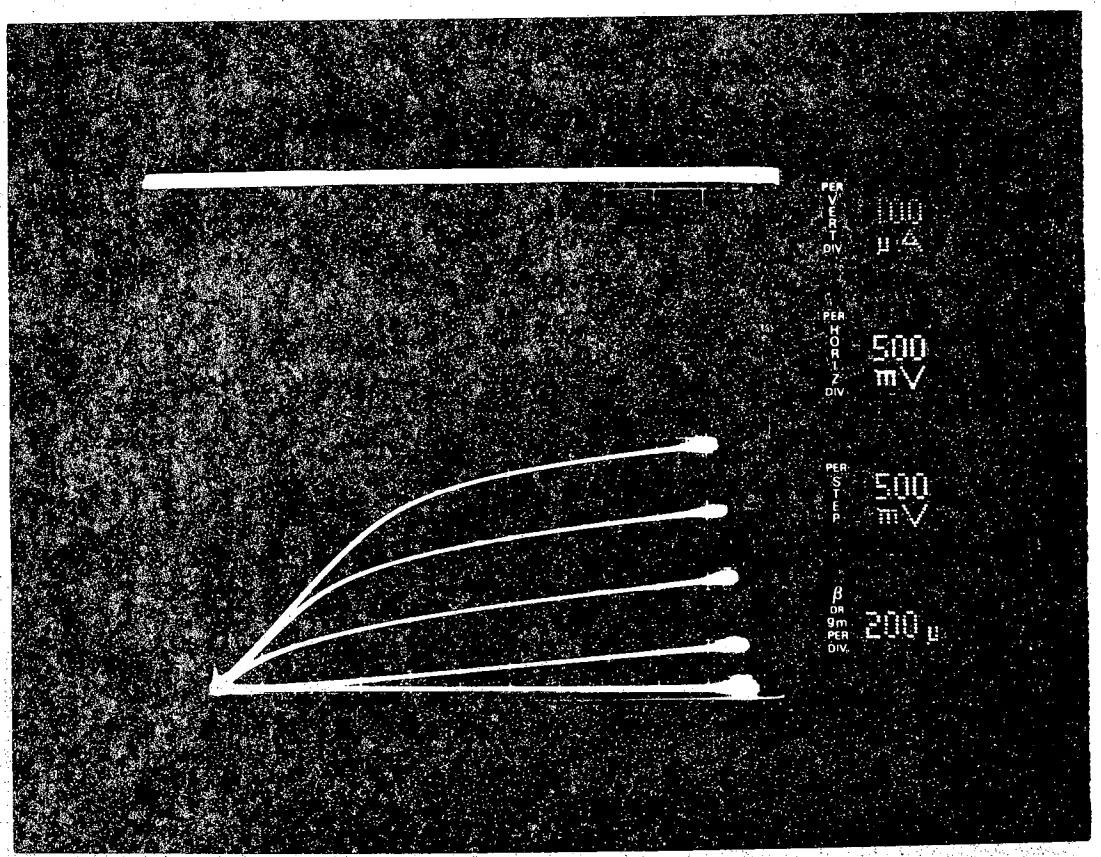

Figure 5.18. I_D versus V_{DS} at 77 °K for the 2μm transistor. The gate bias is decreased by 0.5V per trace starting at 0V.

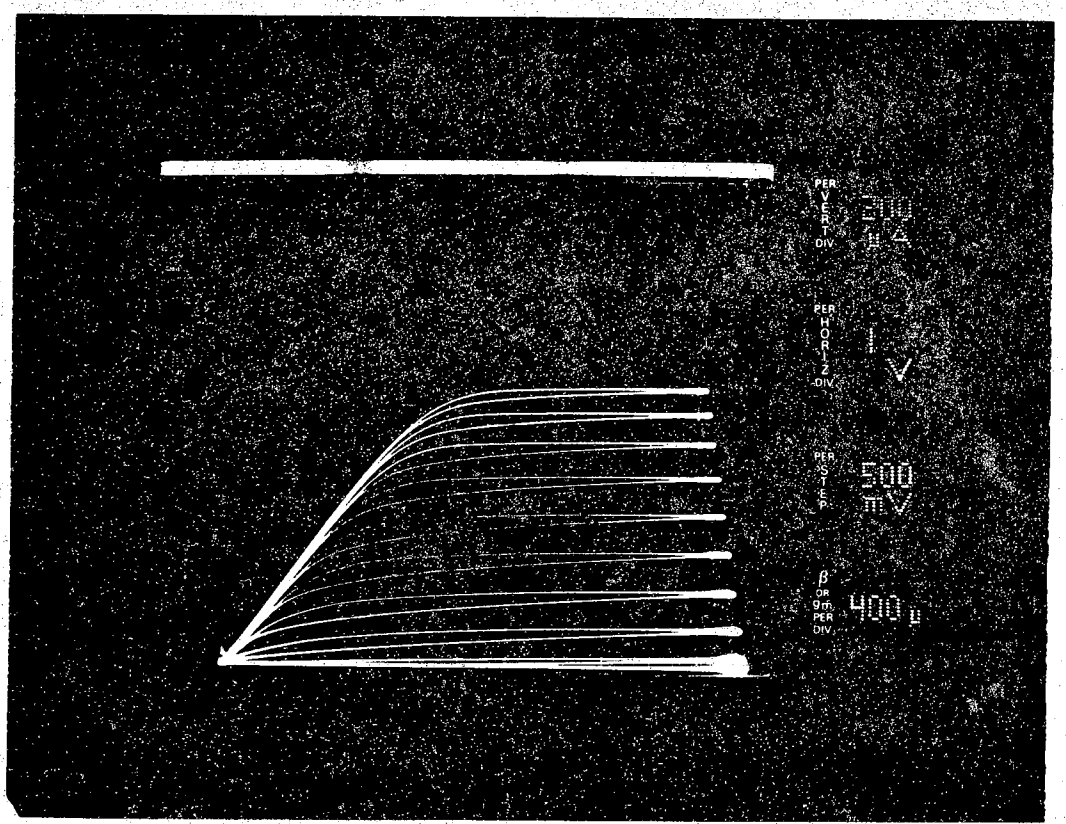

Figure 5.19. I-V relationship for the 2μm device with illumination at 77 $^{\circ}$K. The gate bias is decreased by 0.5V per trace starting at 0V.

CHAPTER 6
SUMMARY AND FUTURE RESEARCH

In summary, we have demonstrated the successful growth and characterization of ZnSe/GaAs(epi) heterostructures for use in MIS devices. The structures were grown in two separate MBE machines using an overlayer of amorphous arsenic to protect the as-grown GaAs epilayer during transfer between the machines. After the arsenic was desorbed, there was a small amount of oxygen present at the GaAs surface. The oxygen contamination was believed to originate from the III-V system and not from the transfer between the systems.

Nucleation of ZnSe on the GaAs epilayer resulted in layer-by-layer growth, as evidenced by the evolution of the RHEED pattern. Unlike nucleation on a GaAs substrate where the diffraction pattern remained spotty for several minutes, the RHEED streaks recovered after only 9 sec. for nucleation on the GaAs epilayer. The layer-by-layer growth mechanism was confirmed by observations of intensity oscillations in the specular spot. In one case, ZnSe nucleation on the epilayer resulted in 120 intensity oscillations. The nucleation of ZnSe on a GaAs substrate displayed intensity variation similar to the InGaAs/GaAs heterostructure which is known to grow three dimensionally.

Cross-sectional transmission electron micrographs of the 1000Å ZnSe on GaAs(epi) revealed a coherent, sharp interface between the two semiconductors. No misfit dislocations were observed in the pseudomorphic ZnSe film. A HREM micrograph showed an atomically flat interface with no interfacial defects present and is similar to the interface seen between GaAs and (Al,Ga)As.

Photoluminescence data from the pseudomorphic film revealed information about the changes in the ZnSe energy bands caused by the 0.25% lattice mismatch. The near-band-edge excitonic features were shifted to higher energy with the n=1 free exciton dominating the spectrum. Also, a n=1 free exciton to light-hole transition was observed which was not

normally seen in PL spectra of thicker ZnSe films.

Employing the 1000Å ZnSe/GaAs (epi) heterostructure, MIS capacitors and field-effect transistors were fabricated. The capacitors showed deep depletion like characteristics with an operating voltage range of 0V to -6V. The doped-channel field-effect transistors worked very well and demonstrated complete current saturation and channel cutoff. The long channel devices behaved as transistors with a constant mobility and had transconductances in the range of 5-12 mS/mm. Shorter channel devices displayed velocity saturation where the transconductance was primarily independent of the gate bias. A 2μm device had a maximum transconductance of 17mS/mm. Although looping was present in the IV characteristics, it was eliminated by sweeping the transistor at a faster sweep rate and by cooling the sample to 77 ° K.

The strength of the interrupted growth MBE procedure is the ability to systematically control the interface and film properties in order to reduce the number of states that contribute to charge trapping. For the devices reported here, a particular set of growth conditions were employed resulting in one single interface condition. Growth parameters such as substrate temperature, flux ratios, and crystal stoichiometry can be used to alter the interface, leading to improved device performances.

The characteristics of the doped-channel transistor can be further improved by reducing the source-drain contact resistance and the source-drain to gate spacing. The addition of nickel to the gold-germanium alloy will aid in reducing the contact resistance. Also, a transistor with a channel doping of $10^{17}cm^{-3}$ should be fabricated in order to better compare ZnSe and AlGaAs as insulators.

The realization of these transistors is a stepping stone into a larger area of ZnSe/GaAs devices. With improvement in the electrical characteristics of the interface, one can envision the use of ZnSe as a passivating layer for GaAs in enhancement-mode, modulation-doped, and high electron mobility FETs. Because of its optical properties, ZnSe will continue to be used for optical as well as current confinement in GaAs based light-emitting-devices. In the future, ZnSe may be used as a passivating layer for other III-V materials as well. With improved techniques for heterojunction fabrication as reported here, the utilization of the ZnSe/GaAs heterointerface for device applications appears promising.

LIST OF REFERENCES

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1. E.H.C Parker, ed. **The Technology and Physics of Molecular Beam Epitaxy,** Plenum Press: New York (1985), Chapters 1-5.

2. T. Yao, E.H.C. Parker, ed. **The Technology and Physics of Molecular Beam Epitaxy,** Plenum Press: New York (1985), pp. 313-342.

3. K. Yoneda, Y. Hishida, T. Tadao, H. Ishii, and T. Niina, Appl. Phys. Lett. **45,** 1300, (1984).

4. T. Mishima, W. Quan-kun, and K. Takahashi, J. Appl. Phys. **52,** 5797, (1981).

5. T. Niina, T. Yamaguchi, K. Yodoshi, K. Yagi, and H. Hamada, IEEE J. Quant. Elect. **QE-19,** 1021, (1983).

6. C.W. Wilmsen, ed. **The Physics and Chemistry of III-V Compound Semiconductor Interfaces,** Plenum Press: New York (1985)

7. S.D. Offsey, S.M. Woodall, A.C. Warren, D.D. Kirchner, T.I. Chappell, and G.D. Pettit, Appl. Phys. Lett. **48,** 475, (1986).

8. H. Hida, A. Okamoto, H. Toyoshima, and K.Ohata, IEEE Elect. Dev. Lett. **EDL7,** 625, (1986).

9. B. Kim, H.Q. Tserng, and H.D. Shih, IEEE Elect. Dev. Lett. **EDL5,** 494, (1984).

10. H.C. Casey, Jr., A.Y. Cho, D.V. Lang, E.H. Nicollian, and P.W. Foy, J. Appl. Phys. **50,** 3484, (1979).

11. Y. Katayama, M. Morioka, Y. Sawada, K. Ueyanagi, T. Mishima, Y. Ono, T. Usagawa, and Y. Shiraki, Jap. Journ. Appl. Phys. **23,** L150, (1984).

12. R.L. Gunshor, L.A. Kolodziejski, M.R. Melloch, M. Vaziri, C. Choi, and N. Otsuka, Appl. Phys. Lett. **50,** 200, (1987).

13. G.D. Studtmann, R.L. Gunshor, L.A. Kolodziejski, M.R. Melloch, J.A. Cooper, Jr., R.F. Pierret, D.P. Munich, C. Choi, and N. Otsuka, Appl. Phys. Lett. **51,** 1249, (1988).

14. N.J. Kawai, T. Nakagawa, T. Kojima, K. Ohta, and M. Kawashima, Electron. Lett. **20,** 47, (1984).

15. W.E. Spicer, I. Lindau, P. Skeath, and C.Y. Su, J. Vac. Sci. Technol. **17,** 1019,(1980).

16. S.P. Kowalczyk, D.L. Miller, J.R. Waldrop, P.G. Newman, and R.W. Grant, J. Vac. Sci. Tech. **19,** 255, (1981).

17. D.L. Miller, R.T. Chen, K. Elliott, and S.P. Kowalczyk, J. Appl. Phys **57,** 1922, (1985).

18. P.G. Neudeck, M.R. Melloch, and J.A. Cooper, Jr., *Experiments in Interrupted Growth Molecular Beam Epitaxy Technolgy,* Master's Thesis, Purdue University, December 1987, **TR-EE-88-3,** (1988).

19. L.A. Kolodziejski, H. Sato, S. Datta, and R.L Gunshor, *Molecular Beam Expitaxy of* $Cd_{1-x}Mn_xTe$. Master's Thesis, Purdue University, Chap. 2, (1984).

20. C. Chang, J. Vac. Sci.Tech., **21,** 663, (1982).

21. P.J. Estrup and E.G. McRae, Surf. Sci., **25,** 1-52, (1971).

22. R.M. Park and N.M. Salansky, Appl. Phys. Lett., **44,** 249, (1984).

23. L.A. Kolodziejski, R.L. Gunshor, T.C. Bonsett, R. Venkatasubramanian, S. Datta, R.B. Bylsma, W.M. Becker, and N. Otsuka, Appl. Phys. Lett., **47,** 169, (1985).

24. T. Yao and T. Takeda, Appl. Phys. Lett., **48,** 160, (1986).

25. M.C. Tamargo, J.L. deMiguel, D.M. Hwang, and H.H. Farrell, *paper presented at the 8th MBE Workshop, Los Angeles, Sept. 10-12, (1987).*

26. J.H. Neave, B.A. Joyce, P.J. Dobson, and N. Norton, Appl. Phys. A, **31,** 1, (1983).

27. L.A. Kolodziejski, R.L. Gunshor, N. Otsuka, B.P. Gu, Y. Hefetz, and A.V. Nurmikko, J. Cryst. Growth, **81,** 491, (1987).

28. B.F. Lewis, T.C. Lee, F.J. Grunthaner, A. Madhukar, R. Fernandez, and T. Maserjian, J. Vac. Sci. Tech. B, **2,** 419, (1984).

29 C. Choi and N. Otsuka, *Transmission Electron Study of Semiconductor Heterostructures Grown by Molecular Beam Epitaxy,* Doctor of Philosophy Thesis, Purdue University, Chapter 7, May 1988.

30. T. Yao, Y. Okada, S. Matsui, K. Ishida, and I. Fujimoto, J. Cryst. Growth, **81,** 518, (1987).

31. T. Yao, J. J. Appl. Phys., **25,** L544, (1986).

32. S. Datta, M. Yaminishi, R.L. Gunshor, and L.A. Kolodziejski, *Proceedings of the meeting on "Excitons in Confined Systems",* Rome, April 13-16, (1987).

33. L.A. Kolodziekji, R.L. Gunshor, M.R. Melloch, M. Vaziri, C. Choi, and N. Otsuka, **Growth of Compound Semiconductors,** Proc. SPIE, **796,** 86, (1987).

34. V.L. Rideout, S.S.E, **18,** 541, (1975).

35. Y. Shih, M. Murakami, E. Wilkie, and A. Callegari, J. Appl Phys., **62,** 582, (1987).

36. D. Munich, *GaAs Surface Passivation With AlGaAsN and ZnSe,* Doctor of Philosophy Thesis, Purdue University, to be published, (1988).

37. R.F. Pierret, **Modular Series on Solid State Devices, Field-Effect Devices, Volume IV,** Addison-Wesley, Reading Mass., (1983).

38. R.F. Pierret, **Modular Series on Solid State Devices, Advanced Semiconductor Fundamentals, Volume VI,** Addison-Wesley, Reading Mass., (1987), 193.

39. M. Fogiel, **Modern Microelectronics,** Research and Education Assoc., New York, (1972), pp. 513-516.

40. R.E. Williams, **Gallium Arsenide Processing Techniques,** Plenum Press: New York, (1986), pp. 225.

41. S. Sze, **Physics of Semiconductor Devices, 2nd Edition,** Wiley & Sons, New York, (1981), pp.325-340.

42. W.R. Frensley, IEEE Trans. Elect. Dev., **ED-28,** 962, (1981).

43. S.H. Wemple, W.C. Niehaus, H.M. Cox, J.V. Dilorenzo, and W.O. Schlesser, IEEE Trans. Elect. Dev., **ED-27,** 1013, (1980).

44. T.J. Drummond, W. Kopp, D. Arnold, R. Fischer, and H. Morkoc, Elect. Lett., **19,** 986, (1983).

APPENDICES

Appendix A
Doped Channel Field-Effect Transistor Run Sheet

Isolation Etch

21. Obtain ZnSe on n-GaAs wafer
    Size of wafer:
    Thickness of wafer:
    n-GaAs resistivity:

2. Ultraclean silicon wafer
    Boil in TCA for 5 minutes
    Ultrasonic in ACE for 5 minutes
    Ultrasonic in Methanol for 5 minutes
    DI H_2O rinse
    Heat dry @ 120 ° C

3. Degrease wafer
    Lightly boil in TCA for 5 minutes
    Ultrasonic in ACE for 5 minutes
    Ultrasonic in Methanol for 5 minutes
    DI Rinse
    N_2 Blow dry

4. Mount sample on silicon wafer
    Spread AZ 1350J-SF positive photoresist (3 drops)
    Place sample in photoresist
    Hardbake resist @ 120 ° C for 15 minutes

5. Deposit AZ 1350J-SF positive photoresist
    Spin @ 5000 RPM for 60 seconds
    Softbake resist for 10 minutes @ 90 ° C

6. Align and expose Mask #1 (Isolation Etch)

Kasper 1:1 mask aligner, exposure 13.0 units

7. Develop resist
   Develop in AZ Developer diluted with DI 1:1 for 30 seconds
   DI rinse for 60 seconds
   N_2 dry

8. Inspect wafer

9. Hardbake resist
   120 ° C for 15 minutes

10. Isolation Etch
    Etch ZnSe layer with 400ml DI H_2O:4ml HNO_3:0.2g $K_2Cr_2O_7$
    for 10-13 minutes (etch rate of $\simeq$ 100Å/sec)
    DI Rinse
    Etch GaAs layer with 400ml DI H_2O:12ml H_3PO_4:3ml H_2O_2
    for 15 minutes (etch rate of $\simeq$ 400Å/sec)
    DI Rinse
    N_2 Dry

11. Inspect Wafer

12. Strip resist
    Rinse in ACE for at least 5 minutes
    Rinse in Meth for 5 minutes
    DI Rinse
    N_2 Dry

13. Inspect wafer

Source-Drain Ohmic Contacts

14. Ultraclean silicon wafer
    Boil in TCA for 5 minutes
    Ultrasonic in ACE for 5 minutes
    Ultrasonic in Methanol for 5 minutes
    DI H_2O rinse

Heat dry @ 120 ° C for 15 minutes

15. Degrease wafer
    (No ultrasonic cleaning)
    Rinse in TCA for 5 minutes
    Rinse in ACE for 5 minutes
    Rinse in Methanol for 5 minutes
    DI Rinse
    N_2 Blow dry

16. Ultraclean Au-Ge pellets and Ti boat
    Obtain 3 pellets
    Boil in TCA for 10 minutes (2x)
    Ultrasonic in ACE for 10 minutes
    Ultrasonic in Methanol for 10 minutes
    DI Rinse
    Heat Dry @ 120 ° C for 15 minutes

17. Mount sample on silicon wafer
    Spread AZ 1350J-SF positive photoresist (3 drops)
    Place sample in photoresist
    Hardbake resist @ 120 ° C for 15 minutes

18. Deposit AZ 1350J-SF positive photoresist
    Spin @ 5000 RPM for 60 seconds
    Softbake resist for 10 minutes @ 70 ° C

19. Align and expose Mask #2 (Source-Drain Contacts)
    Kasper 1:1 mask aligner, exposure 17.0 units

20. Develop resist
    Soak in xylene for 3 minutes
    N_2 dry
    Develop in AZ Developer diluted with DI 1:1 for 30 seconds
    DI rinse for 60 seconds
    N_2 dry

21. Inspect wafer

22. Source-Drain Contact Etch
    Etch ZnSe layer with 400ml DI H_2O:4ml HNO_3:0.2g $K_2Cr_2O_7$
    for 10-13 minutes (etch rate of$\simeq$ 100Å/sec)
    DI Rinse
    Strip oxides with 40 second dip in 400ml H_2O:40ml NH_4OH
    DI Rinse
    Quickly dry with N_2 and load into evaporator

23. Evaporate Au-Ge pellets
    Pump to $5.0x10^{-7}$ Torr
    Evaporate material at 5V and 6A.

(Steps 24 - 28 must be performed within 1 hour after evaporation)

24. Strip resist
    Rinse or squirt with ACE for at least 5 minutes
    (separate wafers)
    Rinse in Methanol for 2 minutes
    DI Rinse
    N_2 Dry

25. Inspect wafer

26. Anneal Contacts
    Heat in Marshall Oven at 450 ° C for 90 seconds
    Cool

27. Inspect wafer

28. Probe ohmic contacts

29. Repeat steps 26-28 if necessary

Top Metallization

30. Ultraclean silicon wafer
    Boil in TCA for 5 minutes
    Ultrasonic in Methanol for 5 minutes
    Ultrasonic in ACE for 5 minutes
    DI H_2O rinse
    Heat dry @ 120 ° C oven

31. Degrease wafer
    (No ultrasonic cleaning)
    Rinse in TCA for 5 minutes
    Rinse in ACE for 5 minutes
    Rinse in Meth for 5 minutes
    DI Rinse
    N_2 Blow dry

32. Degrease 5 aluminum bars and Tu filament
    Boil in TCA for 10 minutes (2x)
    Ultrasonic in ACE for 10 minutes
    Ultrasonic in Meth for 10 minutes
    Rinse in DI
    Heat dry @ 120 ° C for 15 minutes

33. Mount sample on silicon wafer
    Spread AZ 1350J-SF positive photoresist (3 drops)
    Place sample in photoresist
    Hardbake resist @ 120 ° C for 15 minutes

34. Deposit AZ 1350J-SF positive photoresist
    Spin @ 5000 RPM for 60 seconds
    Softbake resist for 10 minutes @ 70 ° C

35. Align and expose Mask #3 (Top Metallization)
    Kasper 1:1 mask aligner, exposure 17.0 units

36. Develop resist
    Soak in xylene for 3 minutes

Dry N_2
Develop in AZ Developer diluted with DI 1:1 for 30 seconds
DI rinse for 60 seconds
N_2 dry
Quickly load into NRC system

37. Inspect wafer

38. Evaporate aluminum
Pump to $5x10^{-7}$ Torr
Evaporate at 3A and 10V for 2 minutes

39. Strip resist
Rinse or squirt with ACE for at least 5 minutes
Rinse in Methanol for 5 minutes
DI Rinse
N_2 Dry

40. Inspect wafer

Appendix B
Derivation of Doped Channel FET Parameters

B.1 Long Channel Devices

The long channel device parameters for the doped channel field-effect transistor are derived in this appendix. The device characteristics of interest are the drain current and the small signal gain, the transconductance. The following derivation is modeled after the analysis of a n-channel junction field-effect transistor found in reference 37.

The cross sectional schematic of the device appears in figure 5.4 showing the coordinate system and the dimensions of the transistor. The channel is three dimensional with width, length, and depth of Z, L and (a), respectively. The current is assumed to be uniform for any value of y, where x and y are the directions perpendicular and parallel to the insulator-semiconductor interface, respectively. As in reference 37, this assumption (1) allows a two dimensional analysis of the drain current. Some of the other assumptions are (2) the device is uniformly doped with a donor concentration equal to N_D. (3) Current flow is confined to the non-depleted portions of the n-region. (4) W(y) is the depletion region under the gate at position y and is either in depletion or deep depletion for all gate voltages of interest. (5) The gradual channel approximation is in effect where the rate of change of electrostatic variables in the y-direction is relatively slow compared to the rate of change of the same variables in the x-direction. (6) Assumption number 5 allows us to write W(y) in terms of both the gate voltage and the drain voltage, equations 1 and 2. (7) The MIS gate capacitor has no initial band bending, and as a result, an ideal gate voltage (V_G') is applied to the device. (8) The voltage drops outside the gate region, source to y=0 and drain to y=L are negligible.

$$W(y)=x_o'\left\{\left[1+\frac{V_G'-V(y)}{V_\phi}\right]^{1/2}-1\right\} \qquad (1)$$

$$V_\delta = -\frac{qK_s x_o^2 N_D}{2K_o^2 \epsilon_o} \tag{2}$$

We begin with the drift equation for electrons which is valid for charge motion in the voltage range below channel pinchoff, $0 \leqq V_D \leqq V_{Dsat}$ and $V_P \leqq V_G \leqq 0$. V_P is the gate voltage that causes W(L) to equal the channel thickness (a). In equation 3, we are assuming that minority carrier current is negligible.

$$J_N = J_{Ny} = q\mu_N N_D \mathscr{E}_y = -q\mu_N N_D \frac{\partial V}{\partial y} \tag{3}$$

J_{Ny} and $\mathscr{E}_y$ are the current density and electric field in the y direction, respectively. The variables used in this appendix are further defined in Table 3 of Chapter 5. Invoking the first assumption that the drain current is uniform throughout the device, the derivation proceeds by integrating the current density, equation 3, over the cross sectional area of the non-depleted channel giving equation 4.

$$I_D = -\int\int J_{Ny} \partial x \partial z \tag{4}$$

The integral over the z direction brings a gate width Z out in front of the first integral while the integration over the x direction multiplies the current density by the width of the non-depleted channel [a - W(y)].

$$I_D = Zq\mu_N N_D [a - W(y)] \frac{\partial V}{\partial y} \tag{5}$$

We now proceed to eliminate the dependence of equation 5 on y by substituting the expression for W(y) given in equation 1 into the I_D relationship. At this point, the current equation consists only of terms that are dependent on a varying drain voltage ($V(y=0) = 0$ and $V(y=L) = V_D$). The derivation is completed by multiplying both sides by ∂y and integrating I_D with respect to y while integrating the right side of the equality with respect to V.

$$\int_0^L I_D \partial y = Zq\mu_N N_D \int_{V=0}^{V=V_D} \left[a - x_o' \left\{ \left[1 + \frac{V_G' - V}{V_\delta} \right]^{1/2} - 1 \right\} \right] \partial V$$

$$I_D L = Z q \mu_N N_D \left[(a+x_o')V_D - \int_{V=0}^{V=V_D} x_o' \left\{ 1+\frac{V_G'-V(y)}{V_\delta} \right\}^{1/2} \partial V \right]$$

The final integral results in the drain current as a function of V_G' and V_D in the linear region of operation, equation 6.

$$I_D = \frac{Z q \mu_N N_D}{L} \left[(a+x_o')V_D + \frac{2}{3} x_o' V_\delta \left\{ \left[1+\frac{V_G'-V_D}{V_\delta} \right]^{3/2} - \left[1+\frac{V_G'}{V_\delta} \right]^{3/2} \right\} \right] \quad (6)$$

$$V_{Dsat} \geqq V_D \geqq 0$$

$$V_P \leqq V_G' \leqq 0$$

When the depletion width in the n-GaAs at the drain end of the gate pinches off to the semi-insulating GaAs, the drain current saturates. To derive the saturation current in the beyond pinchoff state, the saturation voltage is calculated and correspondingly substituted into equation 6. Saturation of the drain current occurs when W(L) = (a), and this happens when $V_D = V_{Dsat} = V_G' - V_P$.

$$V_{Dsat} = V_G' - V_\delta \left[\left(\frac{a+x_o'}{x_o'} \right)^2 - 1 \right] \quad (7)$$

The ensuing substitution of equation 7 into equation 6 results in saturation current at a gate voltage V_G'.

$$I_{Dsat} = \frac{Z q \mu_N N_D (a+x_o')}{L} \left\{ V_G' - V_\delta \left(\frac{a^2+2x_o'}{x_o'^2} \right) + \frac{2}{3} V_\delta \left[\left(\frac{a+x_o'}{x_o'} \right)^2 - \left(\frac{x_o'}{(a+x_o')} \right) \left(1+\frac{V_G'}{V_\delta} \right)^{3/2} \right] \right\}$$

$$V_G' - V_D \leqq V_P$$

The final parameter of interest in the long channel device is the transconductance which is found by taking the derivative of the saturation current with respect to the ideal gate voltage ($g_m = \frac{\partial I_D}{\partial V_G'}$). Every term in the above equation drops out except for the first and the last terms, leaving

equation 9.

$$g_m=\frac{\partial I_{Dsat}}{\partial V_G'}=\frac{Zq\mu_N N_D}{L}(a+x_o')\left\{1-\frac{x_o'}{a+x_o'}\left(1+\frac{V_G'}{V_\delta}\right)^{1/2}\right\} \tag{9}$$

B.2 Short Channel Devices

The short channel transconductance derivation is taken from reference 42 and is similar to the derivation for a short channel junction field-effect transistor under total velocity saturation. In this case, the drain current saturates because the velocity of the electrons in the channel reaches a maximum value of $2x10^7$cm/sec at an electric field of approximately 3500V/cm. The saturation current for a gate voltage V_G' for total velocity saturation under the gate is given by equation 10.

$$I_{Dsat}=qv_sZ(a-W(y))N_D \tag{10}$$

where v_s is the saturated velocity. The drain current saturates for a critical drain voltage approximated by $V_{Dsat} = \mathscr{E} L$ where $\mathscr{E}$ is the electric field at maximum electron velocity.

To solve for the transconductance, the expression for W(y) is substituted into equation 10, V(y) is replaced with $\mathscr{E} L$, and the derivative is taken with respect to the gate voltage.

$$I_{Dsat}=qv_sZ\left(a-x_o'\left\{\left[1+\frac{V_G'-V(y)}{V_\delta}\right]^{1/2}-1\right\}\right)$$

$$g_m=\frac{\partial I_{Dsat}}{\partial V_G'}$$

$$g_m=\frac{-qv_sZN_Dx_o'}{2V_\delta}\left(1+\frac{V_G'-\mathscr{E} L}{V_\delta}\right)^{-1/2} \tag{11}$$

By substituting equation 2 into equation 11, the transconductance can be simplified further.

$$g_m = C_o v_s Z \left(1 + \frac{V_G' - \mathscr{E} L}{V_\delta} \right)^{-1/2} \qquad (12)$$

C_o is the oxide capacitance.

The above expression for g_m, eq. 12, is similar to the transconductance in an enhancement-mode transistor of $C_o v_s Z$. In this case, the square root term is vary close to one because the electric field times the gate length is relatively smalled compared to the gate voltage. Hence, the transconductance for the short channel FET will be essentially independent of the gate voltage.

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