Modeling and Applications of Hydrogenated Amorphous Silicon Thin Film Transistors

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TR-EE 88-1
January 1988

School of Electrical Engineering
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West Lafayette, Indiana 47907

This work was supported by the AMOCO Research Center.
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SILICON THIN FILM TRANSISTORS

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ABSTRACT

Very recently, the hydrogenated amorphous silicon thin film transistor (a-Si:H TFT) has shown its important application as an on-board driver for large-area flat-panel liquid crystal displays. It is also highly desirable to have on-board TFT logic circuits adjacent to the TFT driver matrix and have them implemented in the same technology on the same substrate. This reduces the number of lead connections to the display and hence the cost, and increases the reliability of the display.

The first area to be investigated is the modeling of $I_D$ vs. $V_D$ static output characteristics of the n-channel a-Si:H TFT. Second, ambipolar characteristics of the a-Si:H TFT are investigated and modeled. Thereby device models for CAD circuit simulation programs are made available for circuit design. Third, a novel CMOS-like inverter circuit is presented as an application of the ambipolar a-Si:H TFT, and its static characteristics are analytically modeled. The transient response of the TFT is also characterized and modeled in order to understand its device limitations and to quantify its speed. Finally, the dynamic characteristics of the ambipolar a-Si:H TFT inverter are investigated and modeled so that its switching speed can be predicted and the optimized inverter can be designed.
CHAPTER 1
INTRODUCTION

1.1 Background

In recent years, amorphous silicon has attracted considerable attention as a promising material for the fabrication of thin film transistors, solar cells, and image sensors. Amorphous silicon can be deposited easily and uniformly on large-area substrates of various materials and it has good electrical and optical properties. The hydrogenated amorphous silicon (a-Si:H) thin film transistor (TFT) has shown its important application as a switching element in large-area flat-panel liquid crystal display arrays because it has a large resistivity and the device processing is compatible with standard MOS integrated circuit technology. This also has the promise of vertical integration when the TFT is placed on the top of the standard MOS integrated circuit.

As a-Si:H TFT applications increase, an accurate \( I_D \) vs. \( V_D \) characteristic model is desirable for computer aided design (CAD) circuit analysis programs. For example, developing a-Si:H TFT logic circuits to reduce the number of required leads to a flat-panel liquid crystal display has become an important new area of investigation. Existing CAD models do not have the capability to simulate such circuits. It is one of the purposes of this thesis to develop a set of equations that can be incorporated into computer aided design programs.

The a-Si:H TFT, with ohmic source/drain contact regions and a high quality gate insulator, is capable of operating in either or both the n-channel and p-channel regimes. This ambipolar property of the a-Si:H TFT is also characterized and modeled. Employing the ambipolar characteristics of the a-Si:H TFT, a new complementary type inverter circuit is investigated, and its static characteristics are modeled.

Unlike conventional devices, the electrical characteristics of a-Si:H TFTs are time dependent. Hence, the switching speed of the a-Si:H TFT is one of the major concerns in its applications. In order to understand its
fundamental and device limitations and to quantify reasons for its speed, the transient response of the a-Si:H TFT is studied and modeled by taking into account charge trapping and detrapping mechanisms at the insulator-semiconductor interface.

Dynamic models with and without the transient response of the TFT are then developed, and they are used to predict the switching speed of the CMOS-like a-Si:H TFT inverter and optimize the inverter circuit.

1.2 Thesis Overview

Chapter 2 contains a review of the relevant literature on the basic properties of a-Si and on the concept and applications of the a-Si:H thin film transistor. Chapter 3 develops a model for the static characteristics of plasma-enhanced (PE) CVD a-Si:H TFT from basic principles. Chapter 4 describes and models ambipolar property of the a-Si:H TFT. Chapter 5 shows a new complementary inverter circuit as an application of a-Si:H TFTs and develops an analytical model of the inverter circuit. Chapter 6 describes the transient response of an a-Si:H TFT. Chapter 7 models the dynamic characteristics of the CMOS-like ambipolar a-Si:H TFT inverter and optimizes the inverter circuit. Finally, chapter 8 contains a summary of this investigation and recommendations for future work.
CHAPTER 2
LITERATURE REVIEW

2.1 Introduction

Interest in amorphous solids has picked up considerably since the mid-1960's, and this has been so particularly for amorphous semiconductors. Some of the recent reviews on amorphous semiconductors have been edited by Brodsky¹, Kazmerski², Yonezawa³, Willardson and Beer⁴, Joannopoulos and Carlson⁵,⁶, Adler and Fritzsche⁷, and Adler et al.⁸.

This review shows the present level of understanding of amorphous silicon (a-Si) as it is used as a semiconducting material in thin film transistors. First, some of the basic properties of amorphous silicon will be described. Second, an introduction will be given of the basic concept and various realizations of a hydrogenated amorphous silicon thin film transistor. Finally, a summary will be given of some of the applications of the hydrogenated amorphous silicon thin film transistors reported to date.

2.2 Basic Properties of Amorphous Silicon

2.2.1 Structure

The physical properties of amorphous silicon are related to its structural features: the lack of long range order, even though each atom may have just the conventional number of nearest neighbors at the conventional distance. Figure 2.1 shows the variation of atomic neighbor density with distance for amorphous and recrystallized silicon, as determined from analysis of electron diffraction data⁹. The peaks in Figure 2.1 can be interpreted to show that each Si atom has four nearest neighbors at a distance of 2.35 Å in both amorphous and crystalline silicon, but that the arrangement of more remote neighbors is random in the amorphous state. Thus the curve for a-Si shows almost no peak for the distance of third-nearest neighbors (4.5 Å), while the effects of bond angle distortion are noticeable as a line broadening at the distance for second-nearest-neighbors.
Figure 2.1 Radial density of atoms as deduced from electron diffraction data for a thin film of amorphous silicon (as deposited), and following recrystallization of the film. From Ref. 9.
An ideal a-Si can be defined as a random network with no long range order but excellent short range order. Such an a-Si should have no structural defects (such as voids), and should permit local valence requirements to be satisfied for every atom; i.e., there should be no dangling bonds. However, the actual atomic network of a-Si has many defects resulting from imperfect short range order as shown in Figures 2.2(a) and 2.2(b).

### 2.2.2 Localized States

The general features of the atomic and electronic structures of both single-crystal and amorphous Si are dominated by their covalent bonding requirements. From Figure 2.1, the short-range order in a-Si was shown to be similar to that found in single-crystal Si leading to conduction and valence bands such as shown in Figure 2.3. The existence of such band-like behavior in a-Si as in single-crystal Si has been verified by the activated temperature dependence of the electrical conductivity described by

\[ \sigma = \sigma_0 e^{-\Delta E/kT} \]  

(2.1)

where \( \sigma_0 \) is a pre-exponential factor in \((\text{mho} \cdot \text{cm})^{-1}\), \( \Delta E \) is the activation energy in eV, \( k \) is \( 8.62 \times 10^{-5} \text{ eV/K} \), and \( T \) is the temperature in degrees K.

Within the conduction and valence bands, the states are "extended", which means that the wave-functions occupy the entire volume. The only kind of wave-function that is valid for one of the gap ranges of energy is a wave-function localized around a defect or at the surface of the crystal. A foreign atom, lattice vacancy, or other interruption of perfect periodicity can lead to the existence of a bound state wave-function centered on the defect location \( \mathbf{r}_0 \):

\[ \psi = A \exp[-ik|\mathbf{r}-\mathbf{r}_0|] \]  

(2.2)

Since \( k \) is imaginary, the wave-function of Equation (2.2) decays steadily as it moves away from \( \mathbf{r}_0 \) in any direction, which implies a localization of the charge density \(-|\psi|^2\).
Figure 2.2  Schematic representation of possible defects in (a), (b) a-Si, and (c) single-crystal Si. The three defects in (a) and (b) correspond to three dangling bonds in various configurations in a continuous random network. The three defects in (c) correspond to a monovacancy, a divacancy and a dislocation. From Ref. 10.
Figure 2.3 Energy band model of a-Si. The continuous distribution of states in the energy gap is not seen in crystalline semiconductors. The energies $E_v$ and $E_c$, called mobility edges, mark the boundaries of the mobility gap. From Ref. 12.
An electron can be trapped by the local electric field of the defect and has an energy lying within one of the energy gaps; an energy which is forbidden for freely moving electrons. Such “localized" states are always present in a-Si due to its lack of long-range order. Strong structural disorder within noncrystalline material can lead to spatial fluctuations in potential resulting in the formation of localized states. Localized states deep in the gap of a-Si are due to defects in the amorphous network and impurities. The simplest defect is a broken or dangling bond in which one of the two shared atoms in a covalent bond is not available to complete the bonding arrangement as shown in Figures 2.2(a) and 2.2(b).

Conduction mechanisms in single-crystal Si take place through extended states alone, while such mechanisms in a-Si take place through both extended and localized states as will be explained in Section 2.2.4. Although the temperature dependence of the activated conductivity described by Equation (2.1) seems to indicate a sharply defined energy bandgap, such is not actually the case because of localized states at the band edges as explained above. The distribution of localized states in a-Si at the band edges tapers off into the bandgap. The reason that such a distinct ΔE is observed is due to the difference in mobility of carriers in the localized and extended states. The carrier mobility in localized states is much lower than that in extended states. Hence, there appears to be a sharp cutoff in the conduction mechanism, and the observed ΔE relates to a mobility gap rather than an energy gap in the density of states.

Various experimental techniques have been used to measure the density of localized states in the mobility gap of amorphous silicon. The earliest results about the density of localized states were obtained by the field effect technique. Other techniques have been used to measure the density of localized states, and they are capacitance-voltage, capacitance-frequency, capacitance-temperature, and deep level transient spectroscopy techniques. Recent reviews of all these techniques and their different results were given by Cohen and Street and Biegelsen.
2.2.3 Energy Band Models

Several density of states models have been proposed for use in explaining conduction in a-Si. Differences in the models arise in the expected shape of the localized states in the mobility gap.

The Cohen-Fritzsche-Ovshinsky (CFO) model\textsuperscript{18} is shown in Figure 2.4(a)\textsuperscript{19}. The CFO model assumes that the band tail states extend across the gap with little fluctuation in the state distribution. The gradual decrease of the localized states destroys the sharpness of the conduction and valence band edges. Such a distribution results from conduction and valence band tails overlapping when the disorder of amorphous solid is sufficiently great. With such overlapping, there may be electrons in the valence band tail states having higher energies than electrons in conduction band tail states. The electrons in the valence band tail states can fall into the lower energy conduction band tail states. When this electron redistribution occurs, the filled states in the conduction band tail are negatively charged, assuming they are acceptor-like states, while the empty states in the valence band tails are positively charged, assuming they are donor-like states. Hence, this redistribution insures self-compensation and pins the Fermi level close to the middle of the gap where the density of states is at a minimum\textsuperscript{19,20}. This model will be simplified and then used for modeling of the a-Si bulk in a plasma-enhanced (PE) CVD a-Si:H TFT in Chapter 3.

The Davis-Mott model\textsuperscript{21} is shown in Figure 2.4(b). The band tails of localized states are now rather narrow at the edges of the mobility gap and another band exists at the middle of the gap originating from defects in the random network, e.g., dangling bonds, vacancies, etc. This center band may be split into donor and acceptor bands, which also pins the Fermi level.

Experimental evidence has been found for the existence of various localized gap states, which are split off from the tail states and are located at well-defined energies in the gap. These states are also associated with defect centers. The position of the Fermi level is then determined by the charge distribution in the gap states. Marshall and Owen also introduced a variation to the Davis-Mott model showing bands of donors and acceptors in the upper and lower halves of the mobility gap\textsuperscript{22}. This model seems to be best suited for chalcogenide glasses rather than elemental amorphous semiconductors. The simplified Davis-Mott model will be used for modeling of the insulator-semiconductor interface states in a PECVD a-Si:H TFT in Chapter 3.
Figure 2.4 Schematic density of states diagrams for amorphous semiconductors: (a) CFO model and (b) Davis-Mott model. From Ref. 19.
2.2.4 Electrical Conduction

On the basis of the Davis-Mott model, there can be three processes leading to conduction in a-Si. Their relative contribution to the total conductivity predominates in different temperature regions. At very low temperatures conduction can occur by thermally assisted tunneling between states at the Fermi level. At higher temperatures charge carriers are excited into the localized states of the band tails; carriers in these localized states can take part in the electric charge transport only by "variable range hopping". In these conduction mechanisms, carriers jump from localized states to other sites through a phonon assisted tunneling process. This process is similar to impurity band conduction in heavily doped semiconductors at low temperatures.

Figure 2.5 shows a schematic illustration of electron transport mechanisms in a-Si, using the format of an energy level diagram in real space\textsuperscript{23}. Two hopping transitions are indicated by A and B in Figure 2.5, two possible tunneling processes which take an electron in a filled state below the Fermi level to either of two nearby empty states above $E_F$. $R$ denotes the distance the electron hops, while $W$ denotes the energy separation of the final and initial states. This hopping conduction has been described by Mott\textsuperscript{24} and is characterized by the relation

$$\sigma = \left[ \frac{e^2}{2(8\pi)^{1/2}} \right] \nu_{ph} \left[ \frac{N(E_F)}{\alpha k T} \right]^{1/2} e^{-\left( A / T \right)^{1/4}}, \quad (2.3)$$

where

$$A = 2.1 \left[ \frac{\alpha^2}{k N(E_F)} \right]^{1/4}, \quad (2.4)$$

$\nu_{ph}$ is the phonon frequency in Hz, $\alpha$ is the rate of wave function fall-off at a site, $N(E_F)$ is the density of states at the Fermi level in $\#$/cm$^3$-eV and "$e$" is the charge of an electron in Coulombs. This relation has been verified experimentally.

At still higher temperatures the electron is excited to the level labeled C, an extended state above the conduction-band edge $E_C$, and contributes to the conductivity in a way similar to that of a conduction electron in a single-crystal Si. The mobility in the extended states is much higher than in
Figure 2.5  Energy-level schematic for electronic conduction mechanisms in an a-Si. Energy is represented in the vertical direction, distance in the horizontal direction. From Ref. 23.
the localized states. However, because of the presence of localized states below $E_C$, the electron's motion is interrupted by trapping and release events as indicated in Figure 2.5. Hence, the electron's drift mobility is severely limited by trapping as well as by scattering, and the carrier mobility in the extended states of a-Si is much lower than in single-crystal Si.

The electrical conductivity of a-Si described by Equation (2.1) increases exponentially with respect to the temperature $T$. This is due to the fact that the electron density in the extended states varies very steeply with an exponential relationship with the temperature ($\sim e^{-\Delta E/kT}$).

Figure 2.6 pictures a two-dimensional amorphous semiconductor for energies below, at, and above the mobility edge. For the low energy of part (a), there are a few small isolated regions in which electrons may move freely, but there is no connection between these regions. Current can flow from one end of the sample to the other only by electron hopping. The intermediate energy of part (b) reveals some connected channels which permit long-distance percolation without hopping. For the still higher energy of part (c), only a few isolated pockets remain which are not contributing to the overall current flow.

The ability of an amorphous semiconductor to conduct is thus dependent on getting electrons into above the conduction band edge (or holes into below the valence band edge). As a consequence, just about any amorphous solid has a conductivity that increases on warming. Figure 2.7 shows how the electron drift mobility and electrical conductivity increase with increasing temperature for a 1.3 $\mu$m evaporated film of a-Si. The values of $\Delta\varepsilon$ quoted in part (b) refer to a comparison with Equation (2.1). For temperatures below the indicated $T_c$, transport occurs by hopping among the localized states within the gap.

### 2.2.5 Role of Hydrogen in a-Si

By introducing hydrogen into a-Si films either during preparation or by subsequent infusion of atomic hydrogen, it is possible to reduce material defects, thereby decreasing the number of localized states in the mobility gap. Hydrogen acts as a dangling bond terminator and thus passivate or compensate the dangling bond in a-Si. With fewer localized states in the mobility gap, the energy band structure of the hydrogenated a-Si more closely approaches that of single-crystal Si allowing its greater applications
Figure 2.6  Percolation theory applied to the concept of a mobility edge in an amorphous semiconductor. From Ref. 23
Figure 2.7  Temperature dependence of (a) electron drift mobility, and (b) electrical conductivity for an a-Si film. From Ref. 25.
in semiconductor-type devices. When hydrogen reduces the density of localized states, the extent of carrier trapping and scattering is decreased, and thus the carrier mobility in the extended states is increased. The proper designation for the hydrogenated a-Si alloy is "a-Si:H" and is the form of a-Si used in this thesis.

Evidence that hydrogen neutralizes dangling bonds is given by the disappearance of the electron spin resonance (ESR) signal in hydrogenated a-Si as compared to pure a-Si. The ESR signal originates from unpaired electron spins which are produced by dangling bonds.

The properties of a-Si:H are affected by the way that hydrogen is incorporated into a-Si26,27. To investigate the local environments at the hydrogen sites, several groups28 have studied infrared absorption and Raman scattering (scattering of photons by phonons) of a-Si containing substantial amounts of bonded hydrogen. The material is described as a Si-H binary alloy where there are multiple, as well as single, H-atom attachment. Figure 2.8 shows the atomic motions of the vibrational modes used to investigate the a-Si:H structure26.

Besides hydrogen, several other species such as chlorine and fluorine have also been found to be effective dangling bond terminators in amorphous silicon. It is found that the bond energy of fluorine with silicon is about 1.6 times as large as that of hydrogen-silicon and that fluorine has remained in the a-Si film and kept its bond with Si even after annealing at 600 °C29. In fact, it has been shown that glow discharge a-Si:F:H has characteristics superior to a-Si:H (i.e., better doping efficiency and lower density of states in the mobility gap)30.

2.2.6 Preparation of a-Si:H Films

In general, there are three classes of preparation techniques used to date to produce the a-Si:H film: decomposition of a compound material containing hydrogen and silicon, addition of hydrogen during the deposition process of a-Si, and diffusion of hydrogen into a-Si deposited by other technique. In particular, the a-Si:H films have been prepared by vacuum evaporation31,32, ion implanting into single-crystal Si33, sputtering34, chemical vapor deposition (CVD)35 and plasma-enhanced low pressure CVD (glow discharge) techniques36. The emphasis in the film preparation has moved to those techniques which make the film more hydrogen-rich because
Figure 2.8  Atomic displacement of H atoms in local and resonance mode vibrations in (a) SiH groups, (b) SiH$_2$ groups, and (c) SiH$_3$ groups. From Ref. 26.
hydrogen incorporation in a-Si results in a higher quality semiconducting film. Today plasma-enhanced CVD produced a-Si is known to have a hydrogen content of 10 to 50 at % and most of the hydrogen is bonded to Si atoms\textsuperscript{37}.

While the plasma-enhanced CVD technique is inherently hydrogen-rich because of the dissociated silane (SiH\textsubscript{4}) gas containing hydrogen ions, the vacuum evaporation, sputtering, and CVD techniques are not as hydrogen rich. To incorporate hydrogen, sputtering can be accomplished in a hydrogen-rich environment or the sputtered a-Si can be post-hydrogenated. Similarly, the CVD material must be post-hydrogenated because of its inherently high temperature processing (\(\approx 600^\circ\text{C}\)) which tends to evolve any hydrogen incorporated during this thermal decomposition process.

In the process of the a-Si:H film, the substrate temperature should not exceed 300\(^\circ\text{C}\) as hydrogen effuses from the film at this temperature. Undoped a-Si:H also crystallizes near 620\(^\circ\text{C}\)\textsuperscript{38}. Hence, high temperature process must be avoided on the a-Si:H film if the film is to remain amorphous and hydrogen-rich.

The thin film transistor modeled in this thesis uses a-Si:H which is prepared by plasma-enhanced CVD technique. In PECVD technique, the silane gas is decomposed and the amount of hydrogen in the deposited film is controlled by the reaction chemistry. The dominant species in gas-phase reactions are SiH, SiH\textsubscript{2}, and SiH\textsubscript{3}, and isolated silicon atoms are not present in any appreciable concentration\textsuperscript{39}. It is expected that the growth of the film proceeds through nucleation, growth, and coalescence of islands.

Deposition reactors are classified by the type of electrical excitation used; direct current (dc) or radio-frequency (rf) current. In rf excitation the reactors are further classified by how the excitation is coupled into the plasma; inductive or capacitive. The deposition process is a surface reaction and thus strongly affected by the deposition parameters such as silane concentration, gas flow rate, pressure, rf power, and substrate temperature.
2.3 Amorphous Silicon Thin Film Transistors

2.3.1 Introduction

Spear and LeComber\textsuperscript{10} used the field effect technique to measure the density of localized states during their early investigations into the electrical properties of a-Si:H. In the field effect technique, a structure similar to that shown in Figure 2.9 is used. Their experiments showed that a-Si:H has a remarkably low density of localized states, and that its conductivity can be controlled by several orders of magnitude by moderate gate voltages. In 1979, the first a-Si:H TFT\textsuperscript{40} suitable for driving liquid crystal displays was developed by Lecomber et al\textsuperscript{41}.

The structure shown in Figure 2.9 is that of a thin film transistor (TFT) described widely in the literature\textsuperscript{42}. The TFT have been made with various semiconducting materials such as a-Si:H, poly-Si, Te, CdSe, and CdS, and they have different advantages and disadvantages.

In order to obtain good experimental data from structures fabricated with a-Si:H films, consideration must be given to the scheme used for making electrical connection to the film. If the contact resistance is too high, the film and/or device performance can be obscured or masked entirely by the contact resistance. Since all metals form reasonable Schottky barriers on a-Si:H\textsuperscript{43}, techniques similar to those used in crystalline semiconductors are needed to form ohmic contacts on a-Si:H. Two such techniques include annealing and doping the a-Si:H film in the vicinity of the metal/a-Si:H interface. The highest current levels achieved to date in a-Si:H TFTs have been with doped source/drain contact regions\textsuperscript{44}.

2.3.2 Various types of the a-Si:H TFT

Cross sectional structures of various a-Si:H TFTs are classified in Figure 2.10\textsuperscript{45}. Plasma deposited Si$_3$N$_4$ or SiO$_2$ grown by thermal oxidation on a single-crystal Si and that deposited by low temperature CVD or plasma CVD have been widely investigated as potential gate insulator films.

Doped low resistive single-crystal Si wafers are widely used for substrates to study the basic properties of a-Si:H TFTs. Insulating substrates such as glass and vitreous quartz are also used for integrated devices.

Type (a), (c), and (e) structures in Figure 2.10 have source and drain metallic contacts directly on the a-Si:H active layer, while other types of
Figure 2.9  Field effect measurement test structure or thin film transistor.
Figure 2.10 The cross sectional structures of various a-Si:H TFTs. From Ref. 45.
structures in Figure 2.10 have a highly doped n\textsuperscript{+} layer between the active layer and the metallic contacts.

Type (a) and (b) structures are suitable for studying the basic properties of the device. These structures are easy to fabricate as the insulating film can be prepared without affecting the properties of a-Si:H. However, thermally grown SiO\textsubscript{2} film is degraded in the process of a-Si deposition by a DC-glow discharge, so special care and a thick (1 \, \mu m) film is needed\textsuperscript{46}, while, with the radio-frequency glow discharge deposition of a-Si, the degradation may not be so serious, and a thin (0.1/\mu m) oxide film can be utilized\textsuperscript{47}.

Type (c) and (d) structures are fabricated on insulating substrates, so they are appropriate for integration. However, an insulating film must be deposited on the gate electrode. SiO\textsubscript{2} films grown by plasma CVD or low temperature CVD can be used for the insulating film\textsuperscript{48,49}.

Type (c) and (d) structures are fabricated on insulating substrates, so they are appropriate for integration. However, an insulating film must be deposited on the gate electrode. SiO\textsubscript{2} films grown by plasma CVD or low temperature CVD can be used for the insulating film\textsuperscript{48,49}.

The a-Si:H (non-doped) TFT should operate in both n- and p-channel modes; when a positive gate voltage is applied, electrons are accumulated in the active layer, and when a negative gate voltage is applied holes should be accumulated in the active layer. Matsumura et al. reported that the TFTs which have metallic source and drain contacts on an a-Si:H active layer, can operate in both modes, and that the device which has an n\textsuperscript{+} contact layer connected directly to the channel operates only in the n-channel mode since the n\textsuperscript{+} layers block the hole injection.

The operation speed of an a-Si:H TFT is slow as compared to the conventional MOSFET, due to the low carrier mobilities in a-Si. In general, there are three approaches to increase the current drive capability and thus improve the operation speed of the a-Si:H TFT\textsuperscript{50}. First, the carrier mobilities are increased by improving the a-Si and insulator quality as well as by improving the a-Si—insulator interface quality. Second, the channel length, L, is reduced by invention of a new a-Si:H TFT structure. The typical channel length reported to date is about 10 \, \mu m, which is limited not by the device physics but by the photoetching process for delineating the source and drain. Third, a new circuit is invented for a-Si:H TFTs.

When the channel length is reduced, the intrinsic gate capacitance is also decreased since the gate capacitance is proportional to L. This makes the operation speed of the TFT even faster. The dynamic performance of the TFT may be affected by the transit time of the carriers across the channel. In such a case reduction of L is also very important because the
transit time of the device is proportional to $L^2$.

Very recently, vertical-type amorphous silicon FET has been demonstrated\textsuperscript{50-52}. In this TFT the channel is formed vertically as shown in Figure 2.11, and the current flows along the channel perpendicular to the substrate surface. Thus, the channel length can be reduced less than 1 $\mu$m without serious technical difficulty since $L$ is given by $n$-a-Si layer thickness. The most serious drawback arising from this structure is the increase of off-current due to the space-charge-limited current, and this may be resolved by adding SiN layer to the thin $n$-a-Si bulk as shown in Figure 2.11.

2.4 a-Si:H TFT Applications

Recently, the a-Si:H TFT has shown its important application as an on-board driver for large-area flat-panel displays, particularly liquid-crystal displays in computers and TV sets. Tomihisa et al. reported a 7-in-diagonal active-matrix color LCD with $520 \times 520$ pixels addressed by a-Si TFT\textsuperscript{53}. The a-Si:H material is well-suited for these arrays because it can be easily deposited over large areas, has a high resistivity (a requirement for low leakage current), and has a low mobility (a disadvantage for high frequency operation, but desired for high resolution displays)\textsuperscript{54}. The desired low mobility for high resolution displays stems from the minimum device size causing a lower off-resistance with lower mobility materials than it does with higher mobility materials, thereby permitting the required low off-currents needed for successful display operation.

Figure 2.12 shows a schematic diagram of a number of elements in the LCD panel\textsuperscript{55}. Such arrays typically require a 3 - 6 V ac drive signal without any dc component which tends to degrade the material. The TFT responds to the rms value of the ac signal having a threshold of 1 - 2 V.

One TFT is used to control one element at the cross-point of the array. The TFTs are interconnected by means of X and Y drive buses, (i.e., $G_1$, $G_2$, ... gate lines and $S_1$, $S_2$, ... source lines), linking gate and source contacts, respectively. The drain contact of each TFT is connected to the indium-tin-oxide (ITO) electrodes, $D$. From the section through the panel in Figure 2.12(b), it can be seen that the liquid crystal material is sandwiched between the substrate carrying the TFTs and an ITO coated glass top plate which is normally returned to ground. The liquid crystal element is therefore in series with the drain circuit and behaves electrically as a capacitor $C_{LC}$ with
Figure 2.11  Schematic cross section of the vertical-type a-Si FET. The upper and lower Cr electrodes are for the source and drain, and the left-hand-side Mo electrode is for the gate. From Ref. 55.
Figure 2.12  Example of a-Si:H TFTs in LCD array: (a) schematic layout of an addressable TFT array, (b) cross-section of liquid crystal elements with capacitance $C_{lc}$, (c) cross-section of the a-Si:H TFT, and (d) layout of the a-Si:H TFT. From Ref. 55.
some leakage resistance $R_{LC}$. Part (c) shows a section through an individual a-Si device and part (d) illustrates the design of the TFT in part of the matrix array.

The transient behavior of the TFT in the matrix is determined by the capacitive loading of the liquid crystal element. Panels containing 20x25 elements have been built and successfully run at 80 Hz for 15 months, (i.e., $6 \times 10^{15}$ operations) with no evidence of deterioration in the device transfer characteristics.

Another application for a-Si:H TFTs is in integrated circuits. It is highly desirable to have on-board logic circuits adjacent to the TFT driver matrix and have them implemented in the same technology on the same substrate. Figure 2.13 shows examples of the early inverter circuits\textsuperscript{56,57}. Nara and Matsumara\textsuperscript{58} used circuit (c) which requires two TFTs and an additional supply $V_G$. For their inverter circuit, the maximum oscillation frequency was 500 Hz, the small-signal gain was about 10, and the transfer characteristics are shown in Figure 2.14\textsuperscript{58}.

LeComber et al\textsuperscript{59} chose circuit (a) in Figure 2.13 which uses the load resistor from an integrated a-Si gap cell. Figure 2.15 shows the section and plane view of the inverter circuit\textsuperscript{59}. This circuit is simple and has the advantage that the a-Si resistor requires less space than an TFT load. The transfer characteristics of this inverter circuit are shown in Figure 2.16 and the small-signal gain is lower than that of E/D inverter in Figure 2.14\textsuperscript{59}.

By simple extension of the above basic design, logic circuits such as NAND and NOR gates as well as bi-stable multivibrators have been produced\textsuperscript{59}.

Application of a-Si:H TFTs in three-dimensional circuit was demonstrated by Nara et al\textsuperscript{60}, and inverters and nine-stage ring oscillators were made in three-dimensional form. The inverter circuit is composed of an n-channel driver and a p-channel load TFTs, and its small-signal gain is about 10. The ring oscillator has 60$\mu$s propagation delay per gate.

The a-Si:H TFT is also used in addressable image sensors which use the high photoconductivity and low dark photoconductivity of a-Si:H\textsuperscript{59,61}. A schematic circuit diagram and measured output current from LeComber et al's work are shown in Figure 2.17\textsuperscript{59}. The circuit is composed of a photoconductor, capacitor and field effect transistor. The magnitude of the output current pulse increases with increasing light intensity for gate pulse frequencies of 2, 20, and 40 Hz. The capacitor is charged up when light is
Figure 2.13  Three examples of a-Si:H TFT inverter circuits: (a) and (b) from Ref. 56, and (c) from Ref. 57.
Figure 2.14 The transfer characteristics of E/D type converter. From Ref. 58.
Figure 2.15  Section and plane view of the integrated a-Si:H inverter. From Ref. 59.
Figure 2.16  The transfer characteristics of inverter type (a) in Figure 2.13. (a) single a-Si inverter and (b) three inverters connected in series. From Ref. 59.
Figure 2.17  Circuit of the a-Si image sensor and measured output current as a function of light intensity for various gate pulse frequencies. From Ref. 59.
incident on the photoconductor, and the TFT output current can be read upon application of a clock pulse. The TFT output current is proportional to the incident photon flux on the photoconductor. Snell et al. have dispensed with the capacitor and developed a new vertically integrated image sensing element using a TFT fabricated on top of the a-Si photoconductor.

Although the use of a-Si:H TFTs as switching devices in LCD arrays has been well demonstrated, their use in logic circuits appears to be limited by their slow switching time. A figure of merit characterizing the high-frequency performance of TFT is the gain-bandwidth product, which leads to the maximum operating frequency (defined as the condition when the device is no longer amplifying the input signal) given by

$$f_m = \frac{g_m}{2\pi CWL}$$  \hspace{1cm} (2.5)

In this relation, \(g_m\) is the transconductance, \(C\) is the gate capacitance per unit area, \(W\) is the gate width and \(L\) is gate length. For the conventional expression for \(g_m\), used in MOSFETs,

$$g_m = \frac{CW\mu}{L} V_G$$  \hspace{1cm} (2.6)

where \(\mu\) is the effective field-effect mobility and \(V_G\) is the effective gate voltage, \(f_m\) becomes

$$f_m = \frac{\mu V_G}{2\pi L^2}$$  \hspace{1cm} (2.7)

If \(\mu = 0.1 \text{ cm}^2/\text{V-sec}, V_G = 15 \text{ V}\) and \(L = 4 \mu\text{m}\), a value of \(f_m = 1.5 \text{ MHz}\) is obtained. In practical circuits the response of a-Si:H TFTs is further limited by the time required for the device on-current to charge up circuit capacitances. The charging time can be improved by increasing the on-current, and this can be achieved by optimizing device geometry (i.e., reducing the channel length) and/or optimizing device on-conductance by reducing the density of interface states at the insulator/a-Si interface and
the density of localized states of a-Si. From the properties described above, the a-Si:H TFT is expected to be used in a growing number of applications, in a frequency range approaching 1 MHz.

2.5 References


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CHAPTER 3
A MODEL FOR THE STATIC CHARACTERISTICS OF
PECVD a-Si:H THIN FILM TRANSISTORS

3.1 Introduction

In recent years, the hydrogenated amorphous silicon thin film transistor (a-Si:H TFT) has shown its important application as an on-board switching element for "large-area electronics" such as flat-panel liquid-crystal displays and facsimile devices. In addition, developing a-Si:H TFT logic circuits has become an important new area of investigation because it is highly desirable to have on-board logic circuits adjacent to the TFT driver matrix, and to have them implemented in the same technology on the same substrate. This reduces the number of lead connections to the display which reduces the cost and increases the reliability of the display. As a-Si:H TFT large area electronics applications increase, a more accurate and simplified $I_D$ vs. $V_D$ characteristic model is necessary for predicting circuit performance. Computer aided design (CAD) circuit analysis programs, which are critical to further circuit development, need accurate internal models. Of particular importance is to have equations that can be incorporated into existing computer programs.

Although the study of the static characteristics of a-Si:H TFT is important for understanding, improving, and applying these devices, it is not easy to obtain a simple analytical expression for the $I_D$ vs. $V_D$ characteristics from "first principles", mainly due to the large density of localized states in the mobility gap of amorphous silicon.

Recently, a simple expression was derived for the $I_D$ vs. $V_D$ characteristics of a vacuum deposited hydrogen implanted a-Si:H TFT, which had a large density of localized states. They pointed out that the $I_D$ vs. $V_D$ characteristics can be predicted more precisely by improving the model for the sheet conductance. This modeling technique was later verified for a plasma-enhanced (PE) CVD ambipolar a-Si:H TFT, which had a relatively low density of localized states. Curve-fitting expressions were
developed for the experimental sheet conductance (which was interpolated to $V_D = 0$) in various regions of the gate voltage. Then the empirical expressions were integrated to obtain the $I_D$ vs. $V_D$ characteristics.

In this chapter the basic expressions were derived for the sheet conductance of a PECVD n-channel a-Si:H TFT, and they show very close agreement with the experimental data at small and large gate voltages. The expressions for the sheet conductance are developed on the basis of two assumed energy band models, one for the a-Si bulk and one for the a-Si–SiO$_2$ interface. These basic expressions are then simplified to give two sets of simple analytical formulas for the calculation of $I_D$ vs. $V_D$ for various values of $V_G$.

3.2 Simplified Energy Band Models

Due to its lack of long-range order and many structural defects, amorphous silicon has localized states in the mobility gap which are composed of tail states and defect states. Several energy band models have been proposed for the electronic structure of the amorphous silicon in order to explain the experimental data for the electrical transport properties of amorphous silicon.

Figure 3.1(a) illustrates the simplified CFO energy band model used for the density of the a-Si bulk states, assuming that the density of bulk defect states is nearly constant for the fabricated a-Si:H TFT. However, at the interface between the a-Si bulk and the SiO$_2$ insulator, the extent of disorder of the atomic network and the density of structural defects (e.g., dangling bonds, vacancies, etc.) are expected to increase. Therefore, a different model is needed for the density of interface localized states. It has been previously shown that these interface states play an important role in the performance of TFT's. Previously published models have assumed a constant density of states for the interface states.

Davis and Mott proposed that another band exists at the middle of the mobility gap originating from defects in the atomic random network. Therefore, a simplified Davis-Mott model was assumed for the density of interface states as shown in Figure 3.1(b). The density of defect-states is larger near the middle of the mobility gap because of the increased defect states at the interface. Also, due to the increased extent of the disorder at the interface, the tails of interface localized states extend further into the
Figure 3.1  (a) The simplified CFO model and (b) the simplified Davis-Mott model.
mobility gap than those of bulk localized states.

3.3 Drain Current of the a-Si:H TFT

From the gradual channel approximation, the drain current, $I_D$ is expressed as

$$ I_D = W G_s \frac{dV_o(y)}{dy} $$

where $W$ is the channel width, $G_s$ is the sheet conductance of the channel, and $V_o(y)$ is the potential at the edge of the space-charge layer where there is no band bending, with the assumption that the a-Si layer is thick. Basically, $G_s$ is a direct function of the surface band bending, $\phi_s(y)$, where $\phi_s(y)$ is proportional to $V_G - V_{FB} - V_0(y)$ ($V_{FB}$ is the flat-band voltage). The averaged $G_s$ for the forward and reverse sweeps of the gate voltage can be obtained as a function of $V_G - V_{FB}$ with $V_o$ interpolated to zero by the effect of making $V_D = 0$. By measuring the experimental $G_s$ curves for $V_D$ equal to $-3$, $-1$, $+1$, and $+3$, a two dimensional spline interpolation is used to obtain $G_s$ values at $V_D = 0$. Thus, $G_s$ can be expressed as a function of the parameter $V = V_G - V_{FB} - V_0(y)$, and the $G_s$ vs. $V_G - V_{FB}$ curve is interpreted as a $G_s$ vs. $V$ curve for the general case where $V_0(y) \neq 0$. Equation (3.1) then becomes

$$ I_D = -W G_s(V) \frac{dV}{dy} $$

After integration from the source to the drain, Equation (3.2) becomes

$$ I_D = \frac{W}{l} \int_{V_\beta}^{V_o} G_s(V) dV $$

where $V_\alpha$ and $V_\beta$ are the potentials at the source and drain respectively, and $l$ is the channel length. Thus, the limits of the integration become
\[ V_\alpha = V_G - V_{FB} \]  \hspace{1cm} (3.4)

\[ V_\beta = V_G - V_{FB} - V_D \]

where \( V_D \) is the potential difference between the drain and the source with the source potential being grounded.

### 3.4 Sheet Conductance of the a-Si:H TFT

From Equations (3.3) and (3.4), the drain current, \( I_D \) is expressed as

\[
I_D = \frac{W}{l} \int_{V_G - V_{FB}}^{V_G - V_{FB} - V_D} G_S(V) \, dV. \tag{3.5}
\]

The sheet conductance as a function of \( V \) is shown in Figure 3.2 for an n-channel device.

The basic definitions for the channel configuration and variables for the a-Si:H TFT investigated are illustrated in Figure 3.3(a) and (b). Refer to Figure 5.1(b) for the structure of the TFT, where \( W = 500 \, \mu m \) and \( l = 10 \, \mu m \). The electrostatic potential in the space-charge layer at the point \((x,y)\) in the channel is expressed as \( V(x,y) = V_0(y) + \phi(x,y) \) where \( \phi(x,y) \) is the amount of the band bending in the channel.

The conductance for an element of the channel length \( dy \) and the width \( W \), as shown in Figure 3.3(a), is composed of the flat-band conductance \( \Delta G_o(y,y+dy) \) and the field-induced (enhanced) conductance \( \Delta G(y,y+dy) \) arising from the band bending \( \phi(x,y) \). \( \Delta G_o(y,y+dy) \) can be written as

\[
\Delta G_o(y,y+dy) = (\sigma_{no} + \sigma_{po}) \frac{Wd_a}{dy}
= \sigma T \frac{Wd_a}{dy} \tag{3.6}
\]

where \( \sigma_{no} \) and \( \sigma_{po} \) are the extended state conductances for electrons and holes, respectively. The thickness of a-Si:H film is \( d_a \) (\( = 3700 \, \text{Å} \) for the
Figure 3.2  The sheet conductance of an a-Si:H TFT: experimental (circles), numerically solved (dashed line), and analytically solved (solid line) data.
Figure 3.3 (a) Geometric definitions and (b) energy band of an a-Si:H TFT.
modeled device). The enhanced conductance is obtained by

\[
\Delta G(y,y+dy) = \frac{W}{dy} \left[ \sigma_{no} \int_{0}^{d_a} \frac{e^{\phi(x,y)/kT} - 1}{dx} \right. + \sigma_{po} \int_{0}^{d_s} \frac{e^{-\phi(x,y)/kT} - 1}{dx} \right].
\] (3.7)

Changing the variable of integration yields

\[
\Delta G(y,y+dy) = \frac{W}{dy} \left[ \sigma_{no} \int_{\phi(d_a,y)}^{\phi(y)} \frac{e^{\phi(x,y)/kT} - 1}{\partial \phi / \partial x} \right. + \sigma_{po} \int_{\phi(d_a,y)}^{\phi(y)} \frac{e^{-\phi(x,y)/kT} - 1}{\partial \phi / \partial x} \right].
\] (3.8)

where \( \phi_s(y) \) equals the surface band bending, \( \phi_s(y) = \phi(0,y) \) (see Figure 3.3(b)). In Equations (3.7) and (3.8) it is assumed that the extended state conduction obeys Maxwell-Boltzman statistics and the mobilities are not a function of electric field. For an n-channel device, the second term expressing the enhanced hole conduction is negligible, and the total sheet conductance, \( G_s \) is approximated as

\[
G_s = \sigma_T d_a - \sigma_{no} \int_{\phi(d_a)}^{\phi(y)} \frac{e^{\phi(x,y)/kT} - 1}{\partial \phi / \partial x} \ d\phi
\] (3.9)

where the \( y \)-dependence of \( \phi \) is not shown because \( V_D \) is interpolated to zero.
For an ambipolar device, the enhanced hole conduction can be dominant over the enhanced electron conduction.

In order to solve the integral in Equation (3.9), the expression for \( \phi(x) \) is needed. The band bending \( \phi(x) \) obeys Poisson's equation

\[
\frac{\partial^2 \phi(x)}{\partial x^2} = \frac{-\rho(x)}{\epsilon_0 K_s}.
\] (3.10)

For the case of an enhanced n-channel, the excess density of electrons are trapped in the localized states, which are assumed to be much larger than the enhanced density of free electrons. Therefore, the free electron term of
\( \rho(x) \) is ignored. This assumption will be verified later in the section V. When the Fermi level is in the uniform bulk-defect states, \( N_t \) of Figure 3.1(a), \( \rho(x) \) is related to the \( N_t \) by

\[
\rho(x) = -qN_t \phi(x) \quad (3.11)
\]

for a symmetrical Fermi function. Solving Poisson's equation yields

\[
\frac{\partial \phi}{\partial x} = -L \phi \quad (3.12a)
\]

\[
\phi(x) = \phi_s e^{-Lx} \quad (3.12b)
\]

where

\[
L = \left( \frac{N_t q}{\epsilon_0 K_s} \right)^{1/2} \quad (3.13)
\]

Substituting Equation (3.12a) into Equation (3.9) results in

\[
G_s = \sigma_T d_s + \frac{\sigma_{no}}{L} \int_0^{\phi_s} \frac{[e^{q\phi/kT} - 1]}{\phi} d\phi . \quad (3.14)
\]

It is necessary to relate \( \phi_s \) to the applied gate voltage, \( V_G \), in order to solve Equation (3.14) further. With \( V_0(y) \) interpolated to zero by the effect of making \( V_D = 0 \), the surface band bending, \( \phi_s \) is related to the applied gate voltage by

\[
V_G = V_{FB} + V_i + \phi_s \quad (3.15)
\]

where \( V_i \) is the voltage drop across the insulator. To obtain a solution, it is necessary to derive \( \phi_s \) in terms of the gate voltage by eliminating \( V_i \). From the continuity of the dielectric displacement at the a—Si—SiO₂ interface, it is required that
\[
\varepsilon_0 K_s F_s - \varepsilon_0 K_{ox} F_i = Q_s \tag{3.16}
\]

where \( F_s (F_i) \) is the electric field at the interface in the semiconductor (insulator), \( Q_s \) is the interface surface charge density, and \( K_{ox} \) is the dielectric constant of the insulator. When the Fermi level lies in the higher surface-defect states of Figure 3.1(b), the surface charge density, \( Q_s \) is related to the surface band bending \( \phi_s \) by

\[
Q_s = -q N_{s1} \phi_s \tag{3.17}
\]

where \( N_{s1} \) is the high density of surface-defect states (\#/cm\(^2\)-eV). From Equation (3.12a), \( F_s \) is defined as

\[
F_s = -\frac{\partial \phi}{\partial x} \bigg|_{x=0} = L \phi_s . \tag{3.18}
\]

Then, from Equations (3.16), (3.17), and (3.18), one finds

\[
F_i = \frac{1}{\varepsilon_0 K_{ox}} \left( \varepsilon_0 K_s L + q N_{s1} \right) \phi_s . \tag{3.19}
\]

Solving for \( V_i \) yields

\[
V_i = d_{ox} F_i = \frac{d_{ox} K_s}{K_{ox}} \left( L + \frac{q N_{s1}}{\varepsilon_0 K_s} \right) \phi_s \tag{3.20}
\]

where \( d_{ox} \) is the thickness of the insulator. From Equations (3.15) and (3.20), one obtains
\[
\phi_s = \frac{K_{ox}}{K_{ox} + K_s d_{ox} \left( L + \frac{qN_{s1}}{\varepsilon_0 K_s} \right)} (V_G - V_{FB}). \quad (3.21)
\]

To simplify the \( \phi_s \) expression, define \( K_1 \) as

\[
K_1 = K_{ox} + K_s d_{ox} \left( L + \frac{qN_{s1}}{\varepsilon_0 K_s} \right). \quad (3.22)
\]

Note that \( L \) increases as the square root of \( N_t \) and \( K_1 \) increases linearly with \( L \) and \( N_{s1} \). Then, the surface potential can be written in terms of \( V_G \) or \( V \) as

\[
\phi_s = \frac{K_{ox}}{K_1} (V_G - V_{FB}) = \frac{K_{ox}}{K_1} V. \quad (3.23)
\]

In order to obtain a closed form solution for \( G_s \), the integral of Equation (3.14) was simplified in the pure arithmetic sense as follows:

\[
\int_{\phi(d_s)}^{\phi} \frac{[e^{q\phi/kT} - 1]}{\phi} \, d\phi \approx S \int_{\phi(d_s)}^{\phi} e^{q\phi/kT} \, d\phi
\]

\[
= \frac{S kT}{\alpha q} \left[ e^{q\phi_s/kT} - e^{q\phi(d_s)/kT} \right]. \quad (3.24)
\]

where \( S \) and \( \alpha \) are curve-fitting parameters to a numerical calculation of the integral. For a thick amorphous silicon layer, the exponent of the second term in Equation (3.24) is very small since \( \phi(d_s) \simeq 0 \), and Equation (3.24) can be further simplified to

\[
\frac{S kT}{\alpha q} \left[ e^{q\phi_s/kT} - 1 \right]
\]

The curve fitting parameters \( S/\alpha = 32 \) and \( \alpha = 0.77 \) were determined to
give the best fit to the numerical calculation of the integral on the left hand side of Equation (3.24) for the region of small $\phi_s$ as shown in Figure 3.4. Hence, Equation (3.14) is approximated as

$$G_S = \sigma_T d_a + B_1 [e^{0.77 q\phi_s/kT} - 1]$$  \hspace{1cm} (3.25)

where

$$B_1 = 32 \frac{\sigma_0 kT}{Lq}.$$  

The value of $B_1$ can be obtained by extrapolating the experimental $G_s$ data in region I of Figure 3.2 to $V = 0$. Thus, from Equations (3.23) and (3.25), one can find the expression for $G_S$ as a function of $V$,

$$G_S = \sigma_T d_a + B_1 \left[ \exp \left( \frac{0.77 qK_{ox}}{kT_1} V \right) - 1 \right].$$  \hspace{1cm} (3.26)

When the applied gate voltage is increased to make $V > V_1$ in Figure 3.2, the Fermi level enters the low surface-defect states and the $Q_S$ is related to the $\phi_s$ by

$$Q_s = -qN_{s2} \phi_s - q\phi_{s1}(N_{s1} - N_{s2})$$  \hspace{1cm} (3.27)

where $\phi_{s1}$ is the surface band bending when the high surface-defect states, $N_{s1}$ are completely filled, hence

$$\phi_{s1} = \frac{K_{ox}}{K_1} V_1.$$  

Following similar procedure as above, one can find a new relationship between $\phi_s$ and $V$,
Figure 3.4  Numerical integration (triangles) and approximate calculations (solid and dashed lines) of Equation (3.24).
\[ \phi_s = \frac{K_{ox}}{K_2} [V - \Delta V_{FB}] \]  

(3.28)

where \( K_2 \) is defined as

\[ K_2 = K_{ox} + K_s d_{ox} \left( L + \frac{qN_{s2}}{\epsilon_o K_s} \right) \]  

(3.29)

and \( \Delta V_{FB} \) is defined as

\[ \Delta V_{FB} = \frac{qK_{ox}}{C_{ox} K_1} (N_{s1} - N_{s2}) V_1 . \]  

(3.30)

The oxide capacitance per unit area is \( C_{ox} \). Note that the shift of the flat-band voltage, \( \Delta V_{FB} \) originates from the different densities of surface-defect states at large and small band bending.

For the region of large \( \phi_s \), the integral of Equation (3.24) is best fitted with parameters \( S/\alpha = 6 \) and \( \alpha = 0.95 \) as shown in Figure 3.4, and \( G_S \) can be approximated as

\[ G_S = P \ e^{0.95q\phi_s/kT} \]  

(3.31)

where

\[ P = 6 \ \frac{\sigma_{ao} kT}{Lq} . \]

When the applied gate voltage is further increased to make \( V > V_2 \) in Figure 3.2, the Fermi level enters the exponentially increasing surface-tail states. It was assumed that the density of surface-tail states can be expressed as:
where \( \beta = 1/(kT_0) \) and \( T_0 \) is the characteristic temperature. Then, by employing Equations (3.27), (3.32), and the zero-temperature approximation, the relation of \( Q_s \) to \( \phi_s \) is obtained as follows:

\[
Q_s = -q \int_0^\phi_s N_s \, d\phi_s
\]

\[
= -q \left\{ N_{s2} \phi_{s2} + (N_{s1} - N_{s2}) \phi_{s1} + \frac{N_{s2}}{\beta} \left[ e^{\beta(\phi_s - \phi_c)} - 1 \right] \right\} \quad (3.33)
\]

where \( \phi_{s2} \) is the surface band bending when the low surface-defect states \( (N_{s2}) \) are all filled. Also

\[
\phi_{s2} = \frac{K_{ox}}{K_2} (V_2 - \Delta V_{FB}).
\]

From Equations (3.16), (3.18), and (3.33), a transcendental equation for \( \phi_s \) is obtained as

\[
V = \frac{1}{C_{ox}} (Q_F - \frac{qN_{s2}}{\beta}) + (1 + \frac{d_{ox}K_s L}{K_{ox}}) \phi_s + \frac{qN_{s2}}{C_{ox}} e^{\beta(\phi_s - \phi_c)} \quad (3.34)
\]

where \( Q_F \) is defined as

\[
Q_F = q[N_{s2} \phi_{s2} + (N_{s1} - N_{s2}) \phi_{s1}].
\]

Equation (3.34) can be solved numerically for \( \phi_s \), and Equation (3.31) is again used for the calculation of the sheet conductance.
3.5 Parameter Determination

In Figure 3.4 the slopes \((a_1 \text{ and } a_2)\) of the experimental data (the circles) on an exponential scale in regions I and II, respectively, can be found by using a "least squares" fit to the experimental data. Hence, from Equations (3.26) and (3.31), one can compare the values of the slopes and obtain the values of \(K_1\) and \(K_2\) as follows:

\[
K_1 = \frac{0.77 qK_{ox}}{a_1 kT} \quad (3.35)
\]

\[
K_2 = \frac{0.95 qK_{ox}}{a_2 kT} \quad (3.36)
\]

From Equations (3.22), (3.29), (3.35), and (3.36), one can find

\[
N_{s1} - N_{s2} = \frac{\epsilon_o (K_1 - K_2)}{qd_{ox}} \quad (3.37)
\]

Then, the value of \(\Delta V_{FB}\) can be determined from Equations (3.30) and (3.37).

In Figure 3.2 the extrapolated value of the experimental data in region II to \(V = 0\), which is defined as \(B_2\), is compared with Equation (3.31) to give

\[
L = \frac{6 \sigma_{nc} kT}{B_2 q} \exp \left( \frac{-0.95 qK_{ox} \Delta V_{FB}}{kTK_2} \right) \quad (3.38)
\]

Thus, the value of \(L\) can be determined if the value of \(\sigma_{no}\) is known. It was found that \(\sigma_{no} = 9.7 \times 10^{-11} (\Omega\cdot\text{cm})^{-1}\) gave the closest result to the experimental data as will be shown in the following section. Now the values of \(N_{s1}\) and \(N_{s2}\) can be obtained from Equations (3.29), (3.35), (3.36), and (3.38) as follows:
\[ N_{s1} = \frac{\varepsilon_{0}K_{s}}{q} \left[ \frac{K_{ox}}{K_{s}d_{ox}} \left( \frac{0.77q}{a_{1}kT} - 1 \right) - L \right] \] (3.39)

\[ N_{s2} = \frac{\varepsilon_{0}K_{s}}{q} \left[ \frac{K_{ox}}{K_{s}d_{ox}} \left( \frac{0.95q}{a_{2}kT} - 1 \right) - L \right]. \] (3.40)

The value of \( N_t \) can be determined from Equations (3.13) and (3.38). The value of \( B_{1} \) in Equation (3.25) can also be found by using Equation (3.38) with a small discrepancy from the extrapolated one. For the modeled device, it was found that \( \Delta V_{FB} = 3.6 \) volts, \( 1/L = 560\lambda \), which is much smaller than the thickness of the a-Si layer (= 3700\lambda), \( N_{s1} = 6.6 \times 10^{12}(\#/\text{cm}^{2}-\text{eV}) \), \( N_{s2} = 3.5 \times 10^{12}(\#/\text{cm}^{2}-\text{eV}) \), and \( N_{t} = 2.1 \times 10^{17}(\#/\text{cm}^{3}-\text{eV}) \). All these numbers are very reasonable when compared to other published values.

### 3.6 Sheet Conductance for \( V > V_2 \)

Equations (3.23) and (3.28) are used for the calculation of the surface band bending when \( V \leq V_1 \) and \( V_1 < V \leq V_2 \), respectively, in Figure 3.2. For the region of \( V > V_2 \), the \( \phi_{s} \) can be calculated by solving the transcendental equation, Equation (3.34), numerically. The numerical result is shown by the solid line in Figure 3.5.

In order to have an analytical solution, Equation (3.34) needs to be simplified. The second and third terms in Equation (3.34) are dependent on \( V \) and their values are obtained by numerical calculation as shown in Figure 3.6. One can see that the second term (the dashed line) is quite flat as compared with the third term (the solid line). Therefore, \( \phi_{s} \) of the second term in Equation (3.34) can be substituted as some average value, \( \phi_{a} \), and Equation (3.34) is then solved to give

\[ \phi_{s} = \frac{1}{\beta} \ln \left[ \frac{C_{ox}^{\beta}}{qN_{s2}(V - V_{T})} \right] + \phi_{s2} \] (3.41)

where
Figure 3.5  The surface band bending numerically solved (solid line) from Equation (3.34) and analytically solved (dashed) from Equation (3.41) for $V > V_2$. 
Figure 3.6  The comparison of the second term (dashed line) and the third term (solid line) of Equation (3.34).
\[ V_T = \frac{1}{C_{ox}} \left( Q_F - \frac{qN_{s2}}{\beta} \right) + \left( 1 + \frac{d_{ox}K_L}{K_{ox}} \right) \phi_s. \]  

(3.42)

Substituting Equation (3.41) into Equation (3.31) yields

\[ G_s = A \left[ \beta(V - V_T) \right]^{\frac{0.95q}{kT^\beta}} \]  

(3.43)

where

\[ A = \frac{6 \sigma_{no}kT}{Lq} \exp \left( \frac{0.95q\phi_{s2}}{kT} \right) \left( \frac{C_{ox}}{qN_{s2}} \right)^{\frac{0.95q}{kT^\beta}}. \]

The numerical values of \( \beta \) and \( V_T \) can be determined by fitting the sheet conductance curve to the experimental data on the square root scale as shown in Figure 3.7. For the particular modeled device, it was found that \( \beta = 18.5 \) and \( V_T = V_2 = 22 \) gave the best fitting to the experimental data at room temperature. From Equation (3.41), the corresponding surface band bending is shown by the dashed line in Figure 3.5.

In order to have a continuous expression for the \( G_s \) in all the regions of operation, the sheet conductances in regions II and III are combined together by employing Equations (3.28), (3.31) and (3.43) to yield

\[ G_s = D \ln \left[ \exp \left( \frac{G_s(3.37)z}{D} \right) + \exp(a_2(V - V_2)) \right] \]  

(3.44)

where

\[ z = 0 \quad \text{for} \quad V \leq V_T \]
\[ z = 1 \quad \text{for} \quad V > V_T, \]

and
Figure 3.7 The sheet conductance on the square root scale: experimental (circles) and numerically solved (solid line) data, and the dashed line is from Equation (3.43).
\[ D = P \exp[a_2(V_2 - \Delta V_{FB})]. \]

The result is shown by the solid line in Figure 3.2 with a very close agreement between the model and the experimental data. The dashed line in Figure 3.2 shows the numerical calculation of Equations (3.31) and (3.34) for comparison.

Since the exact values of the \( \phi_s \) have been obtained, it is possible to examine the assumption that the density of free electrons is much smaller than that of electrons trapped in the localized states. The free electron density \( (n_f) \) can be calculated by

\[ n_f = n_i e^{q\phi_s/kT}. \]  \hspace{1cm} (3.45)

Then, from Equations (3.12b) and (3.45), one obtains

\[ n_f = n_i \exp \left( \frac{q\phi_s}{kT} e^{-L x} \right). \]  \hspace{1cm} (3.46)

The density of electrons trapped in the a-Si bulk defect states \( (n_b) \) can be determined from Equations (3.11) and (3.12b) as

\[ n_b = N_t \phi_s e^{-L x}. \]  \hspace{1cm} (3.47)

Figure 3.8 shows that \( n_b \) is much larger than \( n_f \) for most of the operating range, and \( n_f \) is larger than \( n_b \) only very near the a-Si—SiO\(_2\) interface when \( V \gtrsim 28 \) volts. Detailed calculations show that \( n_f \) is larger than \( n_b \) for \( x \leq 42 \AA \) when \( V = 36 \) volts. Thus, the magnitude of the sheet density of free electrons \( (N_f) \) should be compared to the density of electrons trapped in the interface localized states \( (N_s) \).

In order to calculate \( N_f \), the surface band bending expressed in Equation (3.12b) was approximated by \( \phi_s(1 - L x) \). Then the expression for \( N_f \) is obtained by
Figure 3.8  Comparison between the free electron density (lower curves) and the a-Si bulk trapped electron density (upper curves).
\[ N_f = \int_{0}^{d_n} n_r \, dx \]

\[ = \frac{n_k T}{q \phi_o L} \left[ e^{q \phi_o / kT} - 1 \right]. \] (3.48)

\( \mu_n = 1 \, \text{cm}^2/\text{V-s} \) was used to calculate the value of \( n_i \). The magnitude of the \( N_f \) can be determined from Equations (3.17), (3.27), and (3.33). The comparison between the \( N_f \) and \( N_s \) is shown in Figure 3.9. Indeed, the magnitude of \( N_f \) is much smaller than that of \( N_s \) through all the region of \( V \). If \( \mu_n = 10 \, \text{cm}^2/\text{V-s} \) is used, then \( n_r \) is reduced by an order of magnitude and the assumption made in Equation (3.11) is verified with even more assurance.

### 3.7 Calculation of the Drain Current

The drain current can be calculated by substituting the different expressions of \( G_s \) for various regions of \( V \) into Equation (3.5). However, it is necessary to simplify the sheet conductance in order to make the model more suitable for computer aided design (CAD) circuit analysis programs. When \( V_G - V_{FB} < V \_T \), the drain current is negligible irrespective of the drain voltage for an n-channel device, and so this region can be considered as an extension of the region II in terms of the calculation of \( I_D \).

When \( V_G - V_{FB} < V_T \) and \( V_G - V_{FB} - V_D > 0 \), the drain current can be obtained by substituting Equation (3.31) into Equation (3.5) to yield

\[ I_D = \frac{WP}{L \alpha_2} e^{a_3(V_G - V_{FB} - V_{RD})} \left[ 1 - e^{-a_4 V_{RD}} \right]. \] (3.49)

When \( V_G - V_{FB} < V_T \) and \( V_G - V_{FB} - V_D < 0 \), the enhanced channel is beyond the pinch-off point at the drain end of the channel. Now the lower limit of the integration in Equation (3.5) should be \( V = 0 \), and Equation (3.49) becomes
Figure 3.9  Comparison between the surface trapped electron density (solid line) and the sheet density of free electrons (dashed line).
Thus, \( V_{DSAT} \) can be defined as

\[ V_{DSAT} = V_G - V_{FB}. \]

Figure 3.10 shows a close agreement between the model and the experimental data for the region of \( V_G - V_{FB} < V_T \).

When \( V_G - V_{FB} \geq V_T \) and \( V_G - V_{FB} - V_D \geq V_T \), Equation (3.43) is substituted into Equation (3.5) to yield

\[ I_D = \frac{W_A}{l_\eta} \beta^{n-1} \left[ V_{GT}^{n} - (V_{GT} - V_D)^n \right] \quad (3.51) \]

where

\[ \eta = \frac{0.95 q}{kT \beta} + 1 \]

\[ V_{GT} = V_G - V_{FB} - V_T. \]

\( \eta = 2.98 \) was found for the particular device modeled.

When \( V_G - V_{FB} \geq V_T \) and \( V_G - V_{FB} - V_D \leq V_T \), the lower limit of the integration in Equation (3.5) should be \( V = V_T \), and Equation (3.51) becomes

\[ I_{DSAT} = \frac{W_A}{l_\eta} \beta^{n-1} V_{GT}^{n} \quad (3.52) \]

Here, \( V_{DSAT} \) is defined as \( V_{GT} \). In Figure 3.11 a close agreement is again shown between the model and the experimental data for the region of \( V_G - V_{FB} \geq V_T \). Equations (3.49), (3.50), (3.51), and (3.52) can be easily programmed into a CAD program for calculating \( I_D \) with different values of \( V_G \) and \( V_D \).
Figure 3.10 Experimental (circles) and modeled (solid line) output drain characteristics for $V_G - V_{FB} < V_T$. 

$V_G = 18$

$V_G = 15$

$V_G = 12$

$V_G = 9$

$V_G = 6$
Figure 3.11 Experimental (circles) and modeled (solid line) output drain characteristics for $V_G - V_{FB} \geq V_T$. 
In summary of this chapter, accurate analytical expressions have been derived for the sheet conductance of the a-Si:H TFT on the basis of two different energy band models, one for the a-Si bulk and one for the a-Si—SiO₂ interface. A simplified CFO model was used for the a-Si bulk states, and a simplified Davis-Mott model was used for the a-Si—SiO₂ interface states. The physical parameters used in the energy band models of a-Si:H TFT can be determined from the experimental sheet conductance data.

The basic expressions for the sheet conductance were simplified, and the simplified formulas were used for the calculation of the drain current and show close agreement with the experimental data. The parameters used in the energy band models show clearly their effects in the \( I_D \) vs. \( V_D \) characteristics through the simplified formulas.

The analytical model for the sheet conductance was applied to the development of the n-channel a-Si:H TFT model. The simplified model for \( G_s \) can be used to calculate the \( I_D \) vs. \( V_D \) characteristics. By using similar procedures, one can develop another set of models for the p-channel a-Si:H TFT. The resultant equations are easily employed in many existing CAD circuit analysis programs for predicting circuit behavior.

3.8 References


CHAPTER 4
AMBIPOLAR PECVD a-Si:H THIN FILM TRANSISTORS

4.1 Introduction

An a-Si:H TFT, with ohmic source/drain contact regions and a high quality gate insulator, shows ambipolar characteristics. This device is capable of operating in either the n-channel or the p-channel regime (first and third quadrant of $I_D$ vs. $V_D$ drain output characteristic, respectively). At large drain voltages the ambipolar TFT can have both electrons and holes modulating the channel conductance. Evidence of the ambipolar behavior of a-Si:H TFTs was observed by Neudeck and Malhotra in 1975 and a formal investigation of this property was published by Pfleiderer et al in 1985.

This chapter describes the physical mechanisms of ambipolar TFTs and presents an improved model. The improved model results from extending the work for an n-channel device done in Chapter 3 and systematically incorporating the effects of the different n-channel and p-channel regime flat-band voltages into the interpolated sheet conductance.

4.2 Ambipolar Property of an a-Si:H TFT

When $V_D < V_G - V_{FB}$, the mobile carriers are primarily enhanced electrons through the entire channel region, and the energy band profile is shown in Figure 4.1. The flat-band voltage, therefore, should be that of an n-channel device, $V_{FBn}$. There is no band bending at the drain end when $V_D = V_G - V_{FB}$ as shown in Figure 4.2.

When $V_D > V_G - V_{FB}$, the flat-band point is located within the channel region as shown in Figure 4.3, and there are additional carriers enhanced from the flat-band point to the drain end. These additional carriers are holes for this bias condition. Therefore, a p-channel regime is developed from the flat-band point in the channel to the drain end. The TFT now shows ambipolar characteristics.
Figure 4.1 The energy band profile of an a-Si:H TFT when $V_D < V_G - V_{FB}$. 

$V_G = 20 \text{ V} \quad V_D \approx 15 \text{ V}$
Figure 4.2 The energy band profile of an a-Si:H TFT when $V_D = V_G - V_{FB}$. 
Figure 4.3 The energy band profile of an a-Si:H TFT when $V_D > V_G - V_{FB}$. 

$V_G = 5 \text{ V} \quad V_D = 30 \text{ V}$
The physical mechanism of carrier flow in an ambipolar TFT is explained as follows. Electrons from the n-channel regime are swept from the flat-band point in the channel toward the drain contact by the high electric field through the high resistivity, nearly intrinsic a-Si:H bulk region. The drain to source voltage is distributed down the channel from the drain to source. Likewise, holes from the p-channel regime are also swept from the flat-band point toward the source contact by a high electric field through the a-Si:H bulk region. Due to the large density of traps of the a-Si:H bulk, recombination of electrons and holes is expected to occur in the a-Si:H bulk region. The TFT now is in a "pure" ambipolar mode of operation. At the drain voltage where the p-channel regime has been developed, the current component from electrons is almost saturated and the current component from holes increases rapidly with additional drain voltage. Similar mechanisms, as explained above, also occur for the "pure" ambipolar operation of the p-channel device at large |V_D|. For the p-channel regime at the drain end, the flat-band voltage should be that of a p-channel device, V_{FBp}.

4.3 Sheet Conductance of an Ambipolar a-Si:H TFT

The averaged G_s for the forward and reverse sweeps of the gate voltage can be obtained as a function of V_G—V_{FB} with V_o interpolated to zero by the effect of making V_D = 0 as shown in Figure 4.4. By measuring the experimental G_s curves for V_D equal to −3, −1, +1, and +3, a two dimensional spline interpolation is used to obtain G_s values at V_D = 0.

The solid lines are for forward and reverse measurement sweeps and the dashed line is for average of forward and reverse sweeps. In Chapter 3 we have derived accurate expressions for the sheet conductance of an n-channel device on the basis of two different energy-band models, one for the a-Si bulk and one for the a-Si—SiO₂ interface. If this work is extended into an ambipolar operation of a-Si:H TFT, then the expressions for G_s, in the various regions of V, can be defined as follows where numerical values of the parameters used in Equations (4.1) to (4.4) can be obtained by curve-fitting of G_s to the experimental data as shown in Figure 4.5:

\[ G_s = \sigma_T d_s + B_{nl}[e^{a_n V} - 1] \] (4.1)
Figure 4.4 Experimental transfer curve of an a-Si:H TFT with $V_D = 0$ V: The solid lines are for forward and reverse measurement sweeps and the dashed line is for average of forward and reverse sweeps.
Figure 4.5 The experimental (circles) and calculated (solid line) sheet conductances of an a-Si:H TFT.
for $0 \leq V < V_{n1}$ where the extended state conductance is $\sigma_T$ and the thickness of a-Si:H film is $d_a$,

$$G_S = D_n \ln \left[ \exp \left( \frac{A_n [\beta_n (V - V_{Tn})]^{(n_n-1)} z_n}{D_n} \right) + \exp (a_{n2} (V - V_{n2})) \right]$$

(4.2)

for $V_{n1} \leq V$ where $z_n = 0$ for $V \leq V_{Tn}$, $z_n = 1$ for $V > V_{Tn}$, and $D_n = B_{n2} \exp (a_{n2} V_{n2})$,

$$G_S = \sigma_T d_a + B_{p1} [e^{-a_{p1} V} - 1].$$

(4.3)

for $V_{p1} \leq V < 0$,

$$G_S = D_p \ln \left[ \exp \left( \frac{A_p [\beta_p (V_{Tp} - V)]^{(n_p-1)} z_p}{D_p} \right) + \exp (a_{p2} (V_{p2} - V)) \right]$$

(4.4)

for $V < V_{p1}$ where $z_p = 0$ for $V \geq V_{Tp}$, $z_p = 1$ for $V < V_{Tp}$, and $D_p = B_{p2} \exp (-a_{p2} V_{p2})$. The subscripts, n and p, denote the n-channel and the p-channel regimes, respectively, and $\eta_{n(p)}$ was defined as

$$\eta_{n(p)} = \frac{0.95 q}{kT \beta_n(p)} + 1.$$

The result is shown by the solid line in Figure 4.5 with very close agreement to the experimental sheet conductance data.
4.4 Shift of Flat-Band Voltages

The difference between $V_{FBn}$ and $V_{FBp}$ results from trapping and detrapping of charge carriers in a-Si:H and the SiO$_2$ insulator. Electrons are trapped in the n-channel regime, and holes are trapped in the p-channel regime. Thus, $V_{FBn}$ is more positive than $V_{FBp}$. This difference in the flat-band voltages should be incorporated into the $G_S$ vs. $V$ curve to obtain a better correspondence between the experimental data and the calculated values from Equation (3.4.1).

The difference between $V_{FBn}$ and $V_{FBp}$, $\Delta V_{FB}$, can be measured from the hysteresis in the $G_S$ vs. $V_G$ curve as illustrated in Figure 4.4. The flat-band voltages were obtained as an algebraic minimum of $G_S$. In Figure 4.4 if we let

$V_{10} = V_{FBn} - V_{FB}$

$V_{20} = V_{FBp} - V_{FB}$

then

$$\Delta V_{FB} = V_{10} + |V_{20}|$$

(4.5)

which is the difference in the two flat-band voltages.

In order to include the effect of channel conversion from n-type to p-type, the $G_S$ vs. $V$ curve in Figure 4.4 is modified as follows. The left portion of $G_S$ vs. $V$ curve, corresponding to the p-channel regime, is shifted left by $|V_{20}|$. The right portion of the curve, corresponding to the n-channel regime, is shifted to the right by $V_{10} = \Delta V_{FB} - |V_{20}|$, keeping $\Delta V_{FB}$ at a fixed value. The modified $G_S$ vs. $V$ curve is shown in Figure 4.6.

The drain current of the a-Si:H TFT can now be calculated by substituting the expression for $G_S$ into Equation (3.4.1). One has to choose a proper expression for $G_S$ out of Equations (4.1) to (4.4) according to the limits of the integration in Equation (3.5).

For the a-Si:H TFT device under consideration ($V_{FBn} = -5$ volts, $V_{FBp} = -7$ volts), selecting $V_{10} = 0.1$ volts and $|V_{20}| = 1.9$ volts and keeping $\Delta V_{FB} = 2$ volts gave the best comparison of the modeled output.
Figure 4.6  Unshifted (dashed line) and shifted (solid line) sheet conductances of an a-Si:H TFT.
characteristics with the experimental data. As shown in Figure 4.7, the results show a very close agreement between the modeled curves and the experimental data for the forward (n-channel) mode of operation.

Results of the p-channel device are shown in Figure 4.8. Selecting $V_{10} = 0.7$ volts and $|V_{20}| = 1.3$ volts and keeping $\Delta V_{FB} = 2$ volts gave excellent results between the modeled curves and the experimental data.

The different values of $V_{10}$ and $|V_{20}|$ for forward and reverse modes of operation have resulted from the different mechanisms of charge trapping and detrapping in the a-Si bulk and the insulator. It should be noted that the methods used to obtain the experimental $G_S$ function can never be made exactly the same as used in TFT theory; except in the case where no charge trapping can occur.

In summary of this chapter, the static output characteristics of an ambipolar PECVD a-Si:H TFT have been successfully modeled by first obtaining an analytical expression for the sheet conductance and then performing the integration to calculate the drain current. The model presented includes a systematic method for incorporating the effects of the different n-channel and p-channel regime flat-band voltages in the interpolated sheet conductance. The model shows very close agreement with the experimental output characteristics over many orders of magnitude of the drain current in both the forward and reverse modes of operation. Because the model includes analytic expressions for the drain current, it readily lends itself to CAD circuit analysis programs.
Figure 4.7 Experimental (symbols) and modeled (solid lines) forward drain output characteristics of an a-Si:H TFT.
Figure 4.8 Experimental (symbols) and modeled (solid lines) reverse drain output characteristics of an a-Si:H TFT.
4.5 References


CHAPTER 5
A NOVEL CMOS-LIKE AMBIPOLAR a-Si:H TFT INVERTER CIRCUIT

5.1 Introduction

The developing of TFT logic circuits, to reduce the number of required leads to be attached to a flat-panel liquid-crystal display, has become an important issue to commercial applications. The basic building block of most logic circuits is the simple inverter circuit. Enhancement-depletion (E/D)\(^1\) and enhancement-enhancement (E/E)\(^2\) (driver/load devices) type inverter circuits using a-Si:H TFTs have been investigated recently by several authors. However, complementary type inverter circuits employing the n-channel and p-channel ambipolar nature of a-Si:H TFTs has not previously been reported in the literature.

In Chapter 4 it was shown that an a-Si:H TFT, with ohmic source/drain contact regions and a high quality SiO\(_2\) gate insulator, can have ambipolar characteristics. This device is capable of operating in either or both the n-channel and the p-channel regimes. In this chapter the ambipolar a-Si:H TFTs are used to make a complementary inverter circuit. The driver and load ambipolar a-Si:H TFTs are fabricated identically at the same time; therefore requiring only one device type and no extra fabrication processes. A device model which was developed in Chapter 4 for the drain current of the ambipolar a-Si:H TFT is used to predict the transfer characteristics of the CMOS-like inverter circuit. The loadlines of the CMOS-like inverter circuit are obtained from the model for the drain current, and the transfer curve of the inverter circuit is graphically determined from the operating points of the loadlines. The transfer curve is then compared to the experimentally measured values.

The inverter circuit is the basic building block of most logic circuits. In this chapter an accurate set of equations is developed for modeling the complementary load a-Si:H TFT inverter circuit. These equations are also important in designing the devices to be used in more complex logic circuits.
The expressions for the sheet conductance of the ambipolar a-Si:H TFT are simplified in the various regions of operation. The sheet conductance function is calculated in a piecewise fashion, using different approximations in different regions of operation. Then, additional simplifications are performed for the expressions of the drain current in order to analytically calculate the transfer curve of the CMOS-like inverter circuit.

It will be also shown that the operating characteristics of the CMOS-like inverter circuit can be improved by shifting the flat-band voltages of both the driver and load TFTs together. By making the flat-band voltages less negative, the noise margin is increased and the switching speed is enhanced.

5.2 Simplified Expressions of the Sheet Conductance

From Section 3.4, the drain current, \( I_D \) is expressed as

\[
I_D = \frac{W}{l} \frac{V_o}{v^*} \int_{V_g - V_{FB}}^{V_g} G_S(V) \, dV
\]  

(5.1)

where the limits of the integration are \( V_o = V_G - V_{FB} \) and \( V^* = V_G - V_{FB} - V_D \).

In the complementary inverter circuit of Figure 5.1(b), the integration limits of Equation (5.2.1) for the driver TFT become

\[
V_{od} = V_{IN} - V_{FB}
\]

\[
V^*_\beta = V_{IN} - V_{FB} - V_{OUT}
\]

For the load TFT, they become

\[
V_{ol} = V_{IN} - V_{DD} - V_{FB}
\]

\[
V^*_\beta = V_{IN} - V_{FB} - V_{OUT}
\]

With these limits of integration and by using the semi-analytical expressions
Figure 5.1  (a) The cross-sectional view and (b) an equivalent circuit of the CMOS-like ambipolar a-Si:H TFT inverter circuit.
developed for the $G_S(V)$ of the driver and load TFTs, the integration was performed yielding the loadlines for the CMOS-like TFT inverter circuit as was shown in Figure 5.2 with various values of input voltage ($V_{FB} = -6$ volts)$^{3,4}$. In Chapter 4 accurate analytical expressions were derived for the sheet conductance of an n-channel device on the basis of two different energy band models, one for the a-Si bulk and one for the a-Si-SiO$_2$ interface states$^5$. To calculate the drain current of the n-channel a-Si:H TFT in a closed form, the accurate expressions for the sheet conductance are simplified as shown by the solid line for $V > V_{Tn}$ and by the dashed line for $0 < V \leq V_{Tn}$ in Figure 5.3. The expressions for the sheet conductance in the p-channel regime are also simplified as shown by the solid line for $V \leq V_{Tp}$ and by the dashed line for $V_{Tp} < V \leq 0$ in Figure 5.4. The simplified expressions for the sheet conductance, $G_S$, in the various regions of $V$ are given as follows;

$$G_S = A_n [\beta_n (V - V_{Tn})]^{(\eta_n-1)}$$  \hspace{1cm} (5.2)

when $V_G - V_{FB} > V_{Tn}$,

$$G_S = P_n e^{a_n V}$$  \hspace{1cm} (5.3)

when $0 < V_G - V_{FB} \leq V_{Tn}$,

$$G_S = P_p e^{-a_p V}$$  \hspace{1cm} (5.4)

when $V_{Tp} < V_G - V_{FB} \leq 0$, and

$$G_S = A_p [\beta_p (V_{Tp} - V)]^{(\eta_p-1)}$$  \hspace{1cm} (5.5)

when $V_G - V_{FB} \leq V_{Tp}$. The subscripts, n and p, denote the n-channel and the p-channel regimes, respectively. The numerical values of the parameters used in Equations (5.2) to (5.5) can be obtained by curve-fitting of $G_S$ to the experimental data$^5,6$, and are shown in Table 5.1. The subscripts, d and l, used later will denote the driver and the load TFTs, respectively.
Figure 5.2 The loadlines for the CMOS-like ambipolar a-Si:H TFT inverter circuit. The "•"s indicate the operating points of the inverter. $V_{IN} = V_{DD}$, $V_{on} = V_{IN} - V_{DD}$ ($V_{DD} = 30$ volts), and $V_{IN}$ is in 3 volt steps.
Figure 5.3  The sheet conductance of the n-channel regime: experimental (circles) and modeled (solid line for \( V > V_{Tn} \) and dashed line for \( 0 < V \leq V_{Tn} \)) data.
Figure 5.4 The sheet conductance of the p-channel regime: experimental (circles) and modeled (solid line for $V \leq V_{T_p}$ and dashed line for $V_{T_p} < V \leq 0$) data.
Table 5.1  The numerical values of the parameters used in Equations (5.2) to (5.5).

<table>
<thead>
<tr>
<th></th>
<th>( \beta ) (volts(^{-1}))</th>
<th>( V_T ) (volts)</th>
<th>( a ) (volts(^{-1}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-channel</td>
<td>12.3</td>
<td>17.4</td>
<td>0.8273</td>
</tr>
<tr>
<td>p-channel</td>
<td>9.3</td>
<td>-7.3</td>
<td>0.8642</td>
</tr>
</tbody>
</table>
5.3 Static Characteristics of the CMOS-like a-Si:H TFT Inverter Circuit

The driver and load a-Si:H TFTs are fabricated identically and operate together to give the desired CMOS-like inverter characteristics. The solid line in Figure 5.5 shows the experimentally measured voltage transfer curve for the CMOS-like inverter circuit and its static logic operating points are marked by "\( \diamond \)"s. The measured small-signal gain near the logic threshold is 40, which is larger than that of any other previously reported a-Si:H TFT inverter circuits\(^3\). The measured noise margin of the "zero" is 6.5 volts and that of the "one" is about 18 volts. Note that because of the ambipolar effect, the drain current flowing at the high-input logic level has increased \( V_{\text{OUT}} \) by a small amount.

In order to calculate the transfer curve of the CMOS-like TFT inverter circuit, one must develop expressions for the drain currents, \( I_d \) and \( I_l \), flowing through the driver and the load TFTs, respectively. The expressions for the drain currents can be obtained by substituting the proper expressions of \( G_s \) in various regions of \( V \) into Equation (5.1). When \( V_{IN} \leq V_{IL} \) in Figure 5.5, the driver TFT is in the p-channel dominant ambipolar regime and the load TFT is in the normal p-channel regime as shown by the operating points for low input voltages in Figure 5.2. Figure 5.6 shows various regions of operation of an ambipolar a-Si:H TFT output characteristics\(^7\). One can find that \( V_{od} < V_{Ta} \), \( V_\beta < V_{Tp} \), and \( V_{\alpha p} < V_\beta \). Therefore, Equation (5.5) is substituted into Equation (5.1) to give the expressions for \( I_d \) and \( I_l \).

For the load TFT, the expression for \( I_l \) is given by

\[
I_l = -F_{pl} \left[ (V_{Tpl} - V_{IN} + V_{FB} + V_{DD})^{\eta_d} - (V_{Tpl} - V_{IN} + V_{FB} + V_{OUT})^{\eta_d} \right] \tag{5.6}
\]

where \( F_{pl} \) is defined as

\[
F_{pl} = \left( \frac{W}{L} \right) \frac{A_{pl} \rho_{pl}^{(\eta_d-1)}}{\eta_d}.
\]

The drain current for a separate load TFT, calculated by using Equation (5.6), is shown by the dashed lines in Figure 5.7 for \( V_G = -30, -25, \) and \(-20 \) volts with close agreement to the experimental data.
Figure 5.5 Calculated (dashed line), graphically obtained (dotted line), and experimental (circles) transfer characteristics of the CMOS-like ambipolar a-Si:H TFT inverter circuit. The "\*'s indicate the stable operating points of the inverter.
Figure 5.6 Various regions of operation of an ideal ambipolar a-Si:H TFT output characteristics.
Figure 5.7 Experimental (symbols), analytical (solid lines), and simplified analytical (dashed and dotted lines) drain output characteristics of the load a-Si:H TFT. The dashed (dotted) lines are used to give the operating points of the CMOS-like TFT inverter circuit when $V_{IN} \leq V_{i1}$ or $V_{IN} \geq V_{i2}$ ($V_{i3} < V_{IN} < V_{i2}$) in Figure 5.5.
For the driver TFT, \( V_{nd} \) has a value between \( V_{Tnd} \) and \( V_{Tpd} \) and hence \( V_{Tpd} \) can be used for \( V_{nd} \). Then, the expression for \( I_d \) is obtained as

\[
I_d = F_{pd} \left[ V_{Tpd} - V_{IN} + V_{FB} + V_{OUT} \right]^{\eta_{pi}} \tag{5.7}
\]

where \( F_{pd} \) is defined as

\[
F_{pd} = \left( \frac{W}{L} \right) \frac{A_{pd}^{\beta_{pd}}(\eta_{pd} - 1)}{\eta_{pd}}.
\]

The drain current for a separate driver TFT, calculated by using Equation (5.7), is shown by the dashed lines in Figure 5.8 for \( V_G = 0, 3, 6, \) and 9 volts.

The calculated drain current agree well with the experimental data in the p-channel regime. For low input voltages, only the p-channel current is used to determine the operating points as shown in Figure 5.2. Therefore, only the p-channel current is required to be calculated precisely to give correct output voltages of the CMOS-like TFT inverter circuit for \( V_{IN} \leq V_{i1} \).

One uses the relation

\[
I_d = -I_l \tag{5.8}
\]

to solve for \( V_{OUT} \) as a function of \( V_{IN} \). In order to have an analytical solution for \( V_{OUT} \), Equations (5.6) and (5.7) are simplified as follows. If we define \( \Delta V_{OUT} \) by

\[
\Delta V_{OUT} = V_{DD} - V_{OUT} \tag{5.9}
\]

then Equation (5.6) becomes

\[
I_l = -F_{pl} \left[ V_{ipl}^{\eta_{ipl}} - V_{ipl}^{\eta_{ipl}} \left( 1 - \frac{\Delta V_{OUT}}{V_{ipl}} \right)^{\eta_{ipl}} \right] \tag{5.10}
\]
Figure 5.8  Experimental (symbols), analytical (solid lines), and simplified analytical (dashed and dotted lines) drain output characteristics of the driver a-Si:H TFT. The dashed (dotted) lines are used to give the operating points of the CMOS-like TFT inverter circuit when $V_{IN} \leq V_{i1}$ or $V_{IN} \geq V_{i2}$ ($V_{i1} < V_{IN} < V_{i2}$) in Figure 5.5.
where $V_{ipl}$ is defined as

$$V_{ipl} = V_{Tpl} - V_{IN} + V_{FB} + V_{DD}.$$ 

Since $V_{OUT}$ is now close to $V_{DD}$ as shown in Figure 5.5, $\Delta V_{OUT}$ is much smaller than $V_{ipl}$ and Equation (5.10) is approximated as

$$I_1 = -F_{pl} \left[ V_{ipl}^{\eta_{pl}} - V_{ipl}^{\eta_{pl}} \left( 1 - \eta_{pl} \frac{\Delta V_{OUT}}{V_{ipl}} \right) \right]$$

$$= -F_{pl} \eta_{pl} V_{ipl}^{(\eta_{pl}-1)} \Delta V_{OUT}. \quad (5.11)$$

Likewise, Equation (5.7) is approximated as

$$I_d = F_{pd} V_{ipd}^{\eta_{pd}} \left( 1 - \eta_{pd} \frac{\Delta V_{OUT}}{V_{ipd}} \right) \quad (5.12)$$

where $V_{ipd}$ is defined as

$$V_{ipd} = V_{Tpd} - V_{IN} + V_{FB} + V_{DD}.$$ 

Then, from Equations (5.8), (5.9), (5.11), and (5.12), one can obtain the expression for $V_{OUT}$ as

$$V_{OUT} = V_{DD} - \frac{F_{pd} V_{ipd}^{\eta_{pd}}}{F_{pl} \eta_{pl} V_{ipl}^{(\eta_{pl}-1)} + F_{pd} \eta_{pd} V_{ipd}^{(\eta_{pd}-1)}}. \quad (5.13)$$

The result is shown by the dashed line in Figure 5.5 with very close agreement to the experimental transfer curve for $V_{IN} \leq V_{i1}$.

When $V_{IN} \geq V_{i2}$ in Figure 5.5, the load TFT operates in the n-channel dominant ambipolar regime and the driver TFT operates in the normal n-channel regime as shown by the operating points for high input voltages in
Figure 5.2. One finds that $V_{ad} > V_{Ta}$, $V_\beta > V_{Ta}$, and $V_{Tp} < V_{\alpha} < V_\beta$. Hence, Equation (5.2) is substituted into Equation (5.1) to yield

$$I_d = F_{nd} \left[ (V_{IN} - V_{FB} - V_{Tnd})^\eta_{nd} - (V_{IN} - V_{FB} - V_{OUT} - V_{Tnd})^\eta_{nd} \right]$$

(5.14)

$$I_l = -F_{nl} \left[ V_{IN} - V_{FB} - V_{OUT} - V_{Tnl} \right]^\eta_{nl}$$

(5.15)

where $V_\beta$ is approximated by $V_{Tnl}$ since $V_\beta$ now has the value between $V_{Tnl}$ and $V_{Tpl}$. The calculated $I_d$ for a separate driver TFT is shown by the dashed lines in Figure 5.8 for high gate voltages of from 12 to 30 volts with close agreement to the experimental data. The calculated $I_l$ for a separate load TFT is shown by the dashed lines in Figure 5.7 for $V_G = -15, -10, -5$, and 0 volts. The calculated drain current agrees with the experimental data in the n-channel regime. For high input voltages, only the n-channel current is used to determine the operating points as shown in Figure 5.2. Hence, only the n-channel current is required to be calculated precisely to give correct output voltages of the inverter circuit for $V_{IN} \geq V_{i2}$.

Now that $V_{OUT}$ is close to 0 as shown in Figure 5.5, Equation (5.14) can be approximated as

$$I_d = F_{nd} \left[ V_{ind}^\eta_{nd} - V_{ind}^\eta_{nd} \left( 1 - \frac{V_{OUT}}{V_{ind}} \right)^\eta_{nd} \right]$$

$$\cong F_{nd} \left[ V_{ind}^\eta_{nd} - V_{ind}^\eta_{nd} \left( 1 - \eta_{nd} \frac{V_{OUT}}{V_{ind}} \right) \right]$$

$$= F_{nd}\eta_{nd}V_{ind}^{(\eta_{nd}-1)}V_{OUT}$$

(5.16)

where $V_{ind}$ is defined as

$$V_{ind} = V_{IN} - V_{FB} - V_{Tnd}.$$
Similarly, Equation (5.15) is approximated as

$$I_d = -F_{ni} V_{ini} \left( 1 - \eta_{ni} \frac{V_{OUT}}{V_{ini}} \right) \tag{5.17}$$

where $V_{ini}$ is defined as

$$V_{ini} = V_I - V_{FB} - V_{Th}.$$ 

Then, from Equations (5.8), (5.16), and (5.17), one obtains the expression for $V_{OUT}$ as

$$V_{OUT} = \frac{F_{ni} V_{ini}^{\eta_{ni}}}{F_{nd} \eta_{nd} V_{ind}^{(\eta_{nd}-1)} - F_{ni} \eta_{ni} V_{ini}^{(\eta_{ni}-1)}}. \tag{5.18}$$

The result is shown by the dashed line in Figure 5.5 with close agreement to the graphically obtained transfer curve.

When $V_{i1} < V_I < V_{i2}$ in Figure 5.5, one finds $0 < V_{od} < V_{Th}$ and $V_\beta > V_{Tpd}$ for the driver TFT. For high $V_{OUT}$, $V_\beta$ can have negative values and hence the driver TFT operates in the ambipolar regime resulting in higher operating current than the normal n-channel current. However, this effect of increasing the operating current causes a slightly degraded output voltage, and hence the driver TFT can be assumed to be in the normal n-channel regime. Thus, Equation (5.3) is substituted into Equation (5.1) to yield

$$I_d = F_{TD} \left[ 1 - e^{-a_{ni} V_{OUT}} \right] \tag{5.19}$$

where $F_{TD}$ is defined as
The drain current for a separate driver TFT, calculated by using Equation (5.19), is shown by the dotted lines in Figure 5.8 for \( V_G = 9 \) and 12 volts with very close agreement to the experimental data in the normal n-channel regime.

For the load TFT, one finds \( V_{\alpha l} > V_{\text{TPli}} \) and \( V_{\beta} < V_{\text{TPi}} \). Now \( V_{\beta} \) can have positive values for low \( V_{\text{OUT}} \) and the load TFT operates in the ambipolar regime giving higher operating current than the normal p-channel current. For the same reason as explained above for the driver TFT, the load TFT is assumed to operate in the normal p-channel regime. Hence, Equation (5.4) is substituted into Equation (5.1) yielding

\[
I_l = -F_{\text{Tl}} \left[ e^{a_{\text{pl}} V_{\text{IN}}} - e^{a_{\text{pl}} V_{\text{OUT}}} \right] \quad (5.20)
\]

where \( F_{\text{Tl}} \) is defined as

\[
F_{\text{Tl}} = \left( \frac{W}{L} \right) \frac{P_{\text{pl}}}{a_{\text{pl}}} e^{-a_{\text{pl}} (V_{\text{IN}} - V_{\text{rd}})}
\]

The drain current for a separate load TFT, calculated by using Equation (5.20), is shown by the dotted lines in Figure 5.7 for \( V_G = -20 \) and \(-15 \) volts with very close agreement to the experimental data in the normal p-channel regime.

In order to obtain an analytical solution for \( V_{\text{OUT}} \), either Equation (5.19) or (20) is simplified as follows. If \( V_{\text{IN}} \) is closer to \( V_{\text{il}} \) than to \( V_{i2} \), then \( V_{\text{OUT}} \) is larger than \( V_{\text{DD}}/2 \). Therefore, Equation (5.19) is approximated as

\[
I_d = F_{\text{Td}} \quad (5.21)
\]

since the second term in the square bracket is now much smaller than the unity \( (a_{\text{nd}} = 0.8273) \). From Equations (5.8), (5.20), and (5.21), one then
obtains the expression for $V_{OUT}$ as

$$V_{OUT} = \frac{1}{a_{pl}} \ln \left[ -C_T e^{(a_{nd}+a_{pl})V_{IN}} \left( 1 - \frac{1}{C_T} e^{-(a_{nd}+a_{pl})V_{IN} e^{a_{pl}V_{DD}}} \right) \right]$$  \hspace{1cm} (5.22)$$

where $C_T$ is defined as

$$C_T = \frac{\left( \frac{W}{L} \right) P_{nd}}{\left( \frac{W}{L} \right) P_{pl}} \exp(-a_{nd}V_{FB} - a_{pl}V_{FB}).$$

If $V_{IN}$ is closer to $V_{i2}$ than to $V_{i1}$, then $V_{OUT}$ is smaller than $V_{DD}/2$, and Equation (5.20) is approximated as

$$I_1 = -F_T e^{a_{pl}V_{DD}}$$  \hspace{1cm} (5.23)$$

Then, from Equations (5.8), (5.19), and (5.23), another expression for $V_{OUT}$ is obtained as

$$V_{OUT} = -\frac{1}{a_{nd}} \ln \left[ 1 - \frac{1}{C_T} e^{-(a_{nd}+a_{pl})V_{IN} e^{a_{pl}V_{DD}}} \right].$$  \hspace{1cm} (5.24)$$

The transition from Equation (5.22) to (24) is determined when the arguments of the logarithms of Equations (5.22) and (5.24) become zero, and

$V_{IN}(at transition) \equiv V_{it}$

$$= \frac{1}{(a_{nd} + a_{pl})} \left[ a_{pl}V_{DD} + (a_{nd} + a_{pl})V_{FB} - \ln F_T \right]$$  \hspace{1cm} (5.25)$$

where $F_T$ is defined as
Therefore, Equations (5.22) and (5.24) are used for the regions, \( V_{i1} < V_{IN} < V_{it} \) and \( V_{it} < V_{IN} < V_{i2} \), respectively, to calculate analytically the falling edge of the transfer curve as shown by the dashed line in Figure 5.5. The calculated transfer curve is almost identical to that obtained from the graphical method and shows very close agreement with the experimental data.

5.4 Improvement of the CMOS-like Ambipolar a-Si:H TFT Inverter

For the CMOS-like inverter circuit, 0.22 \( V_{DD} \) was measured for the noise margin of the "zero". This amount of the noise margin is quite acceptable in a-Si:H TFT logic circuits. However, the noise margin can be increased towards an ideal noise margin, \( V_{DD}/2 \), by shifting the flat-band voltages of the driver and load TFTs together. —6 volts was measured for the flat-band voltages of both the driver and load TFTs. If the flat-band voltages can be made less negative, then the p-channel operation is enhanced and the n-channel operation is diminished. The effect of shifting the flat-band voltages is well illustrated in Figure 5.9. The dashed lines are the loadlines of the CMOS-like inverter with original flat-band voltages and the solid lines are the loadlines for less negative (—2 volts) flat-band voltages. The improvement of the noise margin is shown in Figure 5.10. The noise margin of the "zero" is increased by about 40 per cent by shifting the flat-band voltages from —6 volts to —2 volts.

In Figure 5.9 one can notice that the p-channel operating current is increased and the n-channel operating current is decreased. Therefore, the switching speed of the inverter circuit is also enhanced. Because the switching speed of the CMOS-like inverter circuit is limited mainly by the p-channel current, making it more symmetrical in current drive reduces the total switching time.

The shifting of the flat-band voltage can be accomplished by decreasing the oxide thickness or by donor doping in the channel regions of both the
Figure 5.9  Comparison of the loadlines with original flat-band voltages, −6 volts, (dashed lines) and assumed less negative flat-band voltages, −2 volts (solid lines).
Figure 5.10 The transfer characteristics for $V_{FB} = -6$ volts (dashed line) and $V_{FB} = -2$ volts (solid line).
driver and load TFTs. But in the former way of shifting the flat-band voltage, care should be taken in decreasing the oxide thickness not to increase the oxide capacitance too much. Otherwise, the high oxide capacitance will increase the delay and the power delay product per gate.

In summary of this chapter, accurate analytical expressions for the sheet conductance of the ambipolar a-Si:H TFT were simplified and applied to the complementary, or CMOS-like TFT inverter circuit. The circuit is composed of only one type of ambipolar a-Si:H TFT which is used for both the driver and load transistor. This inverter has a very large small-signal gain as compared to other types of a-Si:H TFT inverter circuits. Thus, the CMOS-like ambipolar TFT inverter shows promise as a fundamental unit for TFT large area electronics logic circuits.

The simplified expressions of the sheet conductance of the ambipolar TFT were employed to calculate the drain currents of the load and the driver transistors, and then the expressions for the drain currents were used to yield the voltage transfer curve of the CMOS-like TFT inverter circuit. By making additional simplifications of the expressions for the drain currents of the load and the driver transistors, analytical expressions were obtained for the transfer curve in various regions of input voltage. The calculated transfer curve is almost identical to that obtained by the graphical method and shows very close agreement with the experimental transfer curve. The resultant equations can be easily employed in many existing computer programs for predicting circuit behavior and for designing the devices to give a particular performance parameter. It was also shown that the noise margin of the "zero" could be increased and the switching speed could be enhanced by making the flat-band voltages of both the driver and load TFTs less negative.

5.5 References


6.1 Introduction

The switching speed of the a-Si:H TFT is one of the major concerns in its applications. In order to understand its fundamental device limitations and to quantify reasons for its speed, the transient response of the a-Si:H TFT should be characterized and modeled. In this chapter the mechanisms involved in the transient response are identified and accurately modeled so that the switching speed of a-Si:H TFT circuits can be predicted and the optimized device can be developed.

6.2 Charge Trapping and Detrapping of a-Si:H TFT

The electrical characteristics of a-Si:H TFTs are time dependent unlike conventional devices. The source-drain current decreases with time at constant gate voltage because of two effects: (1) trapping of electrons in the localized states of a-Si, and (2) trapping of electrons in the gate dielectric at the interface. When the gate is turned on in an TFT, mobile electrons in the extended states accumulate under the gate. Some of these electrons are trapped into the localized states in the mobility gap of a-Si. Thus, these trapped electrons, which initially (at \( t = 0 \)) contributed to the channel mobility, are removed from the conduction process in the extended states. Electrons are also trapped at the dielectric semiconductor interface. This externally trapped charge partially shields the electric field of the gate and lowers the number of mobile electrons in the extended states. In addition, the trapped electrons in the localized states of a-Si set up a negative space charge in a-Si which decreases the mobility via Coulomb scattering.

The switching speed of practical a-Si:H TFT circuits is limited by the time required for the on-current to charge circuit capacitances. Therefore, with the large transient current, the switching speed of the a-Si:H TFT
circuits will be higher than expected from the DC current.

Due to the electron trapping when the TFT is turned on, the leakage current when it is turned off is much lower than it would be if the TFT had not been on first. Thus, the leakage current in a dynamic mode is much less than under DC conditions and the effective ON/OFF current ratio is increased. The leakage current increases with time due to detrapping of electrons which are trapped when the TFT is turned on.

The trapping and detrapping mechanisms of electrons continue until a steady state is reached. The trapping mechanism due to the localized states of a-Si appears to be relatively fast and that due to the gate dielectric appears to be slow\(^1\).

6.3 Measurements of the Transient Response

Measurements of the Transient response of the a-Si:H TFT were performed with the measurement setup shown in Figure 6.1. These measurements consisted of measuring the voltage drop across the resistor upon application of a gate voltage pulse. And the source current of the TFT was obtained by dividing the voltage drop with the resistance value. Figure 6.2(a) shows the applied gate voltage pulse varying from 0 to 30 volts, and part (b) shows a typical voltage drop for an unpackaged device with \(V_D = 30\) V. The structure of the a-Si:H TFT investigated in this research has a large gate-source overlap, and so the measured voltage drop shown in Figure 6.2(b) includes the voltage variation due to the gate-source stray capacitance.

In order to find the voltage variation due to the stray capacitance, another measurement for the voltage drop was done with \(V_D = 0\) V, and the result is shown in Figure 6.3. The voltage variation due to only the device transient response can be obtained by subtracting the voltage variation due to the stray capacitance shown in Figure 6.3 from the total voltage variation shown in Figure 6.2(b).

The resulted transient response of the source current is shown in Figure 6.4. As mentioned in section 6.2, the transient response shows that the source current decays fast initially, and then decreases slowly to a DC value.
Figure 6.1. Block diagram for the dynamic response measurements.
Figure 6.2. Transient response of a switching a-Si:H TFT: (a) applied gate-source voltage pulse (10 V/div; 2 ms/div) and (b) the voltage drop across the source resistor (50 mV/div; 2 ms/div) with $V_D = 30$ V.
Figure 6.3. The voltage drop across the source resistor (50 mV/div; 2 ms/div) with $V_D = 0$ V.
Figure 6.4. Transient response of the source current with $V_D = 30$ V.
6.4 Shift of the Flat-Band Voltage

The transient response of an a-Si:H TFT is expected to be originated mainly from charge trapping and detrapping in the trap states of the a-Si and gate dielectric at the interface. Therefore, the time dependence of charge trapping and detrapping need to be developed. The basic time dependence of trapping mechanism, used by Freeman and Luo\(^2\), is shown in Equation (6.1).

\[
\Delta N_T(t) = N_T[1-e^{-t/\tau}]
\]  

(6.1)

where \(\Delta N_T\) is the change in trap density with time, \(t\), \(N_T\) is the trap density in steady state, and \(\tau\) is the time constant for filling the traps.

In general, the charge movement in the gate dielectric and/or near the interface manifests as flat-band voltage shift in measurement of the source-drain current. If there are many trapping mechanisms with different time constants and all of the trapped charges are assumed to be located at the interface, then the flat-band voltage shift, \(\Delta V_{FB}\), can be described by Equation (6.2).

\[
\Delta V_{FB}(t) = \sum_{i=1}^{n} V_{FBi}[1-e^{-t/\tau_i}]
\]  

(6.2)

where \(V_{FBi}\) is the flat-band voltage shift due to the \(i\)-th trapping mechanism in steady state and \(n\) is the number of trapping mechanisms. Thus, the shift of the flat-band voltages due to the time dependent charge trapping and detrapping was incorporated into the static model already developed in Chapter 3. The new model then was used for predicting the transient source-drain current, and the result was compared with the measured transient response as shown in Figure 6.5. Very close agreement with the experimental data was obtained using two charging mechanisms where \(V_{FB1} = 1.2 \text{ V}, \ V_{FB2} = 0.8 \text{ V}, \ \tau_1 = 1.5 \text{ ms}, \) and \(\tau_2 = 8 \text{ ms}.\) Since the trap density is related to the flat-band voltage by

\[
N_T = \frac{C_{ox}}{q} \Delta V_{FB}
\]  

(6.3)
Figure 6.5. Modeled (solid line) and measured (circles) transient responses of the source current with $V_D = 30$ V.
where $C_{ox}$ is the oxide capacitance per unit area and $q$ is the electronic charge, one can find $N_{T1} = 1.1 \times 10^{11} (\#/\text{cm}^2)$ and $N_{T2} = 7.5 \times 10^{10} (\#/\text{cm}^2)$. One might interpret $N_{T1}$ and $N_{T2}$ as the trap densities in the a-Si and the oxide, respectively, because the first charging mechanism is faster than the second one.

Once the associated constants are decided, the dynamic model can be used to predict the switching speed of the a-Si:H TFT circuits, especially the complementary ambipolar a-Si:H TFT inverter circuit, and to optimize the device for other applications.

6.5 References


CHAPTER 7
DYNAMIC CHARACTERISTICS OF THE CMOS-LIKE
AMBIPOLAR a-Si:H INVERTER CIRCUIT

7.1 Introduction

In digital circuits a logic gate is designed from a static point of view to
provide the proper output levels to switch the next logic gate. In Chapter 5
the static characteristics were modeled for the CMOS-like ambipolar a-Si:H
TFT inverter circuit, and the static model can be used to design the inverter
which drives the next gate with the proper output levels.

In addition, the output levels of the logic gate have to change within a
specified period of time, and thus dynamic or transient analysis is crucial in
designing the logic gates. The switching speed of the conventional CMOS
inverter circuit is limited by the time taken to charge and discharge the load
capacitance. In this chapter the dynamic model of the CMOS-like
ambipolar a-Si:H TFT inverter circuit is developed so that the switching
speed of the inverter can be predicted and the optimized inverter can be
designed.

7.2 Dynamic Model Using the Static Model of TFTs

In this section the dynamic characteristics of the CMOS-like ambipolar
a-Si:H TFT inverter are modeled on the basis of the static model developed
in Chapter 5. An equivalent circuit for transient analysis is shown in Figure
7.1. The output load is represented by a load capacitor, $C_L$. The load
capacitance is equal to the sum of input capacitances of the load and driver
TFTs if the output is connected to another inverter.

The input node responds instantaneously to the square wave supplied
by a pulse generator, but the output response is limited by the inverter's
ability to charge and discharge the output capacitance. At the output node
in Figure 7.1, one can obtain following relation,
Figure 7.1  An equivalent circuit for transient analysis.
where \( I_d \) and \( I_l \) are the currents flowing through the driver and load TFTs, respectively, and \( V_o \) is the output voltage. If Equation (7.1) is rearranged and integrated, then one obtains

\[
(I_d - I_l) + C_L \frac{dV_o}{dt} = 0 \tag{7.1}
\]

where \( V_{oi} \) is the output voltage at initial time, \( t_i \).

In the first transition the input changes from \( V_{DD} \) to 0. Immediately after the first transition, the driver TFT almost shuts off in the n-channel regime, and the load TFT changes its operating point from the n-channel dominant ambipolar regime to the normal p-channel regime in saturation as shown in Figure 7.2. Thus, \( I_d \) is negligibly small, and \( I_l \) is calculated by Equation (5.6) (with \( V_{IN} = 0 \) and \( V_{OUT} = -V_{T_{pl}} - V_{FB} \)) as

\[
I_l = I_{l,SAT} = F_{pl}(V_{T_{pl}} + V_{FB} + V_{DD})^{\nu_{pl}}. \tag{7.3}
\]

The load capacitance is then charged by \( I_l \), and the output voltage rises toward \( V_{o2} \). \( V_{o2} \) can be calculated by Equation (5.13) with \( V_{IN} = 0 \). When the output voltage has increased so that the drain end of the load TFT reaches to the flat-band point, the load TFT leaves the saturation region and the \( I_l \) begins to decrease. As the output voltage increases, \( I_d \) increases first in the n-channel regime and then in the p-channel dominant ambipolar regime as shown in Figure 7.2.

Once the driver TFT is in the p-channel dominant ambipolar regime, \( I_d \) increases fast and its magnitude is no longer negligible as compared to \( I_l \). Now, new expressions for \( I_l \) and \( I_d \) are required to be used in Equation (7.2), and they are obtained from Equations (5.6) and (5.7) (with \( V_{IN} = 0 \)) as
Figure 7.2 Movement of the operating points for the first transition where $V_{IN}$ changes from $V_{DD}$ to 0.
\[ I_d = F_{pd} \left( V_{Tpd} + V_{FB} + V_{OUT} \right)^{\eta_{pd}}. \]

In the second transition the input changes from 0 to \( V_{DD} \). Immediately after the second transition, the load TFT almost shuts off in the n-channel dominant ambipolar regime, and the driver TFT changes its operating point from the p-channel dominant ambipolar regime to the normal n-channel regime in saturation as shown in Figure 7.3. Thus, \( I_l \) is very small, and \( I_d \) can be calculated by Equation (5.14) (with \( V_{IN} = V_{DD} \) and \( V_{OUT} = V_{DD} - V_{Tnd} - V_{FB} \)) as

\[ I_d = I_{d, \text{SAT}} = F_{nd} (V_{DD} - V_{FB} - V_{Tnd})^{\eta_{nd}}. \]

The load capacitance is then discharged by \( I_d \), and the output voltage falls from \( V_{o2} \) toward \( V_{o1} \). \( V_{o1} \) can be calculated by Equation (5.18) with \( V_{IN} = V_{DD} \).

When the output voltage has decreased so that the drain end of the driver TFT reaches to the flat-band point, the driver TFT leaves the saturation region and the \( I_d \) begins to decrease. As the output voltage decreases, \( I_l \) increases fast as shown in Figure 7.3. Now, new expressions for \( I_d \) and \( I_l \) are needed to be used in Equation (7.2), and they are obtained from Equations (5.14) and (5.15) (with \( V_{IN} = V_{DD} \)) as

\[ I_d = F_{nd} \left( (V_{DD} - V_{FB} - V_{Tnd})^{\eta_{nd}} - (V_{DD} - V_{FB} - V_{OUT} - V_{Tnd})^{\eta_{nd}} \right). \]

\[ I_l = F_{nl} \left( V_{DD} - V_{FB} - V_{OUT} - V_{Tnl} \right)^{\eta_{nl}}. \]

Substituting different expressions for \( I_d \) and \( I_l \) (Equation (7.3) to (7.8)) into Equation (7.2) according to the operating regimes of the driver and load
Figure 7.3 Movement of the operating points for the second transition where $V_{IN}$ changes from 0 to $V_{DD}$. 
TFTs, one can calculate the time, t, numerically. The switching characteristics were calculated numerically by using Simpson's rule, and are shown by the solid line in Figure 7.4 for the CMOS-like ambipolar a-Si:H TFT inverter. It is very obvious that the switching speed of the CMOS-like inverter is limited by charging process of the load capacitance. Charging of the load capacitance is quite slower than discharging of it, due to low current drive capability of the load TFT.

In order to speed up the charging process, the current drive capability has to be enhanced, and this can be done by several ways. First, the flat-band voltages of both the load and driver TFTs were assumed to be less negative as was done in Chapter 5, where the noise margin was shown to be improved by using less negative flat-band voltages. The results are shown in Figure 7.5, where one can observe that the charging process becomes faster without slowing discharging process appreciably with less negative flat-band voltages.

Second, the width to length ratio of the load TFT was assumed to be ten times longer, and the enhanced charging process is shown by the dotted line in Figure 7.6.

Third, the hole mobility was assumed to be two times larger, and the enhanced charging process is again shown by the dashed line in Figure 7.6.

7.3 Dynamic Model Including the Transient Response of TFTs

In Chapter 6 it was shown that the electrical characteristics of a-Si:H TFTs are time dependent. The source-drain current decreases with time at constant gate voltage. In Section 7.2 the dynamic analysis of the CMOS-like inverter was done on the basis of the static model of a-Si:H TFTs. The static model was based on measurement of the current which was done 10 seconds after the gate voltage was applied. Thus, the actual source-drain current is larger than that used for the static analysis of a-Si:H TFTs within 10 seconds from when the gate voltage is applied. The CMOS-like inverter completes its transient response in much shorter time than 10 seconds. Therefore, the transient currents of the load and driver TFTs are larger than those used for the static analysis, and one can expect that actual charging and discharging processes are faster than those predicted in Section 7.2.
Figure 7.4  Calculated switching characteristics of the CMOS-like inverter.
Figure 7.5 Comparison of switching characteristics of the CMOS-like inverter for different flat-band voltages.
Figure 7.6 Comparison of switching characteristics of the CMOS-like inverter for different width to length ratios and hole mobilities.
After the first transition (with $V_{IN}$ changing from $V_{DD}$ to 0), $I_d$ can be calculated by Equation (7.3) as long as the load TFT is in saturation region in the normal p-channel regime. In Chapter 6 the transient response of an a-Si:H TFT was explained by the shift of the flat-band voltages. If two time constants are used as in Chapter 5, then the flat-band voltage can be expressed as

$$V_{FB} = V_{FBp} + V_{FB1}[1 - e^{-t/\tau_{p1}}] + V_{FB2}[1 - e^{-t/\tau_{p2}}].$$

(7.9)

From Equations (7.3) and (7.9), one obtains

$$I_{SAT,1} = F_{pl} V_{sp}^\eta (1 - \frac{V_{tp}}{V_{sp}})^\eta \cdot (7.10)$$

where

$$V_{sp} = V_{DD} + V_{Tpl} + V_{FBp} + V_{FB1} + V_{FB2}$$

$$v_{tp} = V_{FB1} e^{-t/\tau_{p1}} + V_{FB2} e^{-t/\tau_{p2}}.$$

Since $V_{sp}$ is much larger than $v_{tp}$, Equation (7.10) can be approximated as

$$I_{SAT,1} \approx F_{pl} V_{sp}^\eta (1 - \eta_{pl} \frac{V_{tp}}{V_{sp}})$$

(7.11)

Since the driver TFT nearly shuts off now, $I_d$ is very small (even smaller than that predicted in Section 7.2 due to less negative flat-band voltage), and Equation (7.1) is approximated as

$$I_{SAT} \approx C_L \frac{dV_o}{dt}.$$  

(7.12)

Then, from Equations (7.11) and (7.12), one obtains
Rearranging and integrating Equation (7.13) yields

\[
\int_{V_{o1}}^{V_o} dV_o = \frac{F_{pl}}{C_L} V_{sp}^{\eta_{pl}} \int_0^t (1 - \eta_{pl} \frac{V_{lp}}{V_{sp}}) \, dt
\]

\[
V_o = V_{o1} + C_{p1} t + C_{p1} \frac{\eta_{pl}}{V_{sp}} \left[ V_{FB1} \tau_{p1} (e^{-t/\tau_{p1}} - 1) + V_{FB2} \tau_{p2} (e^{-t/\tau_{p2}} - 1) \right]
\]

where

\[
C_{p1} = \frac{F_{pl}}{C_L} V_{sp}^{\eta_{pl}}.
\]

The load TFT leaves the saturation region and \( I_l \) begins to decrease when the output voltage has increased so that the drain end of the load TFT reaches to the flat-band point. While the load TFT moves to the pinch-off point, \( I_l \) and \( I_d \) approaches their static values. If \( I_l \) and \( I_d \) are assumed to reach their static values at the pinch-off point, then the technique used in Section 7.2 can be used after the pinch-off point.

After the second transition (with \( V_{IN} \) changing from 0 to \( V_{DD} \)), \( I_d \) can be calculated by Equation (7.6) as far as the driver TFT is in saturation region in the normal n-channel regime. The flat-band voltage now can be expressed as

\[
V_{FB} = V_{FBa} - V_{FB1} [1 - e^{-t/\tau_m}] - V_{FB2} [1 - e^{-t/\tau_m}].
\]

From Equations (7.6) and (7.15), one obtains
\[ I_{d,SAT} = F_{nd} V_{sn}^{\eta_{nd}}(1 - \frac{V_{tn}}{V_{sn}})^{\eta_{nd}} \]  \,(7.16)\]

where

\[ V_{sn} = V_{DD} - V_{Tnd} - V_{FB1} + V_{FB1} + V_{FB2} \]

\[ V_{tn} = V_{FB1} e^{-t/r_{n1}} + V_{FB2} e^{-t/r_{n2}}. \]

Since \( V_{sn} \) is much larger than \( V_{tn} \), Equation (7.16) is approximated as

\[ I_{d,SAT} \simeq F_{nd} V_{sn}^{\eta_{nd}}(1 - \eta_{nd} \frac{V_{tn}}{V_{sn}}) \]  \,(7.17)\]

Since \( I_d \) is very small (even smaller than that predicted in Section 7.2 due to more negative flat-band voltage), Equation (7.1) is approximated as

\[ I_{d,SAT} \simeq -C_L \frac{dV_o}{dt}. \]  \,(7.18)\]

Then, from Equations (7.17) and (7.18), one obtains

\[ \frac{dV_o}{dt} = -\frac{F_{nd}}{C_L} V_{sn}^{\eta_{nd}}(1 - \eta_{nd} \frac{V_{tn}}{V_{sn}}) \]  \,(7.19)\]

Rearranging and integrating Equation (7.19) yields

\[ \frac{V}{V_o} = \frac{F_{nd}}{C_L} \frac{V_{sn}^{\eta_{nd}}}{t} (1 - \eta_{nd} \frac{V_{tn}}{V_{sn}}) dt \]  \,(7.20a)\]

\[ V_o = V_{o2} - C_{n1} t - C_{n1} \frac{V_{sn}}{V_{sn}} [V_{FB1} r_{n1}(e^{-t/r_{n1}} - 1) + V_{FB2} r_{n2}(e^{-t/r_{n2}} - 1)] \]  \,(7.20b)\]
where

\[ C_{n1} = \frac{F_{nd}}{C_L} V_{sd}^{''}. \]

When the output voltage has decreased so that the drain end of the driver TFT reaches to the flat-band point, the driver TFT leaves the saturation region and moves into the linear region. \( I_d \) and \( I_l \) approaches their static values while the driver TFT moves to the pinch-off point. If \( I_d \) and \( I_l \) are assumed to reach their static values at the pinch-off point, then the technique employed in Section 7.2 can be used again after the pinch-off point.

Figure 7.7 shows the calculated switching characteristics for \( V_{FBp} = -4 \) V, \( V_{FBn} = -8 \) V, \( V_{FB1} = -1.2 \) V, \( V_{FB2} = -0.8 \) V, \( \tau_1 = 1.5 \) ms, and \( \tau_2 = 8 \) ms. It is clearly seen that the switching characteristics are improved when the transient responses of the load and driver TFTs are taken into account.

In summary of this chapter, the dynamic model of the CMOS-like ambipolar a-Si:H TFT inverter was developed on the basis of the static model. The switching speed of the CMOS-like inverter is limited by charging process of the load capacitance, due to low current drive capability of the load TFT. Some of optimizations of the device parameters were shown to speed up charging process. Finally, actual switching characteristics of the CMOS-like inverter were shown improved when the transient currents of the load and driver TFTs were taken into account.
Figure 7.7 Comparison of switching characteristics of the CMOS-like inverter with (dashed line) and without (solid line) transient response of the load and driver TFTs.
CHAPTER 8
CONCLUSIONS AND RECOMMENDATIONS
FOR FUTURE RESEARCH

8.1 Conclusions

This study has been performed on the static and dynamic characteristics of hydrogenated amorphous silicon thin film transistors. The ambipolar properties of the a-Si:H TFT have been characterized and modeled. As an application of the ambipolar TFTs, a CMOS-like inverter circuit was introduced, and its static and dynamic characteristics were also developed.

Based on two different energy band models, accurate analytical expressions were derived for the sheet conductance of an n-channel a-Si:H TFT. A simplified CFO model was used for the a-Si bulk states, and a simplified Davis-Mott model was used for the a-Si—SiO₂ interface states. The basic expressions for the sheet conductance were simplified and then used for the calculation of the drain current showing very close agreement with the experimental data.

By applying similar procedures to the p-channel mode of operation, the static output characteristics of an ambipolar PECVD a-Si:H could be modeled. The model also included a systematic method for incorporating the effects of the different n-channel and p-channel regime flat-band voltages in the interpolated sheet conductance resulting in very close agreement with the experimental output characteristics over many orders of magnitude of the drain current in both the forward and reverse modes of operation.

A new CMOS-like inverter circuit was made by using two identical ambipolar a-Si:H TFTs which were fabricated at the same time, therefore requiring no extra fabrication processes. This inverter circuit shows an ideal step-like transfer characteristics, a very high small-signal gain, and a reasonable noise margins, as compared to other types of a-Si:H TFT inverter circuits. Thus, the CMOS-like inverter shows promise as a fundamental unit for the logic circuits of TFT large-area electronics.
The simplified expressions of the sheet conductance of the ambipolar TFT were employed to calculate the current of the inverter, and then the expressions for the current were used to give the voltage transfer curve of the CMOS-like TFT inverter circuit. The calculated transfer curve is almost identical to that obtained by the graphical method and shows very close agreement with the experimental transfer curve. It was also shown that the inverter characteristics could be improved by making the flat-band voltages of both the driver and load TFTs less negative.

The electrical characteristics of a-Si:H TFTs are time dependent, and the source-drain current decreases with time at constant gate voltage because of trapping of electrons at the interface. Charge trapping at the interface causes the shift of the flat-band voltages. By incorporating the flat-band voltage shift into the static model of the TFT, the transient response (the current decrease) could be characterized and modeled. The dynamic model of the CMOS-like TFT inverter was developed by combining the static model of the inverter and the transient characteristics of the TFTs.

All the equations and models developed in this study can be used for designing and optimizing the a-Si:H TFTs and their circuits in dynamic as well as in static points of view. They are also easily employed in many existing CAD circuit analysis programs for predicting circuit behavior.

8.2 Recommendations for Future Research

To make the a-Si:H TFT and its circuits more commercially applicable, additional work needs to be done in the following areas.

Basic research is required about the carrier mobility at the interface of TFT. The interface mobility is a fundamental parameter in the electrical performance of TFT. However, it is not easy to measure the interface mobility with solid theoretical support. Field effect mobility has been measured by using the techniques for conventional MOSFETs. This technique may give accurate value of the mobility if TFT is strongly biased so that the channel charge is dominated by mobile charge instead of the trapped charge.

The interface mobility can also be obtained by measuring the transit time of the carriers across the channel because the transit time is inversely proportional to the mobility. Accurate measurement techniques need to be
developed to do this. Complete AC model for TFT and its spray capacitances are also in need.

Ambipolar TFT with a symmetrical conductance curve needs to be developed to improve the CMOS-like inverter characteristics. This may be accomplished by using different material from a-Si for the semiconductor of TFT. For example, a-GeSi:H have shown more symmetrical sheet conductance than a-Si:H. Different implants in the source/drain regions can also be tried to make the sheet conductance more symmetrical. In this approach more study needs to be done about the physical properties of the metal—a-Si:H interface.

Although the thermal oxide is the best insulator for a-Si:H TFTs, it is not practical in terms of applications such as switching elements and logic circuits in large-area LCD arrays. Work needs to be done to develop an insulator with lower surface states and fixed charge than currently used glow-discharge nitride and oxide insulators. For example, a new low-temperature method of thermal-oxidation for a-Si has been demonstrated by utilizing a nitric and sulphuric acid mixture under high pressure conditions. Langmuir-Blodgett film has also been used as an insulator of a-Si:H TFT.

Shift register circuits need to be designed and fabricated to test the dynamic characteristics of TFTs. To improve the circuit performance of TFTs, a short-channel TFT, such as vertical-type TFT, also need to be developed and characterized.