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Abstract—**Thermally activated subthreshold transport has been investigated in *undoped* triple-gate MOSFETs. The evolution of the barrier height and of the active cross-sectional area of the channel as a function of gate voltage has been determined. The results of our experiments and of the tight-binding simulations we have developed are both in good agreement with previous analytical calculations, confirming the validity of the thermionic approach to investigate transport in FETs. This method provides an important tool for the improvement of device characteristics.**

Index Terms—**FinFET, thermionic emission, tight binding (TB).**

I. INTRODUCTION

IN RECENT years, many MOSFET geometries have been introduced to overcome short-channel effects (SCEs) [1]. Among them, one of the most promising is the FinFET *geometry* [1]–[3]. In this structure, a much stronger gate–channel coupling can be obtained by the simultaneous action of the gate electrode on three faces of the channel [see Fig. 1(a) and (b)]. The mechanisms of subthreshold transport can be difficult to clarify due to the presence of screening [4]. As an example, the *undoped* channel version of these devices has a nontrivial and gate-voltage (V_g)-dependent current distribution. Therefore, the necessity of the development of tools that could be used to investigate current distribution has emerged. This knowledge is expected to allow an improvement of the device characteristics toward their scaling to the nanometer size regime. For device widths smaller than 5 nm, full volume inversion is expected to arise [1]. Wider devices are expected to be in the regime of *weak* volume inversion (where the bands in the channel closely follow the potential of V_g) for $V_g \ll V_{th}$ [1], [5]. Several groups have investigated the behavior of such weak-volume-inversion devices using both classical [6], [7] and quantum [8] computational models, but, to our knowledge, no experimental method that yields information on the location of the current-
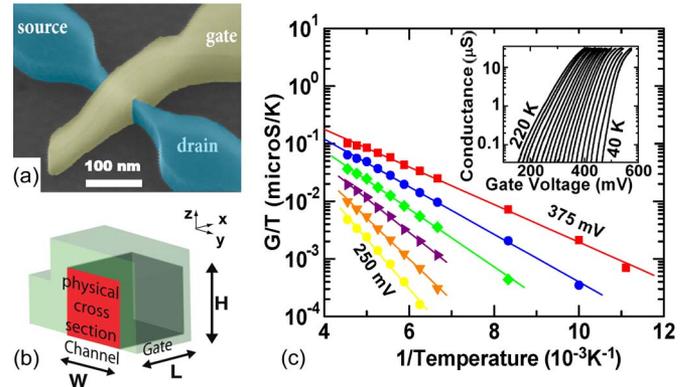
Fig. 1. (a) Scanning-electron-microscope image of a device. (b) Schematic view of our FinFETs. (Light yellow) The gate covers three faces of the (dark yellow) channel. L, H, and W represent the channel length, height, and width, respectively. In red, the physical cross-sectional area is shown. (c) Fits used to extrapolate E_b and S in one of our $W = 55$ nm devices. In the inset, differential conductance versus V_g data, for different temperatures, are shown.

carrying regions of the channel exists. Taur has studied this problem analytically for an *undoped* channel with double-gate geometry, using a 1-D Poisson equation [5].

The main conclusion emerging from this letter is that, when the gate voltage is increased, a crossover takes place between the behavior of the channel at $V_g \ll V_{th}$ and at $V_g \sim V_{th}$, caused by screening of induced carriers which subsequently increases the carrier density at the gate–channel interface. To our knowledge, this prediction has never been directly observed experimentally. In this letter, we use a 2-D model but the physical principle is fully analogous to the 1-D case of Taur.

II. EXPERIMENTAL RESULTS

Conductance versus temperature traces for a set of eight *undoped* FinFET devices with the same channel length $(L = 40$ nm) and channel height $(H = 65$ nm) but different channel widths $(W = 25, 55, 125,$ and 875 nm) are presented. The discussion is focused on one device for each width since the same behavior for each of the devices of the same width is found consistently. Our devices consist of a nanowire channel etched on a 65-nm Si intrinsic film with a wrap-around gate covering three faces of the channel [Fig. 1(a) and (b)] [3]. An HfSiO layer isolates a TiN layer from the intrinsic Si channel [3]. Differential conductance $(G = dI_{sd}/dV_{sd})$ data are taken at $V_{sd} = 0$ mV using a lock-in technique. Thermionic emission above a barrier can be represented by the following [4], [9]:

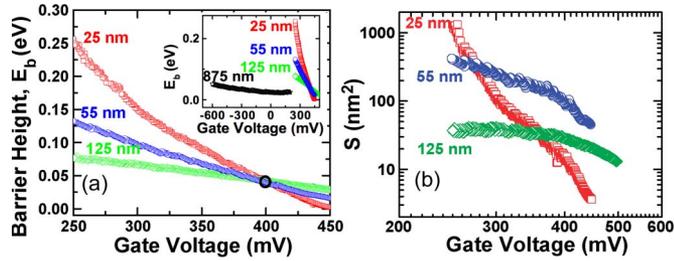$$G = SA^*T \frac{e}{k_B} \exp\left(-\frac{E_b}{k_B T}\right) \qquad (1)$$

Fig. 2. Data obtained using the model of (1). (a) E_b versus V_g for one device for each width from 25 to 125 nm. In the inset, calculated E_b versus V_g for all device widths are shown. (b) Results of the dependence of the active cross section S versus V_g obtained for all devices with $W \leq 125$ nm.

where $A^* = 2.1 \times 120$ A·cm^{-2}·K^{-2} is the effective Richardson constant for Si [4], [9]. Fig. 1(c) shows the G/T versus $1000/T$ data obtained from the rearrangement of the G versus V_g data taken at different temperatures [inset in Fig. 1(c)]. Using the data of Fig. 1(c), results for the source (drain)-channel barrier height E_b versus V_g dependence and for the active cross-sectional area of the channel S versus V_g dependence can be extrapolated using the thermionic fitting procedure. The important fact is that S is to be interpreted as a good estimation of the portion of the physical cross-sectional area through which the transport preferentially occurs [4]. Note that (1) has only two parameters, namely, S and E_b, and the accuracy obtained in the fits made using this equation [$R \sim 0.99$ for all fits of devices with widths ≤ 125 nm, as in Fig. 1(c)] demonstrates the validity of the use of this model to study subthreshold transport in our 40-nm-channel-length FinFETs. Fig. 2(a) examines the barrier height as a function V_g. We observe an expected decrease in E_b while increasing V_g. As can be seen in the inset of Fig. 2(a), this effect is less pronounced for wider devices. We attribute this to SCEs that influence the electronic characteristics even at low bias. This trend is also reflected by the data of Table I, where the coupling factors obtained from our thermionic fits $\alpha_1 = dE_b/dV_g$ [4] (thus, the electrostatic coupling between the gate and the bulk of the channel) show a decrease for increasing width. In Table I, we also show the coupling between the potential of the channel interface and V_g, i.e., α_2, extracted from Coulomb-blockade (CB) measurements (at 4.2 K) of confined states that are present at the channel/gate interface [4], [10]. We find α_2 to be constantly independent of W. In CB theory, α_2 is the ratio between the electrochemical potential of the confined states and the change in V_g. This ratio can be estimated from the so-called "stability diagram" [4]. This leads us to the conclusion that the coupling to the channel interface remains constant for increasing W, whereas the coupling to the center of the channel does not. In the 875-nm devices, SCEs are so strong [see inset Fig. 2(a)] that the thermionic theory loses accuracy; hence, we will not discuss the results of these devices any further. All the E_b versus V_g curves, as shown in Fig. 2(a), cross each other at around 0.4 V (outlined by the black circle), before complete inversion of the channel takes place at $V_{\text{th}} \sim 0.5$ V [3]. This suggests that, at $V_g = 0.4$ V, the work function of the TiN is equal to the affinity of the Si channel in our devices [3]. The same value has also been verified in other measurements using capacitance–voltage (C–V) techniques [11], independently from the W of the channel. This fact gives us confidence that we are indeed observing activated transport over the channel barrier formed by the metal/oxide/semiconductor interface,

TABLE I
SUMMARY OF THE CHARACTERISTIC GATE-CHANNEL CAPACITIVE COUPLING OF DEVICES REPORTED IN THIS LETTER, OBTAINED FROM THE RESULTS OF FIT AS IN FIG. 2(a) (α_1) AND FROM CB MEASUREMENTS AT 4.2 K (α_2)

Width (nm)	α_1	α_2
25	1	0.7
55	0.7	0.8
125	0.14	0.8
875	0.03	0.8

which, at $V_g = 0.4$ V, will not dependent on W. The crossing point in Fig. 2(a) is not located exactly at $E_b = 0$ meV but is at 50 meV. We attribute this feature to the presence, at the channel–gate boundary, of interface states (already found in CB measurements) that can store charge, repel electrons, and therefore, raise up the barrier by a small amount. In Si/SiO$_2$ systems that have been studied in the past, these states were estimated to give an energy shift quantifiable between 70 and 120 meV [10], in line with our data. Fig. 2(b) shows S as a function of V_g extrapolated using (1). We can compare these results to the analytical model [5] discussed before and to our self-consistent simulations performed, as described in [12]–[14]. At low V_g, devices with $W = 25$ nm show an active cross-sectional area of around 1000 nm^2 [see Fig. 2(b)]. This is almost equal to the physical cross-sectional area of the channel at these widths. At higher V_g, the active cross-sectional area decreases to a few square nanometers. We interpret these data as follows: At low V_g, transport in these devices is uniformly distributed everywhere in the physical cross section of the channel (*weak* volume inversion), but with the increase of V_g, an increase of carrier density in the region near the interface and, as a consequence, a reduction of S arise. This interpretation corresponds with the screening mechanism discussed in [5]. Subsequently, the action of the gate in the center of the channel is suppressed. Devices that have 55- and 125-nm widths behave in a fashion similar to the 25-nm ones, but show a less pronounced decreasing trend and counterintuitive small values for S, as we observe a progressive reduction of α_1 for increasing W. This is not a surprise as the barrier in these larger devices is lower and more carriers are allowed to migrate to the interface enhancing the screening effect. These results give, for the first time, an experimental insight into the mechanisms of conduction in *undoped* FinFETs.

III. COMPARISON WITH SIMULATION

We used state-of-the-art-simulations, done using an atomistic ten-band sp3d5s* tight-binding (TB) model, to perform electronic structure calculation, coupled self-consistently with a 2-D Poisson solver [12], and we obtained terminal characteristics using a ballistic top-of-the-barrier model [13]. Due to the extensively large cross section of our device that combines up to 44 192 atoms in the simulation domain, we had to integrate a new NEMO 3-D code into our top-of-the-barrier analysis [14]. With this expanded modeling capability, we have been able to compare our experimental results with the simulation results. We do not expect the effects of the variation of the potential in the source–drain direction to play a role in the device we simulated since V_{sd} is very small [13], [14]. Also, the gate length is long enough to suppress the tunneling current from source to drain [13], [14]. In fact, using a geometry identical to that of one
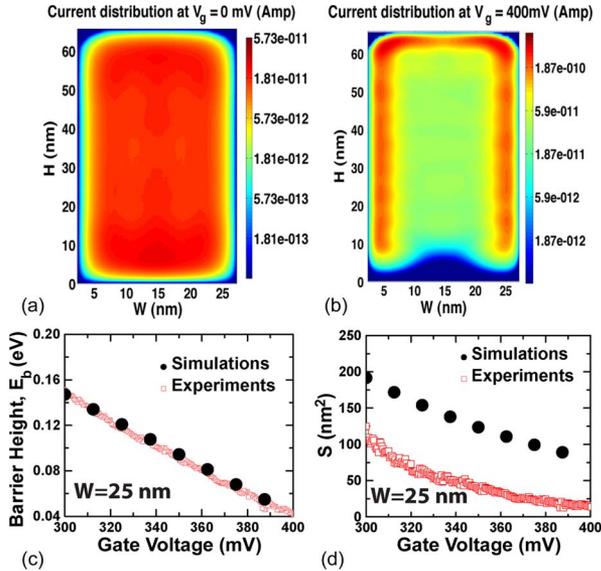
Fig. 3. Current distributions for (a) $V_g = 0$ mV and (b) $V_g = 400$ mV, obtained using TB simulations for a FinFET geometry and $W = 25$ nm. Comparison of the simulated (c) E_b and (d) S with the experimental data for the $W = 25$ nm *device*.

of our FinFETs, with $W = 25$ nm and $H = 65$ nm and under biases similar to the ones of our experiments, the simulated current distribution shows a crossover from a situation of *weak volume inversion* at $V_g = 0$ mV [Fig. 3(a)] to a situation of transport confined prevalently at the interface at $V_g = 400$ mV [Fig. 3(b)]. Therefore, also from the simulated current distribution, which gives a good indication of where mobile charges prevalently flow, a reduction of S with increasing V_g can be extracted. However, this reduction is not as sharp as in the experimental data, as these simulations have been performed at $T = 300$ K and also due to the absence of interface states (expected to enhance the effect of screening in real devices) [4], [10]. As a final benchmark to our experimental method, we have used the results of the TB simulations to calculate the current and the conductance at different temperatures and to extract, using again (1), the simulated E_b and S for a $W = 25$ nm device. In fact, in Fig. 3(c) and (d), we compare the simulated values with experiments and found that we can predict experimental results with good accuracy, although the simulations overestimate the values of S [probably for the same reasons discussed for Fig. 3(b)]. In any case, by comparing our experimental results with the results of the simulations, we have a demonstration of the reliability of the method we have developed. This opens the way of its systematic use to obtain information about the magnitude and the position of carriers in FET devices in general and not only in our FinFET structures. In our investigations, we have neglected possible modifications of A^* due to the constrained geometry [15] of our devices, as we found them to be negligible, and we have excluded tunneling regimes of transport [9], [16] due to different temperature dependences.

IV. SUMMARY

In conclusion, we have presented results that are, at the best of our knowledge, the first experimental study of the behavior of the active cross-sectional area as a function of V_g for *undoped* FinFETs. In particular, we present conductance traces for a set of *undoped* FinFET devices having the same channel length and height but different width, together with TB simulations for the device of $W = 25$ nm, and we compare them to theoretical calculations. For all these small devices ($W \leq 125$ nm), we propose a mechanism of inversion of the bands from flatband to band bending in the interface regions, respectively, all as a function of V_g; therefore, we have, for the first time, directly observed the theoretical result suggested by Taur [5]. By means of our results, we have confirmed the validity of thermionic approach to investigate subthreshold transport in FET devices, and we have furthermore also given some answers to the fundamental technological question on how to localize and quantify areas of transport in these devices.

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