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***Abstract*—The experimental characterization of gate capacitance in nanoscale devices is challenging. We report an application of the charge-based capacitance measurement (CBCM) technique to measure the gate capacitance of a single-channel nanowire transistor. The measurement results are validated by 3-D electrostatic computations for parasitic estimation and 2-D self-consistent $sp^3s^*d^5$ tight-binding computations for intrinsic gate capacitance calculations. The device simulation domains were constructed based on SEM and TEM images of the experimental device. The carefully designed CBCM technique thus emerges as a useful technique for measuring the capacitance and characterizing the transport in nanoscale devices.**

***Index Terms*—Charge-based capacitance measurement (CBCM), nanowire MOSFETs, self-consistent C–V modeling, subfemtofarad-capacitance measurement.**

I. Introduction

With the rapid scaling of CMOS device technology, conventional bulk CMOS devices will soon reach their physical limits on the account of short-channel effects. Three-dimensional (3-D) multiple-gate device structures, such as FinFETs and nanowire and nanotube FETs, have been proposed for next-generation nanoscale technology for their superior subthreshold performance and, hence, lower leakage currents. The experimental characterization of the channel transport in these devices has been hampered due to the difficulty in measuring the capacitance that is typically below the femtofarad scale. The 3-D nature of these devices makes it impossible to have a large-area device for channel charge characterization, as is the case with bulk CMOS technology. Currently, characterization and modeling rely mostly on atomistic simulations and/or experimental capacitance data obtained from a large number of nanowires [1], [2] connected in parallel. However, enhancing the capacitance to a measurable level by connecting many devices in parallel masks the inherent variability at the nanoscale and is therefore undesirable. Tu *et al.* [3] reported the capacitance measurement of single nanowire channel at low temperature (150 K) using a conventional C–V meter. However, the method still suffers from high noise level due to the limited resolution of the instrument and large background capacitance.

In this letter, we report the measurement of gate capacitance on a single Si nanowire (SiNW) device using a carefully designed and calibrated charge-based capacitance measurement (CBCM) technique. We construct a realistic TCAD model with dimensions acquired from the SEM and TEM images of the structure of the characterized device after completing the electrical measurements and use COMSOL multiphysics [4] and the self-consistent $sp^3s^*d^5$ tight-binding model [5]–[7] to obtain the simulated capacitance for validation. This letter is perhaps the first one to present a comparison of the measured C–V data with the carefully constructed simulation model of a single-channel SiNW transistor. The results are of vital importance for characterizing the transport and variability in emerging research devices.

II. CBCM Test-Key Design, Fabrication, and Characterization

A few different circuit schematics have been proposed for on-chip implementation of the CBCM technique [8]–[10]. The accuracy of the three main variants of these was evaluated in [11] based on TCAD simulations. In this letter, we follow the charge-injection-induced error-free scheme proposed by Chang *et al.* [9], which measures two charging/discharging currents from exactly the same branch, eliminating the mismatch in the load. This is particularly important in our measurements since the pseudoinverter drivers are also nanoscale devices, and any mismatch of device dimension in the reference and device-under-test (DUT) branches can introduce significant

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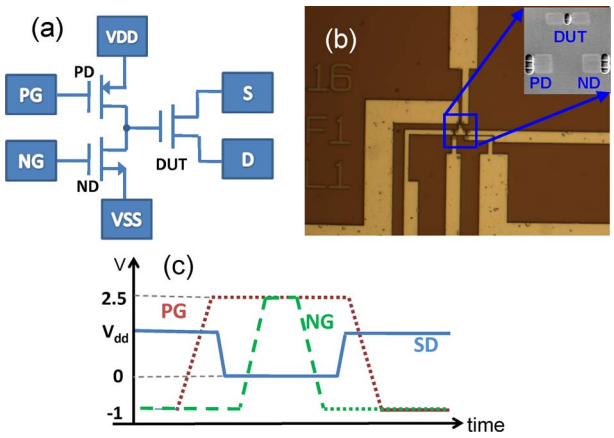

Fig. 1. (a) CBCM test key comprising a pseudoinverter, a DUT, and six input/output terminals. (b) Micrograph image of the fabricated test key. The inset shows the SEM image of the channels of the P driver, N driver, and single-finger DUT immediately after the local release of the SiNW. (c) Pulse inputs to PG, NG, S, and D terminals for the CBCM measurement of N-type SiNW DUT.

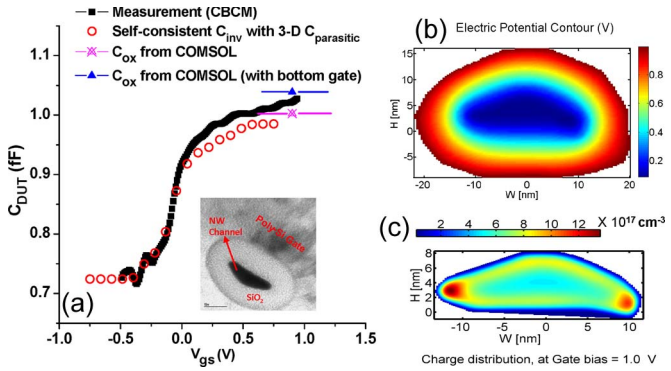

Fig. 2. (a) $C_{\rm DUT}-V_{\rm gs}$ curves of the single-channel SiNW transistor measured by the CBCM technique and self-consistent intrinsic SiNW gate capacitance simulated with the $\rm sp^3s^*d^5$ tight-binding model added with the 3-D electrostatic capacitance without considering NW in COMSOL [4]. The inset shows the TEM cross section of the SiNW channel. (b) and (c) Potential (in volts) and electron density (in units per cubic centimeter) in the channel obtained by self-consistent computation, respectively.

error in capacitance extraction. Measuring the two currents on a single branch with the same capacitance combination also helps reduce the error introduced by charge injection [11]. CBCM test keys with six input/output terminals were designed and fabricated, as shown in Fig. 1(a) and (b).

For fabrication, we modified the process flow in [12] by introducing the "local release" of the SiNW [as shown in the inset of Fig. 1(b)] to prevent the formation of a "gate poly-Si stringer" [13] around the source/drain (S/D) region. This significantly reduces the gate-to-source/drain parasitic capacitance. Single- and multiple-finger SiNWs are integrated as DUT in the CBCM test key. The drivers are SiNW devices with a gate length of 0.35 μm and a larger diameter (around $\sim$50 nm) to efficiently source/sink the charging/discharging current. The DUT has a gate length of 0.85 μm and a rounded triangular cross section with base of $\sim$22-nm length and $\sim$7-nm height. The gate oxide thickness is $\sim$9 nm, as seen from the TEM images.

The nonoverlapping pulses and voltages applied to terminals PG, NG, D, and S are shown in Fig. 1(c). The charging (or discharging) currents $I_{1,\rm VDD}$ and $I_{2,\rm VDD}$ through the VDD pad are monitored. A dc voltage is applied to the S/D pads for $I_{1,\rm VDD}$, while a third nonoverlapping pulse [SD in Fig. 1(c)] is applied for measuring $I_{2,\rm VDD}$ [9]. The bias-dependent gate capacitance of the DUT is then given by

$$C_{\rm DUT} = \frac{{\rm d}(Q_{1,\rm VDD} - Q_{2,\rm VDD})}{{\rm d}V_{\rm DD}} = \frac{{\rm d}(I_{1,\rm VDD} - I_{2,\rm VDD})}{{\rm d}V_{\rm DD}} \frac{1}{f}. \quad (1)$$

The measurement scheme was verified by comparing the gate capacitance of a 100-finger SiNW device measured with CBCM and LCR meter (HP4284). The test key had an additional small pad connected to the DUT gate for this purpose. A constant voltage of 0.75 V was applied to the S/D terminals, and the voltage at the VDD pad was varied between 0.1 and 1.85 V in steps of 10 mV, yielding a range of gate biases for DUT capacitance from -0.65 to 1.10 V. The frequency for the three nonoverlapping pulses was chosen to be 1 MHz for all measurements. The Agilent 4156C was used for the measurement of currents $I_{1,\rm VDD}$ and $I_{2,\rm VDD}$. Each current was measured 16 times, and their average value, after removing the outliers using Pierce's criteria [14], was used in (1). Furthermore, noise-free numerical derivatives were calculated following the algorithm by Savitzky and Golay [15]. The C–V curves derived from the CBCM technique for a 100-finger SINW transistor were found to agree well with the measurements from the LCR meter. For this purpose, we averaged 16 sets of LCR meter measurements to filter the noise for improved accuracy.

III. C–V Modeling of Single-Channel SiNW Transistor

The gate capacitance $C_{\rm DUT}$ of the single-channel SiNW transistor measured by CBCM is shown in Fig. 2(a), along with the TEM cross section of the channel in the inset. As the S/D contacts are n-type, we do not expect any significant capacitance on the accumulation side $(-{\rm ve}\ V_{\rm gs})$. However, a capacitance floor of $\sim$0.72 fF can be seen in the $C_{\rm DUT}-V_{\rm gs}$ curve. We further observed that the minimum capacitance increases linearly with the length of the S/D region (not shown here), suggesting that the origin of this minimum capacitance is parasitic related to the contact pads of the S/D regions.

To investigate this further at a reasonable level of complexity, we simulated the structure in two parts. For the first part, to get the intrinsic gate capacitance, the Schrödinger and Poisson equations were solved self-consistently for the exact cross section of the SiNW based on the TEM image using the $\rm sp^3s^*d^5$ tight-binding model [5]–[7] for density-of-state calculations. Fig. 2(b) and (c) shows the potential distribution and the electron distribution in the cross section of the structure. Significant crowding of electrons can be seen clearly at the corners of the rounded-triangle shape. Low electron concentration at silicon oxide interfaces is due to the quantum effect considered in the simulation.

Next, a 3-D device model was constructed in COMSOL multiphysics [4] based on the TEM and SEM images and layout

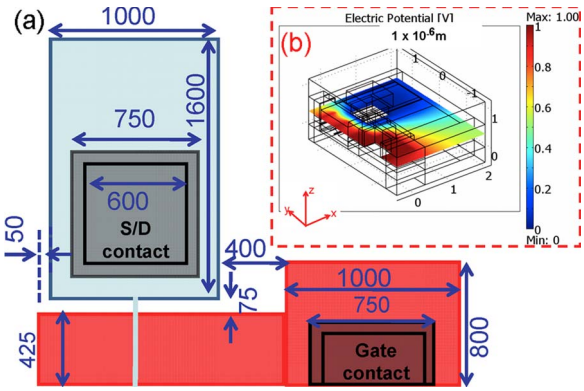

Fig. 3. (a) Top view of the simulation domain with dimensions for COMSOL multiphysics simulations (in nanometers; not to scale). (b) Potential distribution in the device structure (in micrometers) in the plane parallel to the wafer surface.

details of the DUT. Fig. 3(a) shows the simulation domain seen from the top (half of the device structure was considered taking advantage of the symmetry). Potential distribution plots in the planes parallel to the wafer surface are shown in Fig. 3(b). As expected, the potential changes sharply near the corners of the poly-silicon gate facing the S/D region, as well as in the narrow space separating the poly-Si gate contact region and the edge of the S/D region. The parasitic capacitance was estimated to be ∼0.71 fF, which is very close to the measured minimum capacitance for the single-finger device of the same gate length.

Fig. 2(a) shows very good agreement of the measured C_{DUT} with the sum of the simulated intrinsic and parasitic capacitances. The simulated gate capacitance in inversion (∼0.261 fF) from the self-consistent simulation is about 90% of the measured value (∼0.29 fF, measured from the minimum), and the sum of the self-consistent and parasitic capacitances is about 95.8% of the measured capacitance. A little larger value of the measured inversion capacitance is inferred to be due to the bottom-gated portion of the channel that extends from the gate-all-around region by 75 nm to both source and drain contact regions. The oxide capacitance increases by 3.6% when the bottom gate is considered in 3-D electrostatic simulations, as seen in Fig. 2(a).

IV. Conclusion

In this letter, we reported the design, fabrication, and characterization of a CBCM test key with SiNW transistors as DUT and drivers to measure the voltage-dependent capacitance at the subfemtofarad level from a single-channel SiNW device. The CBCM method was carefully verified by conventional LCR meter measurement on a DUT with large number of NW channels connected in parallel. Furthermore, the measured C–V characteristics have been validated by the 2-D self-consistent solution of the Schrödinger and Poisson equations and 3-D electrostatic calculation using the exact TEM cross sections and layout information. We conclude that the CBCM technique is capable of reliably measuring the capacitance in the hundreds-of-attofarad range for emerging 3-D CMOS devices such as FinFETs and nanowire and nanotube transistors.

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