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# Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors

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# Atomistic Full-Band Design Study of InAs Band-to-Band Tunneling Field-Effect Transistors

Mathieu Luisier and Gerhard Klimeck

***Abstract*—Band-to-band tunneling field-effect transistors (BTBT FETs) are expected to exhibit a subthreshold swing (SS) better than the 60-mV/dec limit of conventional metal–oxide–semiconductor FETs at room temperature. Through atomistic modeling of a suite of realistically extended InAs p-i-n single-gate (SG) and dual-gate (DG) ultrathin-body (UTB) and gate-all-around nanowire (GAA NW) devices with a gate length of 20 nm, we demonstrate that such a reduced SS can only be achieved if the electrostatic potential under the gate contact is very well controlled. We find that GAA NWs keep an SS less than 60 mV/dec for diameters larger than 10 nm, while the bodies in DG and SG UTBs must be scaled down to 7 and 4 nm, respectively. Still, all the considered devices are characterized by an ON current smaller than the ITRS requirements.**

***Index Terms*—Band-to-band tunneling (BTBT) transistors, full-band and atomistic quantum transport, subthreshold swing (SS), tight-binding.**

## I. Introduction

TUNNELING field-effect transistors (TFETs) have the potential to reduce heat dissipation in integrated circuits by offering low OFF currents and providing steep subthreshold swings (SSs) [1]–[10]. The voltage change required to increase band-to-band tunneling (BTBT) currents by a factor of ten is not limited to 60 mV at room temperature, as for thermionic currents in metal–oxide–semiconductor (MOS) FETs, but could theoretically reach values below 20 mV [1]. This implies that the switching from the OFF to the ON state of a TFET can be achieved by a lower voltage swing than in a MOSFET. Also, the operating voltage supply of a TFET can be made smaller, further reducing the power consumption.

There have been very few experimental demonstrations of SS lower than 60 mV/dec in TFETs [2], [3], and the resulting devices suffer from very low ON currents that do not fit to the ITRS requirements [11]. To enhance the ON current of TFETs, alternative channel materials like graphene [7], SiGe [8], or III–V compound semiconductors are investigated. InAs bears significant potential due to a very small direct bulk band gap ($E_g = 0.37$ eV), as well as light electron and hole effective masses ($m_e^* = 0.023m_0$ and $m_{lh}^* = 0.027m_0$), where BTBT naturally occurs under certain bias and doping conditions.

InAs-based BTBT FETs have not been fabricated yet, and it is not clear whether they will exhibit 1) low OFF current; 2) high ON current; and 3) steep SS. Through simulations with atomistic details and realistic device sizes, we aim to guide experimental work. We investigate single-gate (SG) and dual-gate (DG) ultrathin-body (UTB) and gate-all-around nanowire (GAA NW) InAs p-i-n TFETs with different thicknesses and diameters.

Accurate BTBT device design requires going beyond analytical solutions [9] and Wentzel–Kramers–Brillouin approximations [10] that are essentially 1-D, ignore the effects of quantization due to confinement, and do not capture the imaginary bands coupling the conduction and valence bands (CB and VB, respectively). We have developed an efficient 3-D atomistic full-band quantum transport simulator [12], [13] that ensures a correct description of the BTBT properties of any direct-band-gap material like InAs. Due to its computational complexity, such an approach has never been applied to realistically sized TFETs.

## II. Simulation Approach and Results

A 3-D atomistic full-band Schrödinger–Poisson solver with open-boundary conditions [12], [13] is used. Each In or As atom composing the device structures is represented in a nearest neighbor tight-binding basis, i.e., $sp^3s^*$ [14] for nanowires and $sp^3d^5s^*$ [15] for ultrathin bodies. The $sp^3s^*$ model considers only five orbitals, but it is almost as accurate as $sp^3d^5s^*$ for InAs, and it allows the computational simulation of larger devices, e.g., nanowires with a diameter greater than 5 nm. To speed up the simulations and to enable the analysis of large cross sections, we neglected spin-orbit coupling effects. We verified that this approximation affects the SS by less than 5%–10% and does not alter our conclusions.

Carrier and current densities are obtained by injecting electrons and holes into the device structures from the source and drain contacts at different energies and wave vectors. The calculation of electrostatic potential and of electron and hole populations are self-consistently coupled and parallelized to reduce the simulation time [16].

Fig. 1 shows the three different geometries considered here. The SG UTB, DG UTB, and GAA NW devices all measure 60 nm in length, divided into a 20-nm p-doped source region ($N_A = 5 \times 10^{19}$ cm$^{-3}$), a 20-nm undoped gate region, and a 2-nm n-doped drain region ($N_D = 5 \times 10^{19}$ cm$^{-3}$). The UTBs

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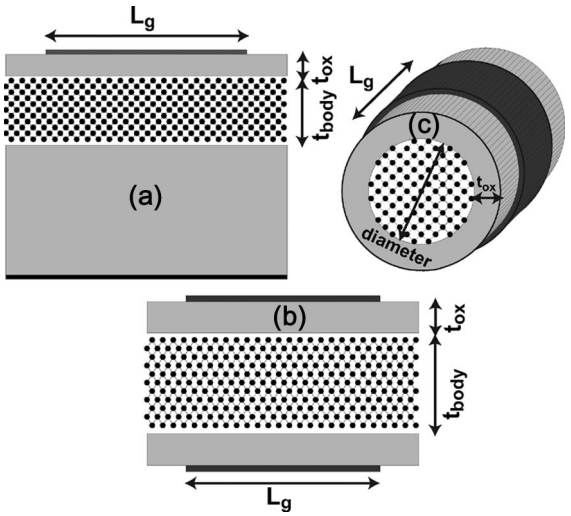


Fig. 1. Structure of the p-i-n InAs BTBT transistors considered in this letter. (a) SG UTB. (b) DG UTB. GAA NW. Devices (a) and (b) are characterized by a body thickness $t_{\rm body}$ ranging from 2 to 10 nm, and device (c) is characterized by a diameter $d$ ranging between 2 and 8 nm. The gate length $L_g = 20$ nm and "oxide thickness" $t_{\rm ox} = 1$ nm have the same dimensions in all three cases.

(NWs) have a body thickness $t_{\rm body}$ (diameter $d$) ranging from 2 to 10 nm. The largest simulated NW structure contains 169 191 atoms resulting in a Hamiltonian matrix of size $N = 845\,955$.

The transport direction $x$ is aligned with the $\langle 100 \rangle$ crystal axis where the highest BTBT probability is expected. The electron and light-hole effective masses of InAs are almost isotropic, and the heavy-hole effective mass has its smallest component along $\langle 100 \rangle$. Due to confinement, the electron effective mass of the lowest conduction subband is larger than the bulk value of $0.023m_0$. In SG and DG UTBs, it increases from $m^* = 0.032m_0$ for a body thickness of 10 nm to $0.064m_0$ for $t_{\rm body} = 2$ nm. Similarly, in 3-D NW structures, it goes from $m^* = 0.04m_0$ at $d = 10$ nm to $m^* = 0.138m_0$ at $d = 2$ nm.

The 1-nm-thick insulator separating the metal gate contact (work function $\phi_m = 4.27$ eV) from the semiconductor is made of a fictitious material with infinite band gap and a relative dielectric constant $\epsilon_r = 12.7$. The lack of tight-binding parametrization for insulator layers such as high-$\kappa$ materials and the difficulty of modeling the semiconductor–insulator interface justify this idealization, resulting mainly in a shift of the quantization levels to higher energies and an increase of the threshold voltage.

The room-temperature transfer characteristics $I_d$–$V_{\rm gs}$ (at $V_{\rm ds} = 0.2$ V) of SG UTB, DG UTB, and GAA NW TFETs with $t_{\rm body} = d = 6$ nm are shown in Fig. 2(a). The choice of a supply voltage $V_{\rm DD} = 0.2$ V is motivated by the desire of reducing the power consumption of devices and of avoiding the ambipolar behavior of TFETs that occurs at high $V_{\rm ds}$.

The GAA NW transistor is the only one to exhibit an SS lower than 60 mV/dec (28 mV/dec) over four orders of current magnitude. The SG UTB has an SS as large as 126 mV/dec. The differences in the device characteristics can be explained by observing their respective band edges and leakage paths as in Fig. 2(b)–(d). In these three subplots, the reference energy is the VB edge on the source side that corresponds to the energy of the highest valence subband in the source contact shifted by

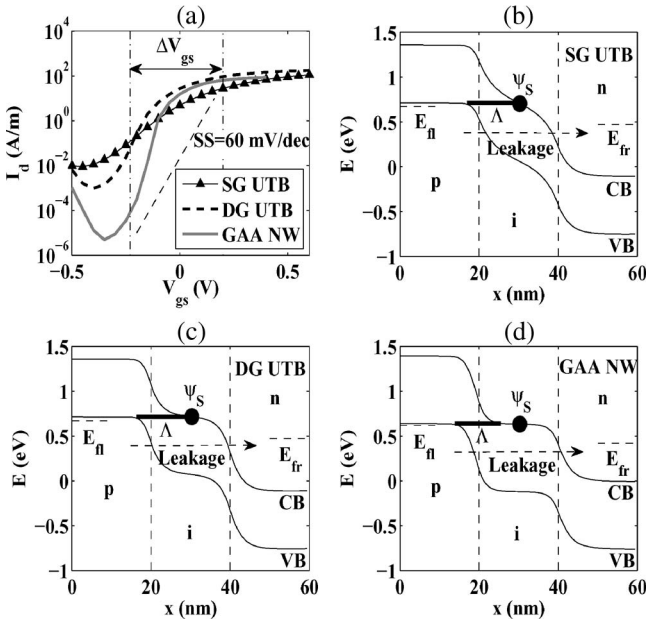


Fig. 2. (a) Transfer characteristics $I_d$–$V_{\rm gs}$ at $V_{\rm ds} = 0.2$ V of the (line with triangles) 6-nm SG UTB, (dashed line) SG UTB, and (gray line) GAA NW devices. The NW current is normalized with its diameter. The off-to-on gate voltage swing $\Delta V_{\rm gs}$ is indicated. (b) CB and VB edges along the transport direction $x$ of the 6-nm p-i-n SG UTB device at the threshold gate voltage. $\Lambda$ indicates the tunneling barrier width, $\psi_S$ is the electrostatic potential in the middle of the gate, and $E_{\rm fl}$ and $E_{\rm fr}$ denote the source and drain Fermi levels, respectively. (c) Same as (b) for the 6-nm DG UTB device. (d) Same as (b) and (c) for the 6-nm GAA NW device. Current leakage paths are indicated by dashed arrows in (b), (c), and (d).

half of the p-i-n built-in voltage $V_{\rm bi}$. The bulk VB maximum of the InAs tight-binding parameters is set to $E_{\rm VB} = 0.2243$ eV.

$$\mathrm{SS} = \frac{\delta V_{\rm gs}}{\delta \log_{10} I_d} = \frac{\delta V_{\rm gs}}{\delta \psi_S} \cdot \left( \frac{\delta \psi_S}{\delta \Lambda} \cdot \frac{\delta \Lambda}{\delta \log_{10} I_d} \right) = \frac{\delta V_{\rm gs}}{\delta \psi_S} \cdot \mathrm{SS}_{\rm int}. \quad (1)$$

A steep SS, defined in (1), is characterized by the following: 1) low leakage currents through the gate potential barrier and 2) a rapid decrease of the tunneling barrier $\Lambda$ over a wide energy range (tunneling window) [10] in response to a gate potential change $\delta V_{\rm gs}$. However, the gate does not act directly on the barrier width $\Lambda$ but on the electrostatic potential level in the middle of the channel $\Psi_S$. Ideally, the gate contact perfectly controls the electrostatic potential in the channel and $\delta V_{\rm gs}/\delta \psi_S = 1$ in (1). This is the case for the GAA NW and the DG UTB.

In conventional MOSFETs, the term $\mathrm{SS}_{\rm int}$ in (1) cannot be made smaller than 60 mV/dec at room temperature and is limited by the electron distribution in the source and drain contacts. In tunneling FETs, $\mathrm{SS}_{\rm int}$ varies from device to device and strongly depends on the electrostatic behavior in the channel. For the tunneling barrier $\Lambda$ to change rapidly and for the leakage current through the gate potential barrier to be as small as possible, the electrostatic potential in the channel should be as flat as possible. The GAA NW in Fig. 2(d) exhibits such a flat potential, while the SG UTB in Fig. 2(b) shows a linear potential drop. A strong gate control is the necessary condition

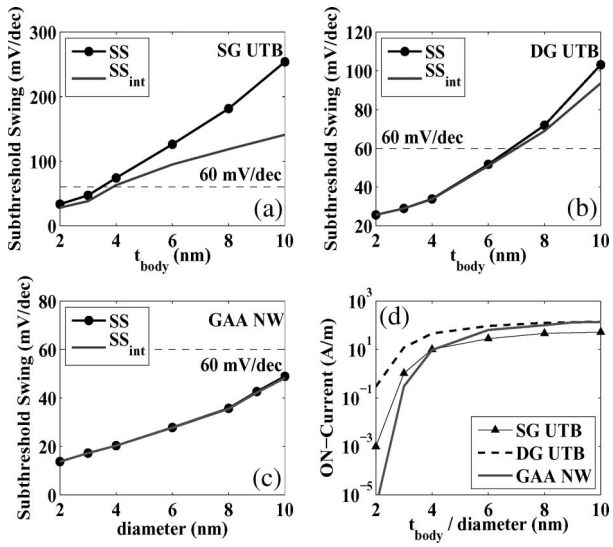


Fig. 3. (a) (Line with circles) Total (SS) and (gray line) intrinsic ($SS_{int}$) SSs of the SG UTB device with different body thicknesses $t_{body}$'s. (b) Same as (a) for the DG UTB device. (c) Same as (a) and (b) for the GAA NW device. (d) ON current $I_d$ at $V_{ds} = 0.2$ V and $V_{gs} = 0.2$ V as a function of SG UTB, DG UTB, and GAA NW device dimensions.

to make the terms $\delta\psi_S/\delta\Lambda$ and $SS_{int}$ as small as possible in (1). Finally, the term $\delta\Lambda/\delta\log_{10} I_d$ mostly depends on the InAs material properties and does not really distinguish our three device categories.

Fig. 3 reports the SS, $SS_{int}$, and ON current of the three device structures with different dimensions. The ON current is measured at $V_{ds} = 0.2$ V and $V_{gs} = 0.2$ V. A large gate voltage swing of about 0.4 V is required to obtain acceptable ON currents and ON/OFF-current ratio. However, it limits the functionality of InAs-based TFETs as logic gates, and it is in contradiction with the desired reduction of power consumption. Since the electrostatic control improves by reducing the device dimensions, an SS lower than 60 mV/dec can be reached in SG UTB with a body thickness smaller than 4 nm and in DG UTB with $t_{body} \leq 7$ nm. However, the ON currents of such devices are limited to 10 and 110 $\mu A/\mu m$, respectively, which are much below the ITRS requirements [11]. The GAA NW TFET appears more interesting since, at $d = 10$ nm, its SS amounts to 48 mV/dec only, but the leakage currents through the gate potential barrier, as shown in Fig. 2(d), drastically increase when the NW diameter becomes larger than 8 nm. Furthermore, the ON current of the GAA NW TFET saturates around 130 $\mu A/\mu m$, which is too low to challenge state-of-the-art MOSFETs.

## III. Conclusion

We have performed 3-D simulations of SG, DG, and GAA InAs BTBT transistors with different dimensions using an atomistic full-band Schrödinger–Poisson solver. TFETs are more sensitive to the control of the electrostatic potential under the gate than conventional MOSFETs, so that InAs single-gate UTB devices with a gate length of 20 nm have to be reduced to a thickness of 4 nm or less to exhibit an SS lower than 60 mV/dec, resulting in a very small ON current. GAA NW TFETs can keep SS $<$ 60 mV/dec up to diameters larger than 10 nm, but with low ON currents. Further structure and parameter optimizations like gate length, position, configuration, doping concentration, choice of supply voltage, or insulator design are necessary to make InAs TFETs viable. A careful investigation of the high-frequency properties of InAs TFETs is also required to determine their potential as logic gates.

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## References

[1] Q. Zhang, W. Zhao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 297–300, Apr. 2006.

[2] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196 805, Nov. 2004.

[3] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. King Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.

[4] V. Nagavarapu, R. Jhaveri, and J. C. S. Woo, "The tunnel source (PNPN) n-MOSFET: A novel high performance transistor," *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1013–1019, Apr. 2008.

[5] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-$\kappa$ gate dielectric," *IEEE Trans. Electron Devices*, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

[6] S. O. Koswatta, M. S. Lundstrom, and D. E. Nikonov, "Influence of phonon scattering on the performance of p-i-n band-to-band tunneling transistors," *Appl. Phys. Lett.*, vol. 92, no. 4, p. 043 125, Jan. 2008.

[7] Q. Zhang, T. Fang, H. Xing, A. Seabaugh, and D. Jena, "Graphene nanoribbon tunnel transistors," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1344–1346, Dec. 2008.

[8] N. Patel, A. Ramesha, and S. Mahapatra, "Drive current boosting of n-type tunnel FET with strained SiGe layer at source," *Microelectron. J.*, vol. 36, no. 12, pp. 1671–1677, Dec. 2008.

[9] W. G. Vandenberghe, A. S. Verhulst, G. Groeseneken, B. Soree, and W. Magnus, "Analytical model for a tunnel field-effect transistor," in *Proc. 14th IEEE MELECON*, 2008, pp. 923–928.

[10] J. Knoch, S. Mantl, and J. Appenzeller, "Impact of the dimensionality on the performance of tunneling FETs: Bulk versus one-dimensional devices," *Solid State Electron.*, vol. 51, no. 4, pp. 572–578, Apr. 2007.

[11] *International Technology Roadmap for Semiconductors 2007*. [Online]. Available: http://www.itrs.net

[12] M. Luisier, G. Klimeck, A. Schenk, and W. Fichtner, "Atomistic simulation of nanowires in the $sp^3d^5s^*$ tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B, Condens. Matter*, vol. 74, no. 20, p. 205 323, Nov. 2006.

[13] M. Luisier, A. Schenk, and W. Fichtner, "Atomistic treatment of interface roughness in Si nanowire transistors with different channel orientations," *Appl. Phys. Lett.*, vol. 90, no. 10, p. 102 103, Mar. 2007.

[14] G. Klimeck, R. C. Bowen, T. B. Boykin, and T. A. Cwi, "$sp^3s^*$ tight-binding parameters for transport simulations in compound semiconductors," *Superlattices Microstruct.*, vol. 27, pp. 519–524, May 2000.

[15] T. B. Boykin, G. Klimeck, R. C. bowen, and F. Oyafuso, "Diagonal parameter shifts due to nearest-neighbor displacements in empirical tight-binding theory," *Phys. Rev. B, Condens. Matter*, vol. 66, no. 12, p. 125 207, Sep. 2002.

[16] M. Luisier and G. Klimeck, "A multi-level parallel simulation approach to electron transport in nano-scale transistors," in *Proc. CM/IEEE Conf. Supercomput.*, 2008, p. 12.