2-1-1992

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TR-EE 92-8

February 1992

This research was supported by Grant from Delco Electronics.

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I. Introduction

Accelerometers and pressure sensors, two typical examples of integrated silicon sensors, utilize a thin semiconductor diaphragm structure. The thin diaphragm, which is formed by selective etching of the silicon, is used as a stress magnifying device. A piezoresistive sensor, which utilizes the piezoresistive effect of silicon, is the most widely employed type of sensor using the thin diaphragm. This is due to its easier fabrication, smaller area consumption, larger dynamic response, and more linear response compared to other types of sensors. For the piezoresistive sensors, a full Wheatstone bridge of diffused resistors is usually formed in a (100) oriented silicon diaphragm to detect the physical stimulus by an electrical output. The piezoresistive effect is a change in the resistivity with applied pressure, which is due to the change of the carrier mobility in the resistors.

In the 1980s, most sensor development had shifted to the use of solid-state batch processes, and there were several important devices in high-volume production. Part of this change was sparked by the automotive industry and its demand for high-volume, low-cost pressure sensing. The electrical performance of many sensors depends on the crystal quality and on an accurate thickness control of the thin silicon diaphragm structure. Thus far, thin silicon diaphragm formation has been controlled by either a boron etch-stop or an electrochemical p-n junction etch-stop technology where a p^+ diffused layer and a p-n junction are employed as etch-stop boundaries respectively. The draw-back of these technologies is that it is hard to obtain the abrupt doping profile with a desirable junction depth, especially with deep junctions. Hence it is difficult to control the membrane thickness. In addition, the heavily doped p^+ layer not only precludes the formation of electrical &vices in it, but also causes defects when the lightly doped n-type silicon is epitaxially grown on that layer. The electrochemical etch-stop is inconvenient to use in large scale manufacturing since elecmcal connections are required before etching each wafer.

A new technique which utilizes a merged epitaxial lateral overgrowth (MELO) of silicon combined with an SiO_2 etch-stop and a crystallographic self-limiting etch-stop was introduced last year. The result of the new technique is a high-quality silicon diaphragm, well-controlled in all dimensions. The MELO is an extension of the Selective Epitaxial Growth (SEG) and Epitaxial Lateral Overgrowth (ELO) technologies which have already been employed in the development of novel devices such as three dimensional MOS and bipolar transistors as well as silicon-on-insulator(SOI) devices. This indicates that the new diaphragm forming technique is IC-compatible and can improve the controllability and repeatability of the silicon diaphragm thickness and the diaphragm material quality as compared to existing techniques.

The $Si\text{-}SiO_2\text{-}Si$ structure, which results from merged ELO silicon on the SiO_2 mask, provides several advantages over other thin diaphragm techniques. First, SiO_2 plays a nearly perfect etch-stop when ethylenediamine or KOH-based solution is used for back-side etching. Hence the epitaxial silicon on the SiO_2 is completely protected from etching as shown in Figure 1.1. Therefore, this technique never needs any etching thickness monitoring which is necessary in the conventional methods. Secondly, the thickness can be controlled much more accurately than the boron diffusion and the boron buried layer etch-stop techniques since it is controlled by ELO growth rate, which can be made less than $0.1\mu m/min$. The growth rate can also be adjusted by the amount of dichlorosilane source gas, HCl, and growth temperature used in the LPCVD reactor. Thirdly, the minimum diaphragm thickness can be decreased to as small as 1 μm because the minimum thickness is limited only by the photolithography and etching of the SiO_2 mask.

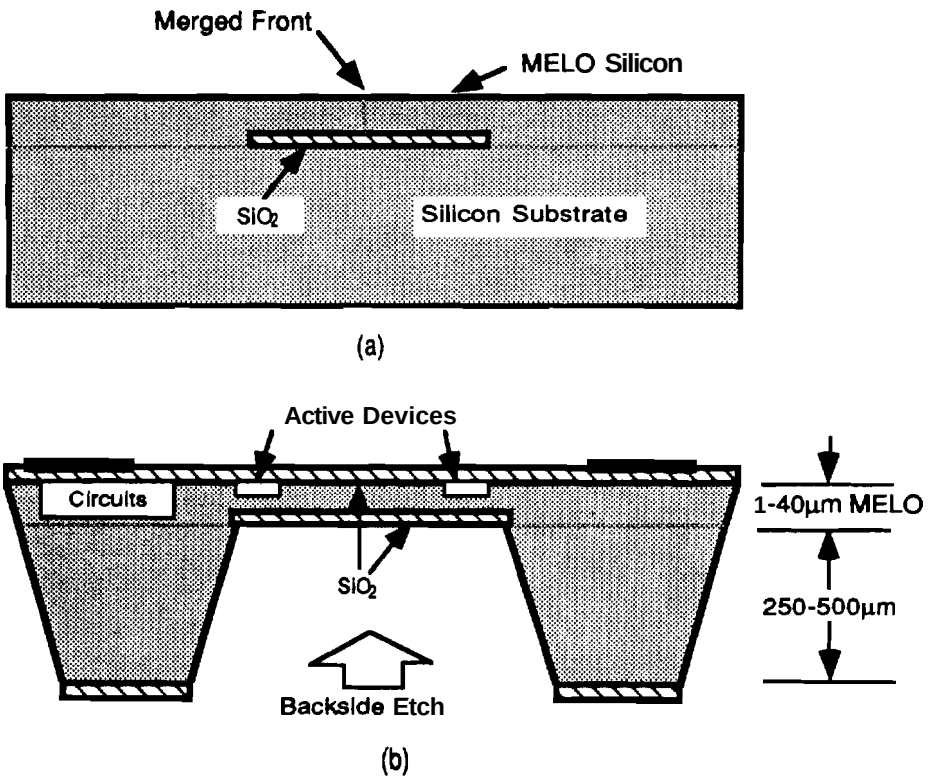


Figure 1.1. A novel method of forming thin silicon diaphragm of controlled thickness. (a) Merged ELO (MELO) structure on SiO_2. (b) Etch-stop by $Si\text{-}SiO_2\text{-}Si$ structure. Complete etch-stop is accomplished by SiO_2.

Note that because of an accurate thin silicon diaphragm, the lateral dimensions of sensing devices can be further reduced keeping identical sensitivity. The smallest dimension of SiO_2 can be as small as 2 μm wide without problems and the ELO growth necessary to make a diaphragm structure turns out to be a little greater than 1μm. The remaining SiO_2 can be etched with Buffered Hydrofluoric Acid (BHF). If thicker beams are necessary, SiO_2 can be left as a part of suspension beams or a thicker epitaxial layer can be grown.

The following is a summary of the proposed research activity extracted from the 1991 proposal. Each topis will be reported in the following chapters.

List of Proposed Research Activity in 1991

* Continuing investigation of MELO Technology
  - Check the effect of different seed window preparation such as wet etched 2μm, RIE with Fr115 or Fr116.
  - Examine the quality of the MELO silicon by fabricating diodes, bipolar transistors and p-type piezoresistors, etc.
  - Observe the effect of growth then anneal by further growth.
  - Explore the optimum condition for the MELO process.

* Realization of Silicon Thin Diaphragm
  - Investigate the crystallographic etching characteristics.
  - Design of KOH etching system
  - Optimize the anisotropic etch process such as temperature, the etching solution, cleaning glasswares, masking material.
  - Fabricate a silicon thin diaphragm and examine it.

* Fabrication and Evaluation of MELO Accelerometer
  - Layout Design of E-beam Mask Set Fabrication
  - Investigation of Proof Mass Comer Compensation
  - Examine Metal Passivation in KOH etch
  - Testing of MELO Accelerometer

Chapter II describes a review of the present understanding of SEG,ELO, MELO of silicon and its incorporation into the development of a new diaphragm formation technique. The MELO of silicon combined with the self-limiting crystallographic etch-stop was realized and a new diaphragm technology which allows precise diaphragm thickness control was verified. The results are divided into four parts. Initial work focused on characterization of the MELO structure and performance of the crystallographic etch-stop has been completed. Secondly, the uniformity of the MELO silicon film has been examined by evaluating the thickness variation in a wafer, and wafer-to-wafer at a reference point. Then the quality of the MELO silicon film has been investigated by fabricating defect sensitive devices, such as diodes or bipolar transistors, on both SEG and MELO silicon, and comparing their device characteristics. Crystal defect etching was also performed

Chapter III shows the application of MELO silicon to the fabrication of single crystal silicon membrane. First, the actual diaphragm structure that has been realized using the MELO structure and the crystallographicetch-stop is illustrated. Also, the seed window preparation by reactive ion etch (RIE) for the MELO structure was investigated. Secondly, a controlled temperature bath for KOH and EDP etching of silicon will be described. It was designed and built to aid in the fabrication for more consistent etch result. Finally, the characteristics of KOH etch with various parameters - crystal orientation, cleaning, temperature, doping concentration, masking material are presented.

Chapter IV represents an example of application of the MELO silicon diaphragm to silicon sensors - here, a MELO accelerometer. The detail of MELO accelerometer fabrication and the related subjects are presented in this chapter. First, its design and layout are described. A simple Wheatstone bridge circuit was employed without any compensation circuits. Different electrical devices such as resistors, diodes, bipolar transistors, capacitors, were included for characterization of the MELO silicon. Proof mass comer compensation was obtained from a series of back etch experiments and incorporated in the design. Secondly, the front and back-side protection was investigated. This is an important process step and could cause catastrophic results, even after the device fabrication was successfully completed, if it was not carefully examined. In addition, the front delineation is explained with a change in the sequence of process steps. Finally, the testing results of the MELO accelerometer are analyzed and the necessary changes of the design described.

Chapter V is a summary of the accomplishment in 1991.

II. Merged Epitaxial Lateral Overgrowth (MELO) Technology

2.1. SEG, ELO, MELO of Silicon

The selective epitaxial growth (SEG) of silicon has brought much attention for the development of various novel device structures. In SEG, the epitaxial deposition conditions are adjusted to prevent deposition on the mask regions, usually oxide, while epitaxial growth occurs on the exposed silicon in the seed windows (Figure 2.1(a)). Once the silicon grows vertically above the mask level, it then grows laterally over the oxide mask as it continues its vertical growth (Figure 2.1(b)). This is referred to as epitaxial lateral overgrowth (ELO), and it constructs a locally silicon-on-insulator (SOI) structure. The epitaxial process can be continued even further until two ELO fronts from different seed windows meet, forming a continuous film of single crystal silicon, or merged ELO (MELO) (Figure 2.1 (c)). Continued growth resulted in a flat and uniform top surface. The thin silicon diaphragm beams are realized by protecting the top of the MELO film and etching from the back-side of the wafer until the etch is terminated by the silicon dioxide and for large diaphragm on the SiO_2 V-groove etch-stop as shown in Figure 2.1(d).

There are several process conditions to be considered in order to achieve good quality MELO, which can be used for silicon micromachined sensors. Since MELO is just a continuation of ELO, the process conditions considered to improve ELO/SEG are also applied to the MELO technique. For the SEG and ELO process, the selectivity of silicon growth is the first concern, i.e. the nucleation of polysilicon on the masking material must be limited. The nucleation depends on the masking material, deposition temperature, pressure, and the carrier gas. It has been found experimentally that nucleation generally occurs somewhat less on silicon dioxide than on silicon nitride. In addition, the nucleation can be suppressed by using reduced reactor pressure, lowering the deposition temperature, and adding HCl gas to the silicon process gases.

The crystal quality of SEG/ELO depends on several deposition conditions such as deposition temperature, pressure, seed surface condition, seed window orientation, masking material, and contaminants in the reactor. First of all, oxide has been proved to be the better masking material than nimde, since nitride generates more stacking faults along SEG sidewalls than does oxide. Therefore, oxide is generally used as the masking material. Typical defects generated by interaction between oxide edges and ELO silicon are edge dislocations and stacking faults. These effects are believed to be a result of the stress relief

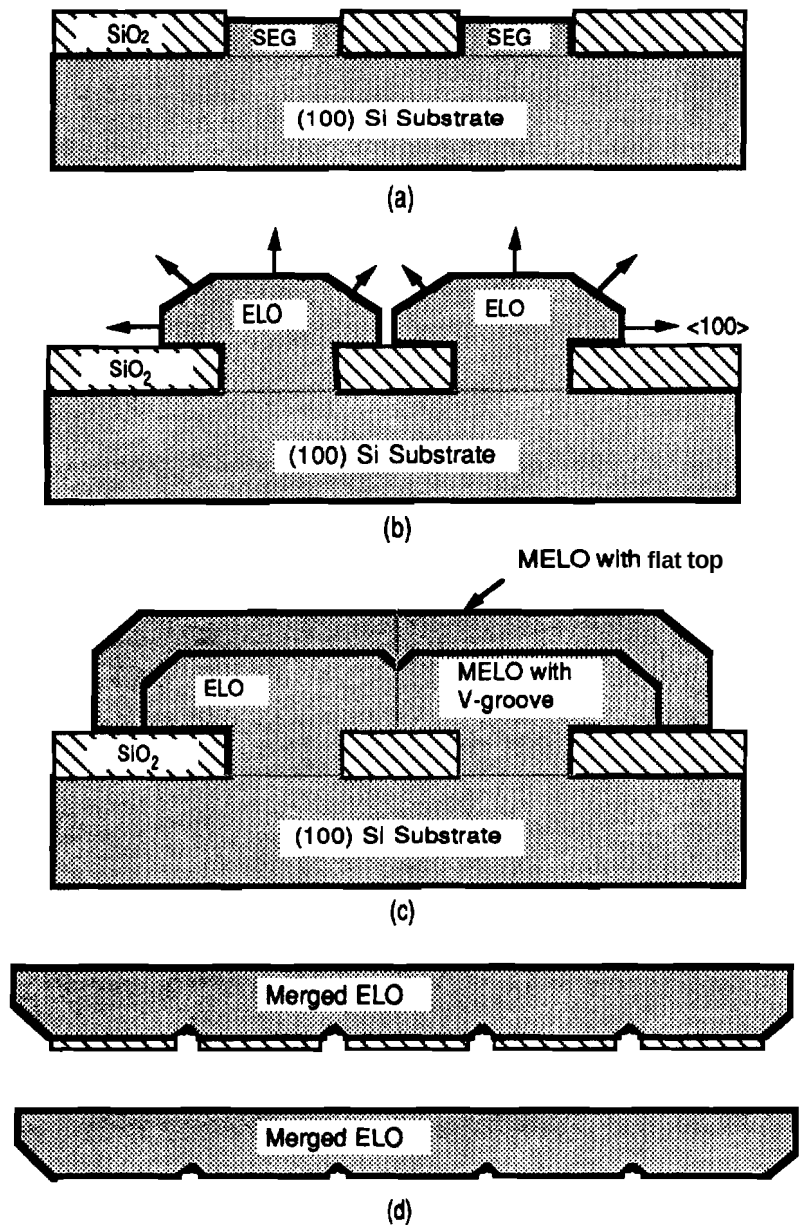


Figure 2.1. A wide and thin diaphragm formation using MELO silicon combined with V-groove self-limiting etch-stop. (a) Selective epitaxial growth (SEG) of silicon. (b) Epitaxial lateral overgrowth (ELO). (c) Merged ELO (MELO). (d) Thin diaphragm structure with oxide, and after the oxide is removed.

caused by the difference in the thermal expansion between the silicon and the oxide during cooling from the growth temperature. The density of these defects in SEG/ELO can be reduced by lowering the growth temperature.

The seed window orientation also has an effect on the SEG material quality. Films grown on the seed windows aligned to <110> directions exhibit a larger density of defects than those grown on seed windows aligned to <100>. Another important factor in the process is the surface condition of seeds. SEG material grown on (100) substrates shows superior quality to that grown on (111) substrates because of their lower probability of stacking fault nucleation. An in-situ precleaning with a hydrogen bake to remove the substrate's native oxide before epitaxy, is also critical to the SEG material quality. It is believed that H_2 at high temperature acts as a reducing agent and removes chemical species that interfere with perfect single crystal formation. It is known that at low pressure and high temperature SiO_2 is removed by the H_2. Low pressure also enhances the H_2 reduction process by encouraging the removal of other foreign atoms from the surface. A RCA clean prior to loading the wafer into the reactor forms a very thin SiO_2 layer that also protects the growing surface.

The use of HCl also decreases defect density on SEGELO films. However, if too much of HCl is used in the cleaning step, the undercut between silicon and SiO_2 mask may occur. Also a high temperature (>1000 °C) H_2 bake can cause the undercut. Recently, the effects of water vapor and oxygen levels in the epitaxy environment were investigated. At the same temperature and pressure, the quality of SEG/ELO improves with the reduction of water vapor and oxygen level in the reactor. It was determined experimentally that the critical temperature, above which deposition of good crystal quality epitaxy is possible, is governed by the moisture and oxygen partial pressure during preclean and growth.

The method of etching the masking oxide also affects quality of the SEG material since the sidewall angle of the oxide is related to defect generation at the interface. It is found that the vertical sidewalls tend to yield the best SEG. Wet etching of the oxide never achieves a vertical sidewall due to its isotropic etching characteristics. The undercut of the photoresist leaves a near 45' slanted wall. Anisotropic reactive ion etching (RIE) should, ideally, create the vertical sidewall. However it often creates radiation damage to the seed surface, leading to defects in the SEG. In order to maintain the vertical sidewalls and to heal the surface damage, RIE followed by a sacrificial oxide, which is wet etched, is an alternative.

Uniformity of **SEGELO** film on a wafer is very important to obtain consistent accelerometer results between devices from the same wafer and between epitaxial runs. The local growth rate of **SEG/ELO** can be different depending on the ratio of the exposed silicon seed area to oxide covered **area.** It appears that growth rates increase locally as the exposed silicon **area** decreases. This phenomenon can occur on a device scale or on a wafer scale depending on the selective epitaxial process conditions. This is called a "loading effect" and is not desirable since it causes non-uniformity across a wafer and even in a single die. Loading effects can be reduced at low deposition temperatures, at reduced pressures, and with higher HCl concentrations during growth. Also, it is less significant at larger Si/SiO_2 surface ratios where most wafer area is exposed. Typically at greater than 30% excellent uniformity is obtained, approaching the full wafer uniformity.

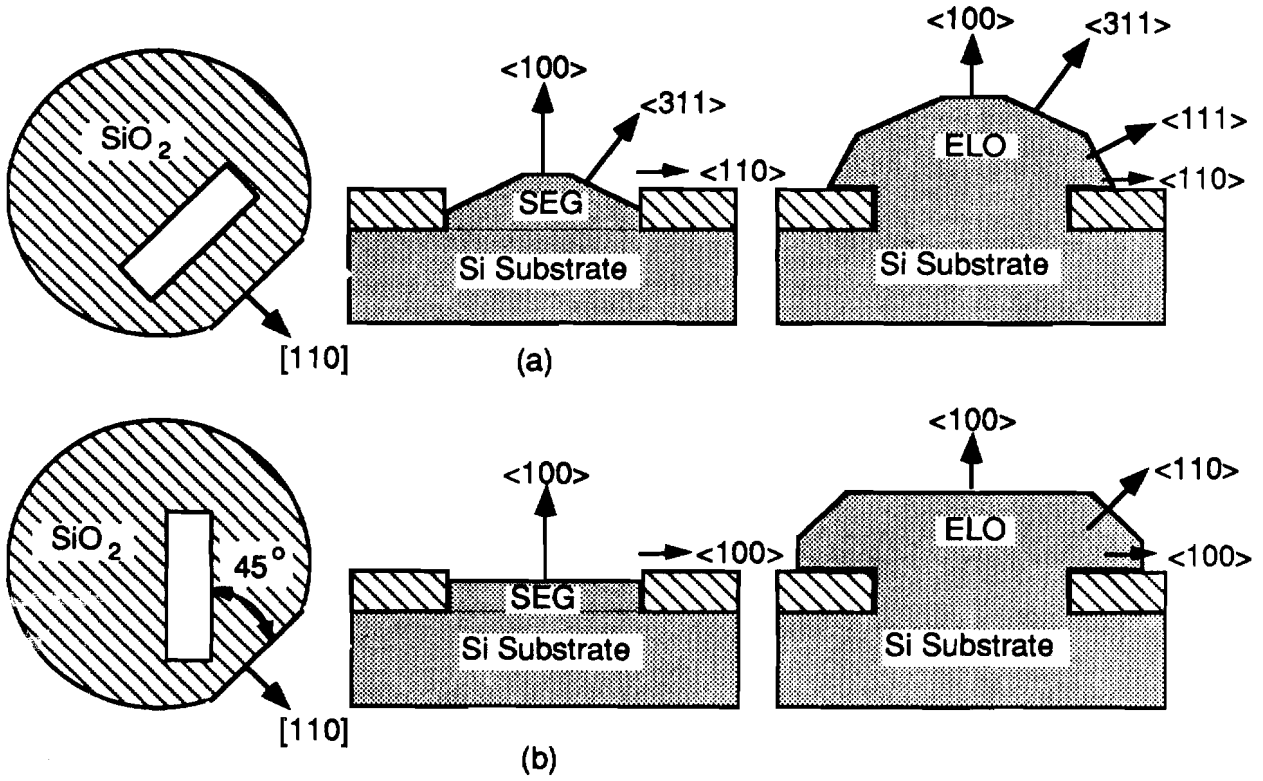


Figure 2.2. Facet formation depending on the seed window orientation. (a) When oxide pattern is aligned to **<110>** directions. (b) When oxide pattern is aligned to **<100>** directions.

The shape of SEG/ELO films and facet formation are determined by the difference of the growth rates between several growing crystal planes. The formation of a facet can be reduced by making seeds oriented along <100> directions, lowering the deposition temperature, reducing the pressure, and increasing HCl concentration. The morphology of SEG films is highly dependent on the orientation of the oxide sidewall with respect to the orientation of the oxide. When the sidewall is parallel to {110) planes, the SEG film typically exhibits {311) facets adjacent to the sidewalls. As the film continues to grow over the oxide, then (111) facets appear on the ELO film as shown in Figure 2.2(a). When the oxide pattern is parallel to (100) planes, less faceting is observed on the SEG and (110) planes are often observed after overgrowth begins as shown in Figure 2.2(b).

Adding HCl, in addition to suppressing polysilicon nucleation on the oxide, changes the growth rate of the (100) planes relative to that of the (110) planes. A high HCl partial pressure increases the growth rate of the {110) planes with respect to that of the (100) planes so that the slow-growing (100) planes remain to bound the deposit, and vice versa (Figure 2.3). Controlling the HCl partial pressure during deposition allows the possibility of varying the shape of the ELO fronts and consequently obtaining satisfactory coalescence of two growth fronts. When a high HCl partial pressure is used, the lateral growth planes become nearly vertical and they may meet together so as to generate a perfect MELO structure without any groove on the top. However, if they meet first near the upper edge of the vertical (100) planes, they may leave a void below the point where the growth fronts first meet (Figure 2.3(c)). On the other hand, if a lower HCl partial pressure is used, faceted growth fronts with only a small vertical (100) plane will be developed and consequently minimize or eliminate the void when they coalesce. In this case, a V-groove will appear on the top MELO structure and longer epitaxy is necessary to obtain a flat top MELO. An alternative is that once the growth fronts merge then the HCl concentration can be changed to enhance the {110) growths and forms the flat top quicker.

For the growth of high quality SEG/ELO material, low temperature, reduced pressures, and addition of HCl in the process gas are generally preferred even though the growth rates are reduced. These conditions give advantages such as: enhanced selectivity, better SEG planarity, fewer stacking faults at the SEG sidewalls, less loading effects, reduced faceting, and fewer crystal defects and polysilicon nucleation.

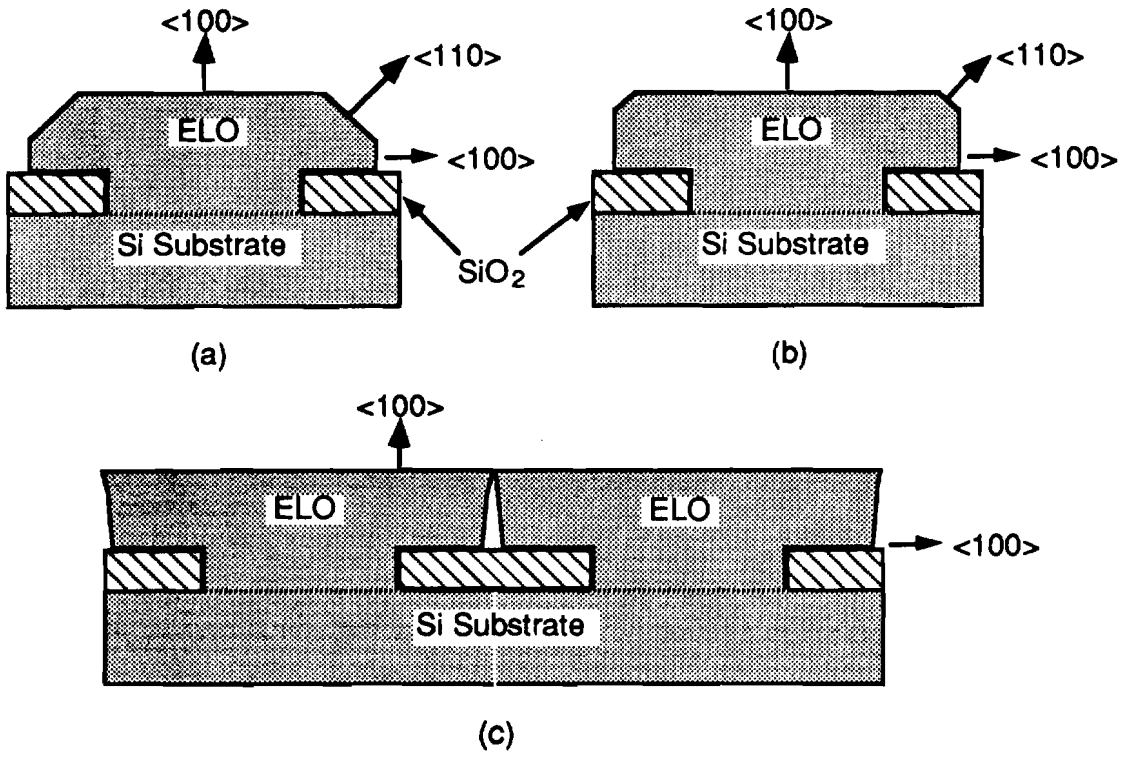
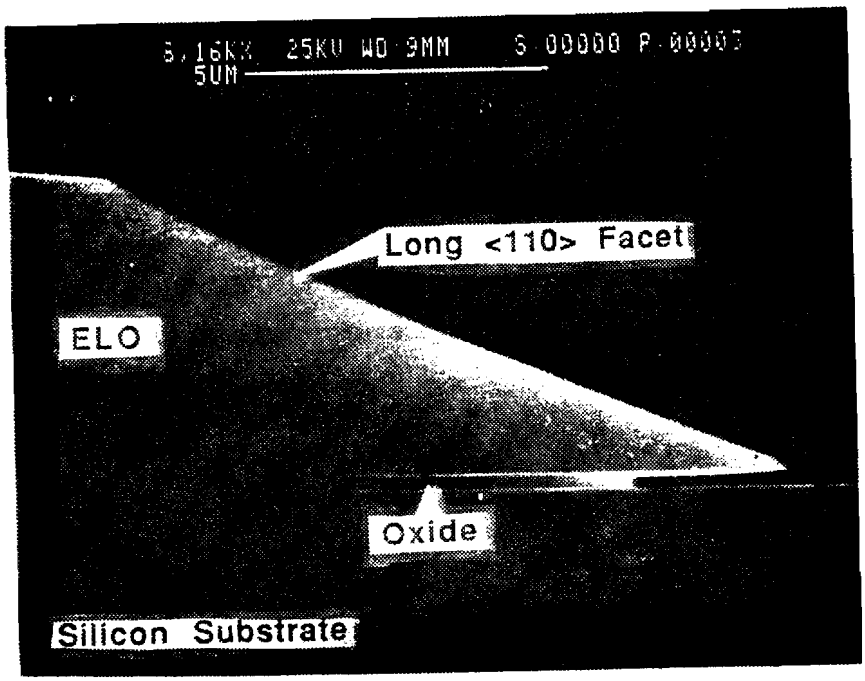
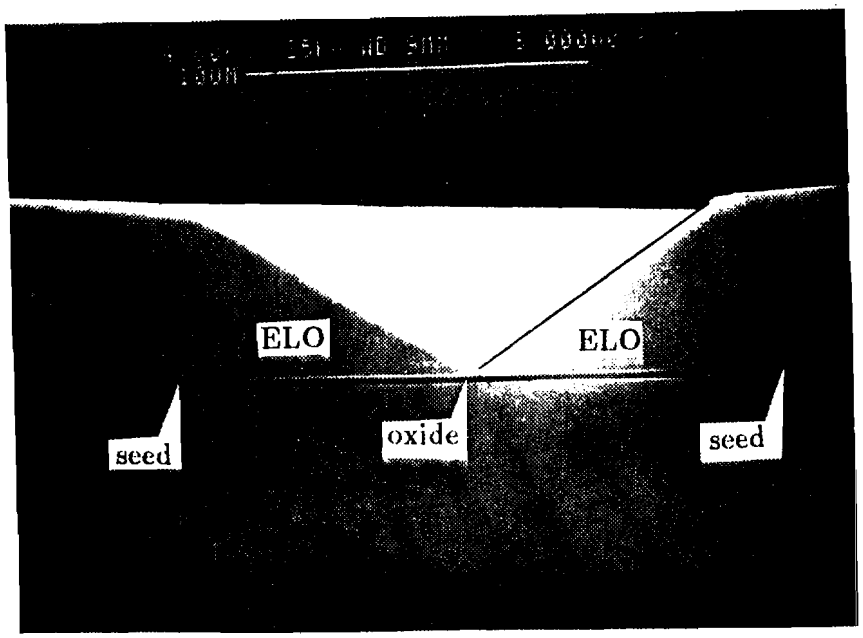


Figure 2.3. Facet formation depending on the HCl partial pressure. (a) With little HCl into the process gas. (b) With more HCl into the process gas. (c) When too much HCI is used, the top of ELO fronts meet first and a void may occur.



(d)



(e)

Figure 2.3. Facet formation depending on the HCl partial pressure. (d) SEM photograph of a enlongated <110> facet resulted from the reduced HCl gas content in SEG/ELO process. (e) SEM photograph of merging ELO fronts showing no voids.

2.2. Uniformity of MELO silicon

Two most important parameters of an accelerometer are its sensitivity and dynamic response. Sensitivity of an accelerometer is defined as the fractional change in output voltage due to applied acceleration divided by the product of the circuit supply voltage times the acceleration. The bandwidth of an accelerometer is determined by its first resonant frequency since in this region the sensitivity varies and the response of the accelerometer is distinctly nonlinear. Using an idealized two-dimensional structure in modeling the bridge-type accelerometer, analytical results for the maximum sensitivity, S_o, and resonance frequency, f_o, can be obtained. As shown in Equations (2.1) and (2.2), the thickness, t, is more dominant than other terms such as beam length (l_1), beam width (w), number of beams (n), and proof mass (m_2) in both equations.

$$S_o = 3\,\pi_l \left[\frac{m_2 l_1}{wnt^2}\right] \tag{2.1}$$

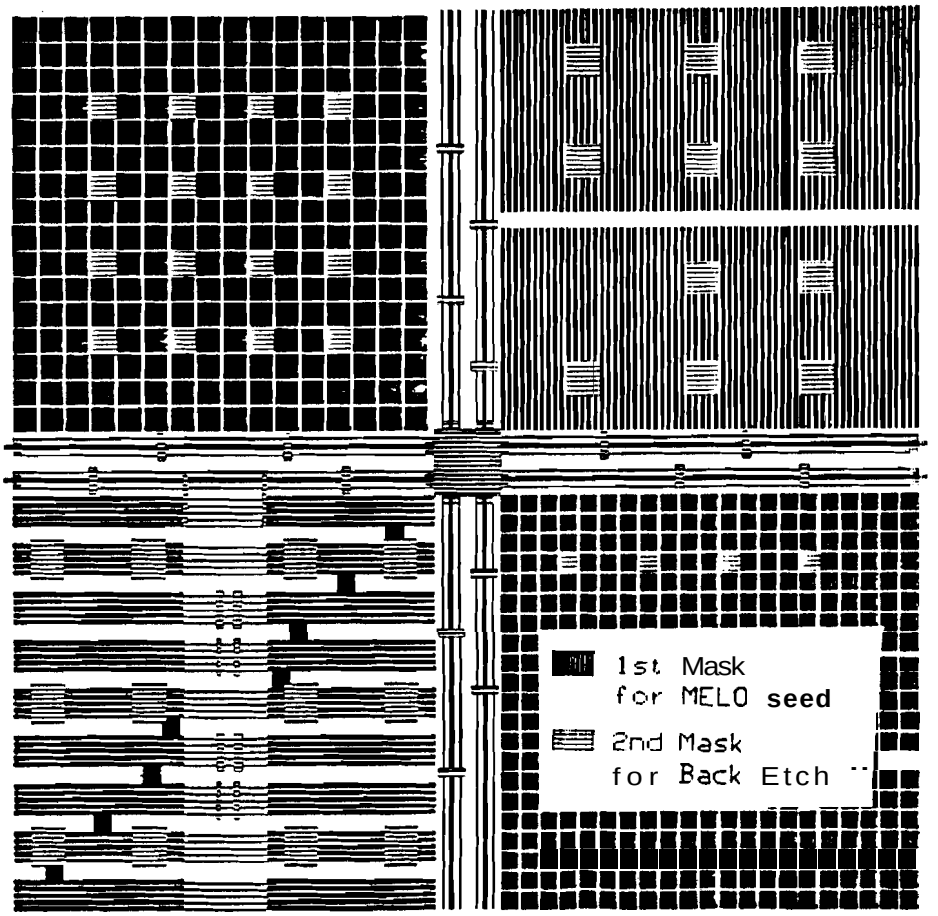
$$f_o = \frac{1}{2\pi}\left[\frac{nwEt^3}{l_1^3 m_2}\right]^{1/2} \tag{2.2}$$

Therefore the control of the thickness becomes quite important for the fabrication of sensitive and consistent accelerometers, hence the uniformity of the MELO silicon was examined throughout the research whenever possible.

Selective growth was carried out in Gemini I LPCVD reactor, an R-F heated pancake reactor, in the Purdue University Solid State Laboratory. After the wafers were placed in the reactor, they were heated to the deposition temperature of 970°C or 1020°C. Then they were subjected to a 5 minute bake, in a hydrogen ambient at 40 or 150 Torr, which is the deposition pressure, to remove any remaining native oxide from the wafer surface. Subsequently, HCl was introduced and the substrates were etched for a short time, typically 30 seconds. Thereafter dichlorosilane was added as a silicon source gas to initiate the deposition and HCl gas was added to enhance the selectivity by preventing the formation of polysilicon on the silicon dioxide. ELO growth rates of approximately 0.1 μm/min have been accomplished. These conditions led to planar SEG with good selectivity and minimum visible defects. The growth morphology was examined using the scanning electron microscope (SEM) and a Nomarski illuminated microscope.

A test mask, illustrated in Figure 2.4, was designed,produced, and implemented for realizing a wide thin silicon diaphragm using the MELO technology and the new etch-stop as well as for MELO growth rate characterization. The growth rate of the MELO films was calculated by measuring the film thickness over the large oxide regions (>100μm) with an alpha step profilometer. Figure 2.5 shows the places on the wafer where the measurements were taken. Positions 1 through 8 correspond to the large oxide islands in quadrant #3. These islands are clearly shown on the mask layout in Figure 2.4. Note that each vertical bar in quadrant #1 of Figure 2.4 consists of a set of 5 x 1200 μm^2 rectangular oxide islands separated by 2μm wide seed holes.

QUADRANT #2 QUADRANT #1



QUADRANT #3 QUADRANT #4

Figure 2.4. Layout of the second test mask.

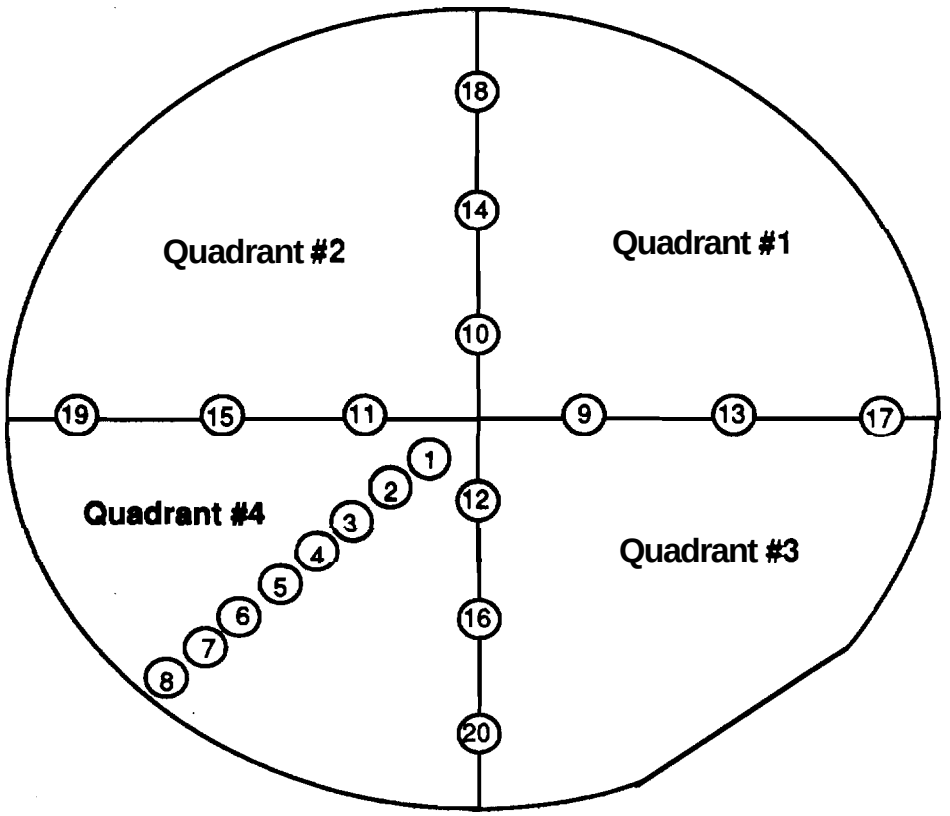


Figure 2.5. MELO thickness measuring positions on the wafer.

Table 2.1 is an example of the statistical results of the MELO silicon growth on the wafers over four different selective epitaxial runs. All wafers in each run used the same pattern and orientation. The silicon film thickness analysis is taken across the wafer; in other words, twenty different positions (shown in Figure 2.5) across each wafer were measured for silicon film thickness. To help understanding the summary tables, refer to the original data sheet of the first epi run given in Figure 2.6. Statistical parameters, such as the average growth, the standard deviation, and the percent variation are calculated across a wafer (down a column) over twenty different locations. Thus, the last three rows in Figure 2.6 are the values listed in the middle three columns of Table 2.1. However, note in the data sheet that the same parameters may be calculated for a particular location (on the wafer) over all wafers, shown in the last three columns. These parameters have a wafer to wafer basis and are not listed in the summary tables. To better visualize the wafer to wafer parameters per run, the ELO thickness for the wafers of Table 2.1 has been plotted against position (Figure 2.7; also known as growth profile), and the standard deviation and the percent variation of all wafers are graphed versus position as well (Figure 2.8). The significance between the parameters within a wafer and the parameters with a wafer to wafer basis will become apparent in the following discussion.

TABLE 2.1

Statistical Results of ELO Growth

Run #1:

growth condition: 80 min. at 1020°C
Pressure: 150 Torr
Oxide thickness: approx. 0.5µm

Wafer	Avg. Growth	Std. Dev.	% Variation	Avg. Growth Rate
GT5	10.43µm	0.30µm	2.90	0.130µm/min
GT6	10.48µm	0.59µm	5.65	0.131µm/min
GT4-tn	10.08µm	0.44µm	4.32	0.126µm/min
GT5-tn	10.11µm	0.45µm	4.44	0.126µm/min
GT6-tn	10.37µm	0.40µm	3.84	0.129µm/min
GT7-tn	10.17µm	0.60µm	5.87	0.127µm/min

Run #1 Data Sheet

Position	GT5 (μm)	GT6 (μm)	GT4-tn (μm)	GT5-tn (μm)	GT6-tn (μm)	GT7-tn (μm)	Avg. W to W (μm)	Std. Dev (μm)	% Var
1	10.34	10.49	10.06	9.985	10.26	10.22	10.23	0.18	1.72
2	10.29	10.33	9.905	9.845	10.09	10.02	10.08	0.17	1.68
3	10.22	10.16	9.77	9.745	10.05	9.89	9.97	0.16	1.61
4	10.25	10.07	9.685	9.66	9.905	9.68	9.88	0.16	1.64
5	10.06	9.725	9.4	9.405	9.73	9.355	9.61	0.17	1.75
6	10.01	9.59	9.34	9.35	9.69	9.235	9.54	0.17	1.79
7	9.74	9.39	9.135	9.2	9.68	9.06	9.37	0.22	2.37
8		9.28				8.975	9.13	0.15	1.67
9	10.67	11.04	10.52	10.46	10.61	10.67	10.66	0.20	1.91
10	10.71	11.14	10.57	10.65	10.91	10.85	10.81	0.20	1.86
11	10.74	11.05	10.58	10.56	10.85	10.78	10.76	0.18	1.69
12	10.86	11.15	10.59	10.61	10.8	10.74	10.79	0.20	1.87
13	10.64	11.07	10.38	10.44	10.57	10.6	10.62	0.24	2.29
14	10.52	10.94	10.41	10.57	10.78	10.8	10.67	0.19	1.75
15	10.71	10.8	10.43	10.47	10.75	10.71	10.65	0.15	1.43
16	10.8	11.03	10.42	10.47	10.68	10.51	10.65	0.22	2.08
17	10.55	10.89	10.2	10.27	10.4	10.41	10.45	0.24	2.31
18	10.1	10.37	9.94	10.28	10.43	10.47	10.27	0.19	1.85
19	10.36	10.35	10.06	10.13	10.56	10.34	10.30	0.18	1.72
20	10.62	10.65	10.19	10.08	10.37	10.11	10.34	0.21	2.04
Avg. Growth (μm)	10.43	10.48	10.08	10.11	10.37	10.17			
Std. Dev (μm)	0.30	0.59	0.44	0.45	0.40	0.60			
% Var.	2.90	5.65	4.32	4.44	3.84	5.87			

Figure 2.6. Data sheet of Run #1

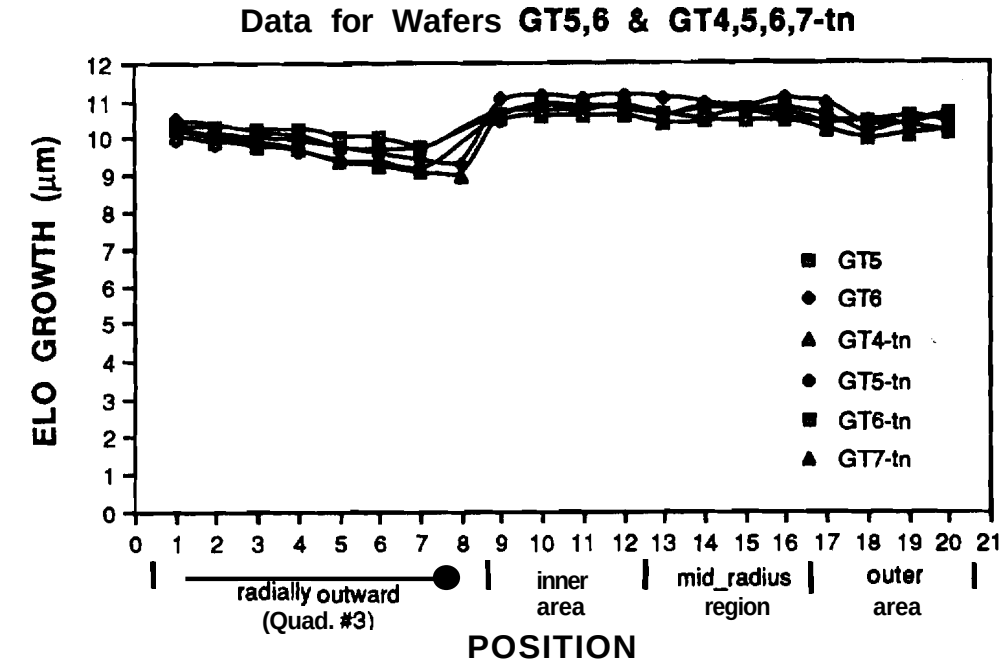


Figure 2.7. Growth profiles of the first run (1020°C).

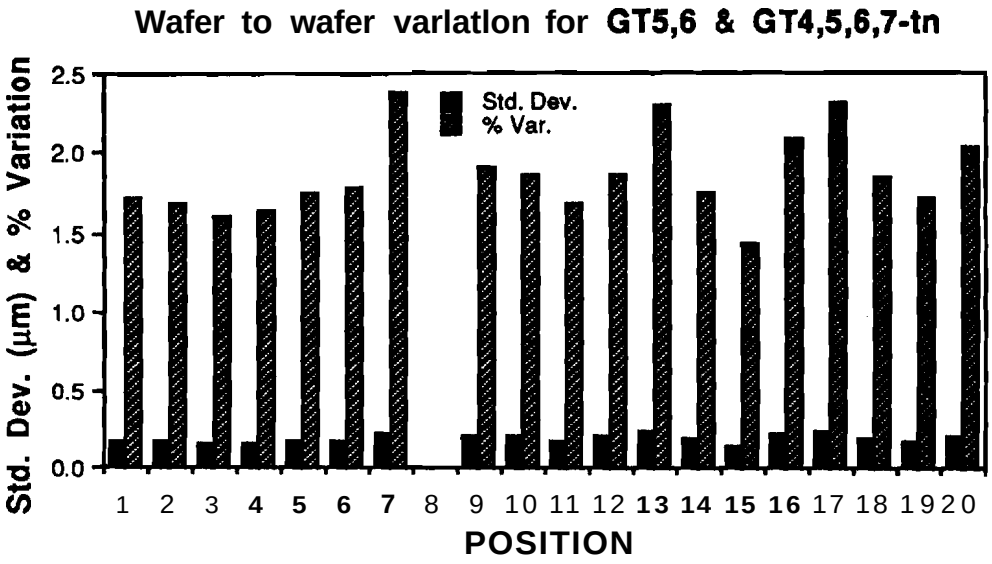


Figure 2.8. Wafer to wafer standard deviation and % variation of thickness at different test points for the first run (1020°C).

In the run of Figure 2.6, the growth was performed at 1020°C and 150 Torr. The variation of growth in a wafer is within 6% for all six wafers, the lowest being 2.9% for wafer #GT5. After examining the uniformity of MELO silicon from numerous runs at different pressures (150 Torr & 40 Torr), and at different temperatures (950°C, 970°C & 1020°C), it was concluded that less than 10% growth variation (the accepted range) across a wafer is always attainable. The growth profile in Figure 2.7 shows a decrease of growth radially outward in quadrant #3. This is merely an indication that the susceptor in the reactor has a temperature gradient, which has been verified by Ge dot melts. The same growth reduction was observed for the low temperature runs. Correction can be made to the reactor by adjusting the RF heating coils such that better uniformity may be ensured during growth.

As for the wafer to wafer variation in each run, the growth profile of each run (Figure 2.7) illustrates that the epitaxial thickness at any given position on a wafer deviates very little from that at the same position on other wafers in the same run. This can be further verified by the corresponding bar graph (Figure 2.8) that displays the standard deviation and the percent variation at any given wafer location per run. In the run of Figure 2.6, the percent variation at a specific location is less than 2.5%, whereas in the low temperature runs the variation is not as good as the higher temperature runs. The nearly constant thickness among the wafers in the same run at higher growth temperature indicates that any thickness of the diaphragm beam can be repeatedly grown in the reactor at Purdue University.

Lastly, it will be explained that the slight increase in the percent variation at a reduced growth temperature is a trade off for a better silicon quality, which is always desired in the semiconductor technology. As mentioned before, the percent variation from wafer to wafer at high temperature is slightly lower than that at lower temperature. This may be explained from a growth rate point of view. The growth rates at high temperatures are always larger and more consistent among the wafers in a run than those at low temperature runs. This is due to the increase in the reaction rate of the reactants at higher temperatures, which ultimately increases the overall growth. Thus, at low temperature, low reaction rate across the wafer results in less consistent growth rates among the wafers in a run; therefore, an increase in the percent variation from wafer to wafer. However, better quality of silicon is obtained at lower temperatures.

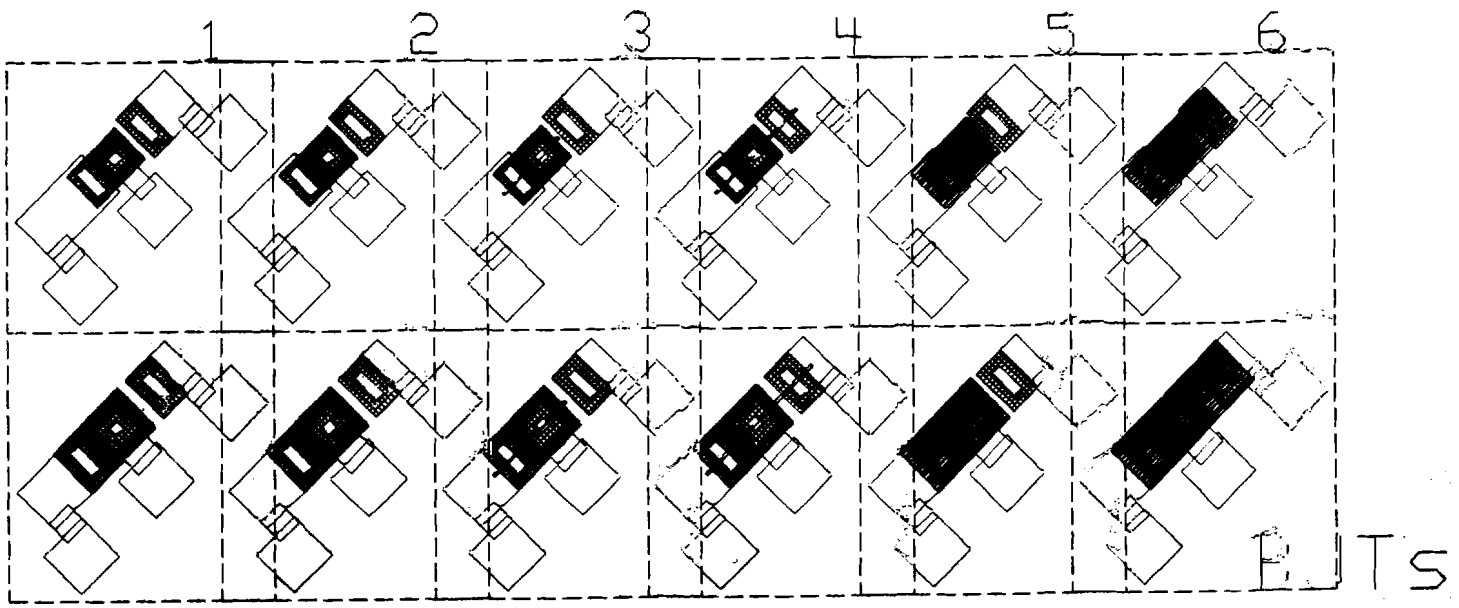
From the above discussion for four different growth runs, the following conclusions were made.

1. Temperature gradient across the susceptor is evident in all growth profiles and has been verified by Ge dot melts.
2. Repeatability of the growth in the reactor is very consistent,
   a. for within a wafer average and
   b. for at a given position average.
3. Uniformity is improved at high temperature runs.
4. Increased temperature yields higher growth rate due to the increase in the reaction rate of the reactants.
5. Lowering of the temperature has slightly increased the percent variation of the growth from wafer to wafer; however, the surface topology appears excellent.

2.3. Evaluation of MELO Silicon

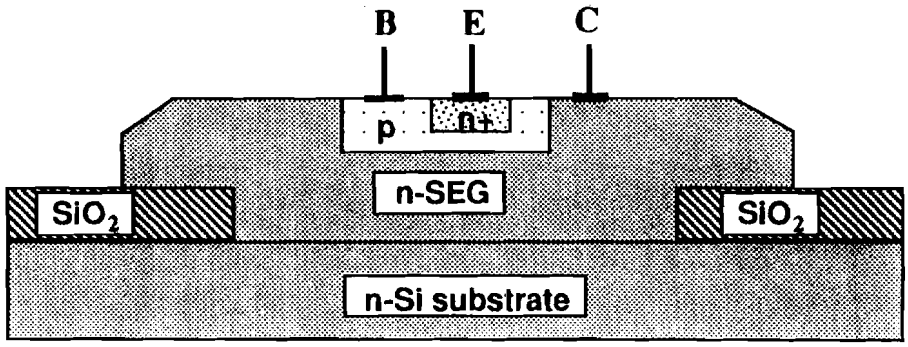
2.3.1. Device Fabrication - Bipolar Junction Transistor

As shown in Figure 2.3, when the two ELO fronts merge on the SiO_2 mask the MELO silicon film may have a voids or defects along and near the merging seam. By optimizing the silicon epitaxy condition, the voids can be minimized or eliminated. The defects induced by the merging mechanism can be physically examined by defect decorating etch such as Secco etch or Wright etch. It is, however, more intriguing to find out if those defects would play a significant role in the electronic device characteristics. In order to evaluate whether the MELO technology is suitable for electronic devices such as resistors, diodes, or transistors, it is important to build devices on the MELO film and examine the device characteristics. The testing device structures were designed to include bipolar junction transistors (BJT) which are one of the most sensitive devices to material defects. With this design, both base-to-emitter (B-E) diodes and base-to-collector (B-C) diodes were evaluated, in addition to the BJT device. By fabricating such devices on both SEG and MELO silicon, the electrical characteristics such as diode ideality factor, junction leakage current could be compared.

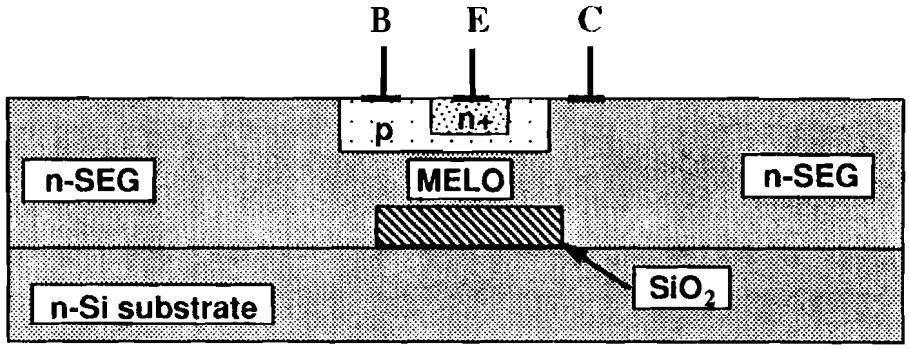


SEG device MELO-1 device MELO-m device

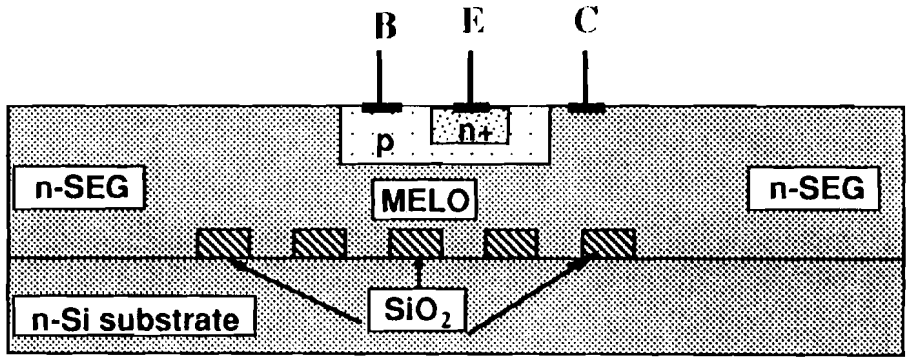
Figure 2.9. Top view of the BJT device for MELO silicon material evaluation.



(a) Device on SEC



(b) Device on MELO on Single Oxide (MELO-1)



(c) Devices on MELO *on* Many Oxide (MELO-m)

Figure 2.10. Cross section diagram of BJT devices on three different types of material. (a) SEG device, (b) MELO-1 device, (c) MELO-m device

The bipolar junction transistor layout is shown in Figure 2.9 which contains two different sizes of emitters in order to observe any perimeter effects. They arc placed in each die so that MELO silicon material can be evaluated across the wafer. The fabrication of BJT devices can be accomplished by adding only two more masking steps to the MELO accelerometer fabrication process. The additional two masking steps are base (mask #4) and emitter (mask #5) implant pattern. The full MELO accelerometer fabrication procedures, including BJT fabrication steps, are described in chapter 4.

The &vices were fabricated on three types of silicon crystal material for comparing the material quality between SEG and MELO silicon: SEG, MELO-1, and MELO-m. Figure 2.10 illustrates the cross section diagram of BJT &vice fabricated on those three types of film. SEG silicon (Figure 2.10(a)) is a single crystal grown on a large seed window (or silicon field area) selectively. Since the SEG silicon is grown far away from the SiO_2 mask, its growth is hardly affected by the SiO_2 mask. The quality of the SEG silicon can be compared to the substrate silicon and hence the devices fabricated on the SEG silicon have repeatedly shown the electrical characteristics comparable to those on the substrate silicon. Therefore, other types of the &vices can be compared to the SEG device for the evaluation of the devices as well as the material. MELO-1 (Figure 2.10(b)) represents the MELO silicon grown over a single oxide strip whereas MELO-m (Figure 2.10(c)) represents the MELO silicon grown over multiple oxide strips, here 13 oxide strips. Consequently, MELO-1 silicon has a single merging seam, and MELO-m silicon has several merging seams. The devices were fabricated on these two types of MELO silicon in order to examine the influence of the oxide strips and the corresponding merging seams above them.

The testing results of BJT devices averaged over a number of dies are summarized in Table 2.2. As mentioned earlier, the SEG devices are showing excellent electrical characteristics. The ideality factors from base-emitter and base-collector p-n junction diodes are almost unity and the reverse biased junction leakage current density from those diodes are also very low. The electrical testing results of the MELO-1 and MELO-m devices are not as good as the SEG devices. The ideality factor of the base-collector diodes are still comparable to the SEG &vices and it indicates that the material quality of the MELO silicon can become as good as the SEG silicon. Also the leakage current of all three types of devices are comparable. This indicates the MELO silicon is good enough for the majority carrier dominant devices such as piezoresistors and MOSFETs as well as diodes and BJT

devices. The measured BJT I_C vs. V_{ce} plots from three types of devices are illustrated in Figure 2.11.

Table 2.2. The testing results of BJT devices fabricated on SEG/MELO Si

material types	η (ideality factor)		leakage current (A/cm^2)		β_{peak}
	BE diode	BC diode	BC diode	BE diode	
SEG	1.01	1.00	$9.70x10^{-8}$	$5.63x10^{-6}$	95
MELO-1	1.35	1.12	$4.98x10^{-6}$	$6.25x10^{-5}$	72
MELO-m	1.23	1.11	$1.85x10^{-6}$	$1.16x10^{-5}$	~72

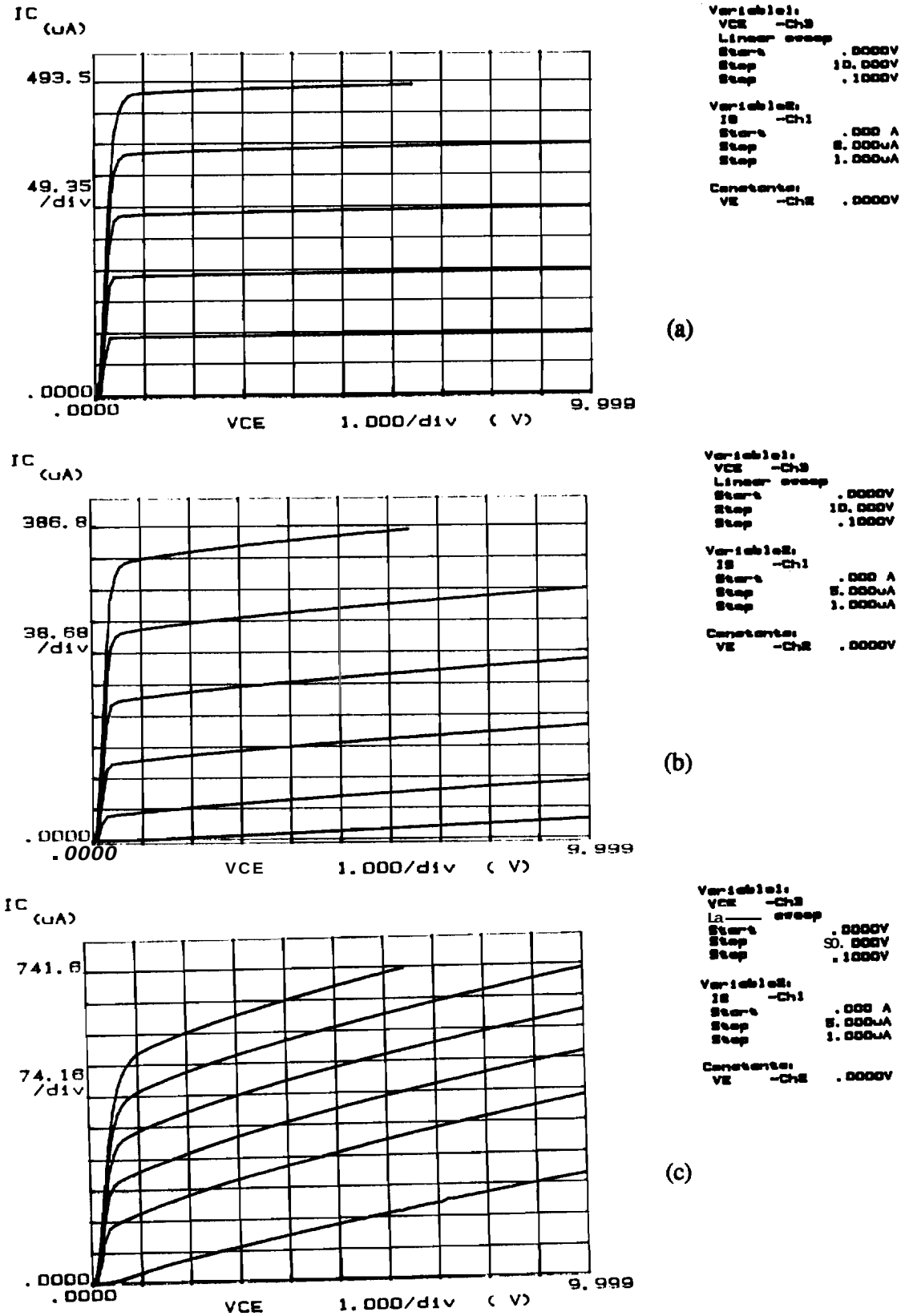


Figure 2.11. Typical I_c vs. V_{ce} plots from BJT device of Figure 2.11. (a) SEG device (b) MELO-1 device (c) MELO-m device.

2.3.2. Crystallographic Defect Etch

The conventional Secco defect etch (one part of 0.15 molar solution of $K_2Cr_2O_7$ plus 2 parts of HF) has been executed on MELO silicon for examining crystallographic defects. Preliminary results show that oval shaped etch pits occurred around the merging seam of the MELO silicon. When two advancing ELO fronts merge at the middle of the oxide island, they produce a thermomechanical stress along the merging seam and thereby induce dislocation faults. Also the temperature gradient in the reactor and the difference of thermal expansion coefficient between silicon and silicon dioxide (SiO_2) may play a role in inducing these dislocation faults.

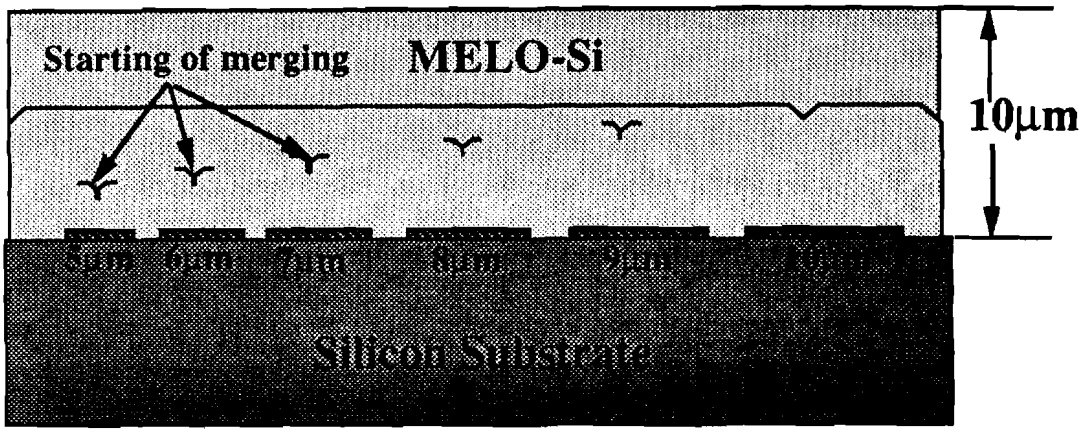
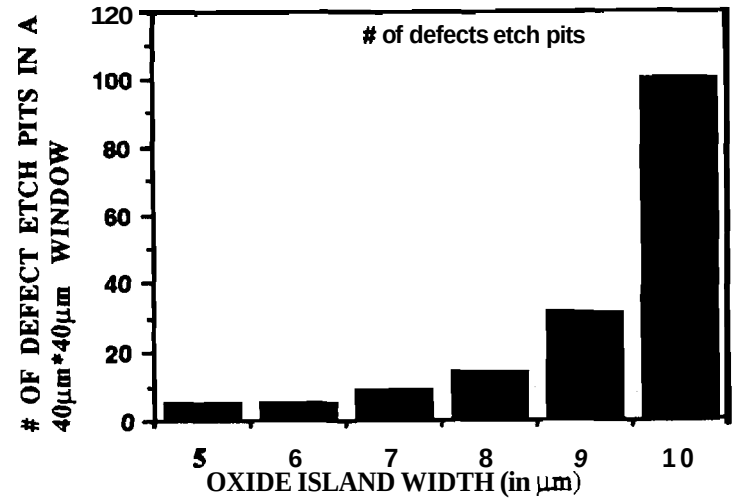


Figure 2.12. Merging on Oxide islands with different width in test mask.

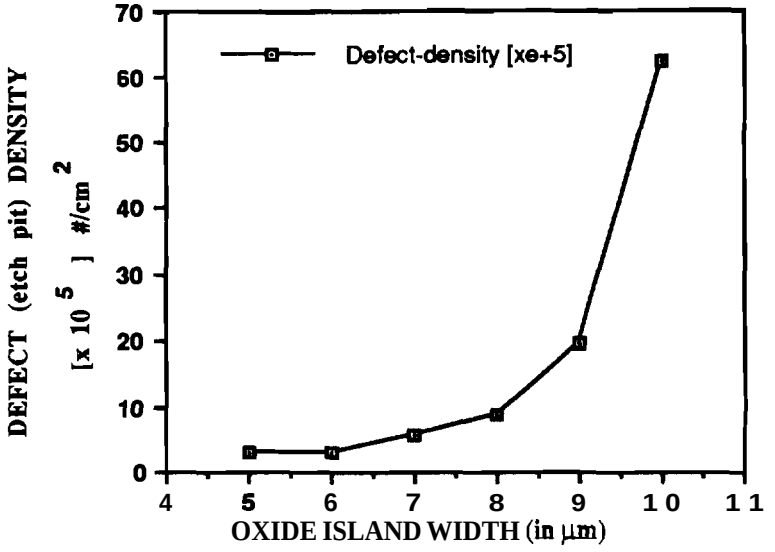
The test mask has different oxide widths starting from 5pm up to 10μm as shown in Figure 2.12. MELO silicon was grown over these oxide islands on a wafer in a same run. As illustrated in Figure 2.12 merging will occur on the 5μm wide oxide island first and finally on the 10μm wide strips. Figure 2.13 shows the variation number of etch pits and the etch pit densities which resulted from a 90 second Secco defect etch on MELO silicon grown on different width oxide islands. Both the number of defects and the defect densities are increasing with the wider oxide islands (Figure 2.13) while having the identical MELO silicon. Since the MELO silicon forms on narrower oxide islands earlier than on wider oxide islands, the merging seam area on narrow oxide islands is covered by thicker single crystal silicon. While the MELO silicon is forming on wider silicon islands,

the defects around the merging seam on the narrower oxide islands gets healed during the subsequent film growth. Therefore, fewer defects propagate to the top of the MELO silicon where the Secco etch has decorated the defects.

In the accelerometer design, piezoresistors are fabricated on the top 1 μm out of a 10 μm thick MELO silicon film grown over a group of 5 μm wide oxide islands. As shown in Figure 2.13, both the number of defects and the defect densities over 5 μm wide oxide islands are minimum and are within a reasonable range. The test results of the p-n junction leakage current densities from the diodes fabricated on the 10 μm thick MELO film showed reasonable leakage. In fact it is much lower than the leakage data provided to us from Delco for their resistor on much thicker (~25μm) epitaxial silicon on P^+ layer. Therefore, for thick MELO film the dislocation faults resulting from merging are not playing a critical role in device performance. However for thinner MELO film a further research to reduce defect counts is recommended.



(a)



(b)

Figure 2.13. Results of Secco etching. (a) Graph showing # of etch pits vs. width of oxide islands. (b) Graph showing the variation of defect density with the width of the oxide island.

2.4. Seed Window Preparation Using Reactive Ion Etch (RIE)

The epitaxial lateral overgrowth (ELO) technique uses single-crystal silicon grown selectively out of a seed hole (SEG) etched in an oxide mask layer. The seed hole window opening plays a crucial role in ensuring better quality selective epitaxial silicon. Usually an oxide with a straight edge and a uniform side-wall results in a fewer number of stacking faults and thereby ensures better merging of the two advancing ELO fronts. Opening of the seed hole by wet etching results in widening of the masked line width by undercutting the photoresist mask. Especially for thicker oxides, this undercutting becomes considerable and the oxide side walls become slanted. For this reason an attempt was ma& to open the seed windows with reactive ion etching (RIE) which is highly selective to the removal of oxide as compared with silicon. In addition RIE should also etch the oxide anisotropically to produce the controlled vertical side walls.

Reactive ion etching is becoming increasingly important in microelectronic fabrication because of its ability to limit the dimensional changes to a minimum while patterning. The development of a plasma process is a somewhat complex due to the number of variables (type of reactor, type of gases, pressure, power, flow etc,) which may potentially influence the etching behavior. Usually the R E process involves the use of a glow discharge to generate reactive species from relatively inert molecular gases in a controlled pressure etching chamber. These reactive species combine chemically with certain solid materials to form volatile compounds which are then removed by the vacuum pumping system. For the experiments at Purdue University a Drytek DRIE-100 13.56MHz parallel plate plasma etcher was used. Figure 2.14 shows a schematic of the basic system. This system was a generous gift from Delco Electronics.

This RIE system is equiped with six individual etch platforms, each with its own tuning network and gas distribution so that up to six wafers can be etched simultaneously at the same etch rate. Gas flow, system pressure, and the etch times are all electronically controlled to provide better uniformity. The wafers are also water cooled and are kept at lower temperatures even with higher power densities.

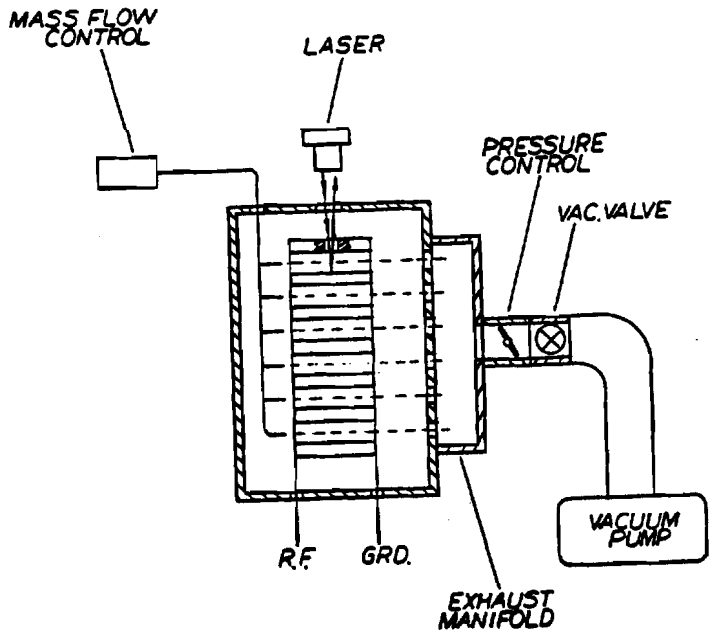


Figure 2.14 Schematic of the Drytek DRIE-100 **RIE** system

Direct exposure of the silicon substrate to the reactive processes was avoided by keeping less than 1000 **Å** of **oxide** at the base of the seed hole cavities. **Therefore** the usual lattice damage introduced into the silicon substrate from bombarding action and plasma species related impurities trapped in the silicon lattice were limited. After the RIE the remaining oxide was removed by a short BHF dip. This short wet etching didn't have a chance to make the oxide side-walls slant considerably. A typical etch profile (etch depths before and after BHF dip with the photoresists removed) is shown in the Figure 2.15. The figure clearly shows that the short **BHF** deep is **removing** the **nonuniformity** that resulted from the RIE.

Table 2.3 lists the etch gases used in these experiments and their **corresponding** etch rates for silicon, SiO_2, and photoresist. The etch rates were estimated by measuring the etch depths using a Tencor alpha-step **profilometer.** It is clear that Freon 116 is having the highest selectivity to SiO_2 over silicon. Whereas due to the presence of **Cl** in Freon 115 it is etching more silicon than oxide. In case of the photoresist AZ 1350 both etchants, even at different etching conditions, have shown the same selectively (**~1:1)** to oxide. It is believed that the fluorocarbon ions from the Freon 116 plasma reacts with SiO_2 during the ion bombardment and forms volatile SiF_4 while suppressing the etching of silicon by **forming** a carbon coating.

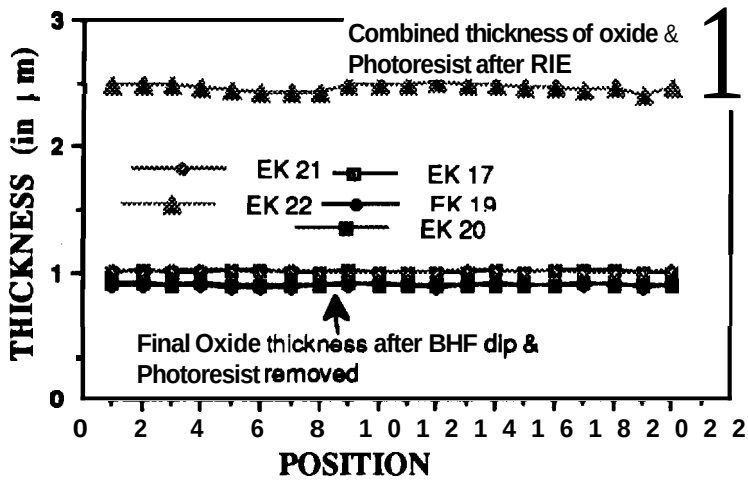


Figure 2.15. A typical etch profile for RIE. The upper curve shows the combined thickness of the oxide and the photoresist. The lower curves shows the final oxide thickness after the BHF dip and the photoresist removed.

TABLE 2.3

DIFFERENT RIE GASES AND THEIR ETCH RATES

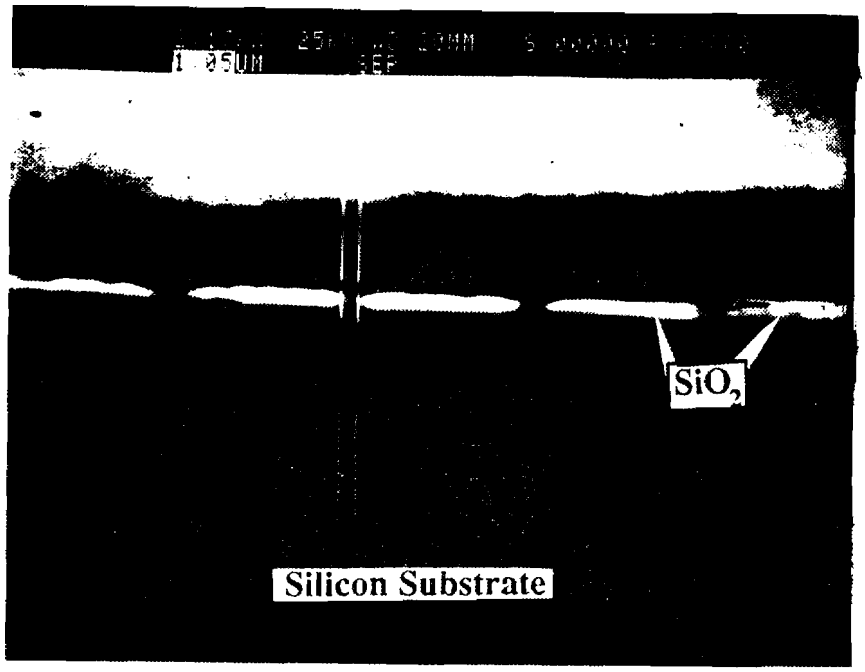
ETCH GAS POWER (W)	PRESSURER (mTorr)	GAS FLOW RATES Freon116 (SCCM)	Freon 115 (SCCM)	ETCH RATES (Å/min.) Silicon	Oxide	AZ 1350
1000	495	150	---	??	100	100
1000	300	150	---	10-20	50	48
750	ALAP	----	95	350	100	100
500	ALAP	----	95	100	50	50

2.4.1. RIE with Freon 116 (C_2F_6)

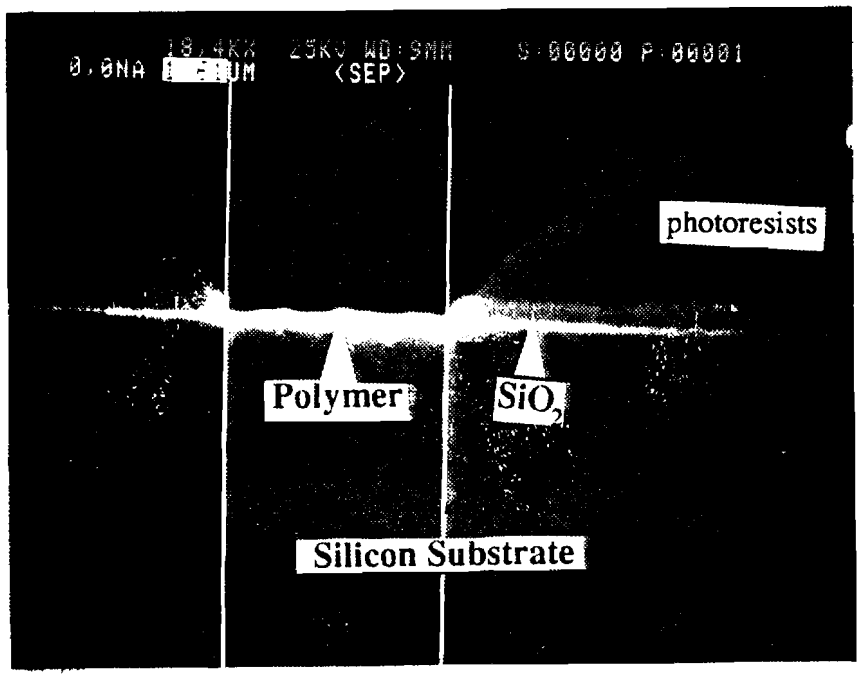
In the DRIE-100 etcher the exposure of Freon 116 plasma to silicon resulted in a residue (mostly florine polymer) on the whole wafer when the etching was performed at a relatively high pressure (495mT). Even a slight exposure of silicon at the wafer edges resulted in this residue deposition on both silicon and oxide and thereby stopped the oxide etching. Higher temperature annealing or plasma ashing didn't remove the polymer although they were the two suggested remedies published in the literature.

Figure 2.16(a) shows a SEM photograph of the cross section of the polymer deposited oxide islands. In Figure 2.16(b) a more magnified view of the residue on the oxide surface at the seed holes is shown. Here it clearly shows the deposited residue on the unetched base oxide in the seed hole. This residue is only etched in BHF at a very slow rate. By the time all the polymers were removed the oxide islands were also etched away in BHF.

Another interesting observation occurred when wafers with more oxide to be etched were loaded in the etch chamber; the residue deposition started even earlier (within 10 minutes of etching). This suggests a possible link between the deposition of the polymer and the loading of the etcher. Reduction of the operating pressure has shown gradual improvement in preventing the polymer deposition. But at a lower pressure it was very difficult to have a sustained plasma. The lowest possible pressure for uniform sustained plasma in the RIE system was achieved at 300mT without changing the operating power (1000 W) and the gas flow (150 SCCM) . We believe the reduced pressure in the chamber has established a more ion-bombardment dominant environment during the etching and thereby the reactive compounds resulted from the chemical reaction are easily pulled away from the oxide surfaces. The sacrifice made at this new setting is the etch rate, which is now half of the previous value (down to 50 Å/min) (Table 2.3.).



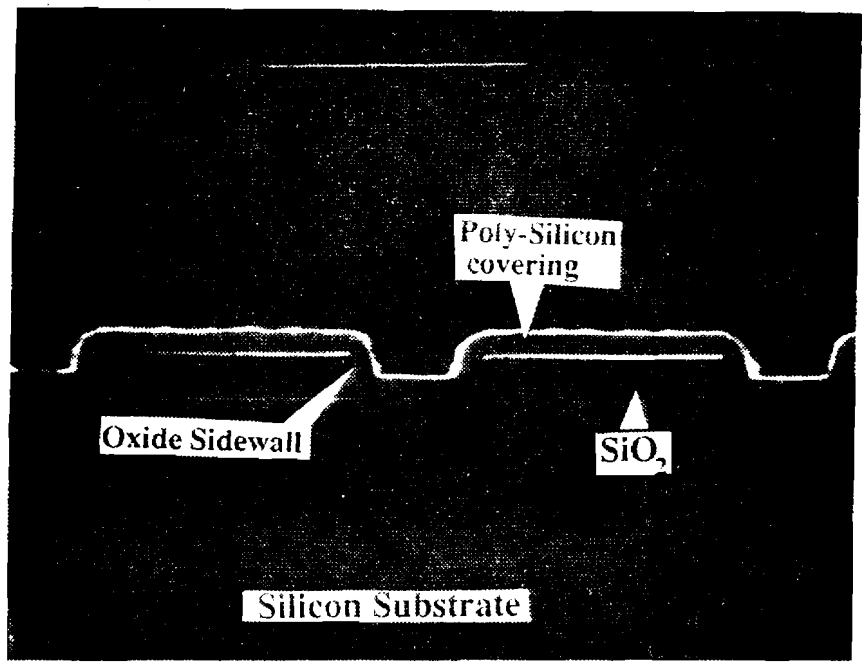
(a)



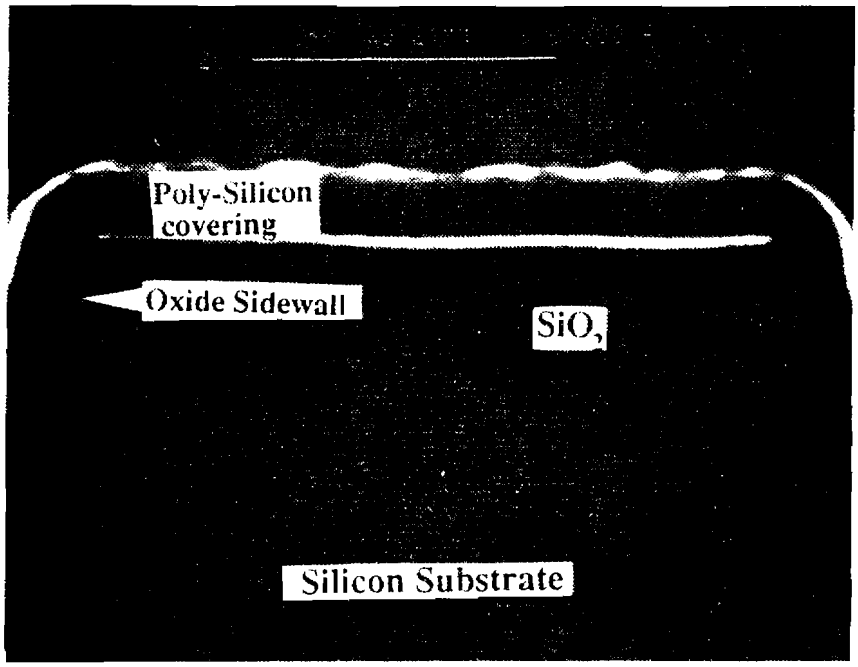
(b)

Figure 2.16. Polymer deposition on wafer while etching in Freon 116 plasma at 495mT and 1000 W. (a) SEM photograph of polymer on the seed holes .(b) SEM photograph showing the polymer in the seed hole in a magnified view.

Figure 2.17(a) shows an SEM photograph of the oxide side walls which were etched by Freon 116 at the new setting (Pr=300 mT, P=1000 W, Flow= 150 sccm). To avoid charging on the insulator surface while taking the SEM picture a thin layer of poly-silicon was deposited on the etched seed holes and the oxides were removed from the cross-section by a HF wet etch. A closer view is presented in Figure 2.17(b). The vertical wall resulted in this anisotropic etching is close to 85 degrees and the oxide thickness is about 1 μm. During the 200 minutes of etching no polymer deposition was noticed on any parts of the wafer. The etching was stopped while there was about 600 Å of oxide left at the base of the seed holes. This left-over thin oxide was removed in a short BHF dip. As shown in Figure 2.17, this etching (BHF dip) didn't make the oxide side walls slant.



(a)



(b)

Figure 2.17. RIE etching of oxide in Freon 116 at 1000 W and 300mT. (a) SEM photograph showing the vertical side walls of the oxide after etching (a thin poly-silicon layer is deposited for better clarity of the SEM). (b) A more closer view shown in the SEM photograph.

2.4.2. RIE with Freon 115 (C_2ClF_5)

While Freon 116 was initially selected for RIE due to its highly selective etching characteristics on the oxide over silicon, Freon 115 was also examined as an alternative. Since it was planned to stop the etching by keeping less than 1000 Å of oxide in the seed holes it was not necessary to worry about the etching of the silicon substrate. One of the advantages with Freon 115 was that the deposition of polymer on the wafer never occurred regardless of the etching pressure.

In achieving the vertical wall SiO_2 of the seed window for silicon epitaxy, the photoresist profile control became very important. The reactive ion etching is often used for making a vertical wall structure in the substrate. However, if the mask material profile is not well controlled, then it becomes difficult to achieve a vertical wall because the RIE etches the masking material and the substrate at the same time. Therefore, when the masking material profile has a slanted slope, the substrate will be etched following the slanted slope. The SEM photograph shown in Figure 2.18 is an example of the slanted side wall produced by RIE because of the slanted photoresist sidewall profile. A thin polysilicon layer was deposited on the etched surface and the oxide was removed to increase the clarity of the SEM photograph.

In order to control the photoresist profile, the humidity and temperature should be carefully controlled When the AZ1350J-SF positive photoresist was spun at 4000 rpm for 30 sec. followed by 90 'C soft-bake for 30min., the photoresist profile after patterning became slanted as shown in Figure 2.16 (b) and resulted in the slanted SiO_2 sidewall after RIE with Fr115. The resist thinning at the oxide edge has resulted in an oxide side-wall slant similar to wet etching. However, after optimizing the soft-bake temperature and the time to at 110 'C for 30min., the SiO_2 sidewall profile improved to 75 to 80'. This is clearly shown in the SEM photograph in Figure 2.19. The photoresist profile is close to vertical and the SiO_2 sidewall also follows the same vertical line. The etch rate of SiO_2 is about 100Å/min which is about twice faster than Fr116 and hence less time will be required to etch the same oxide thickness.

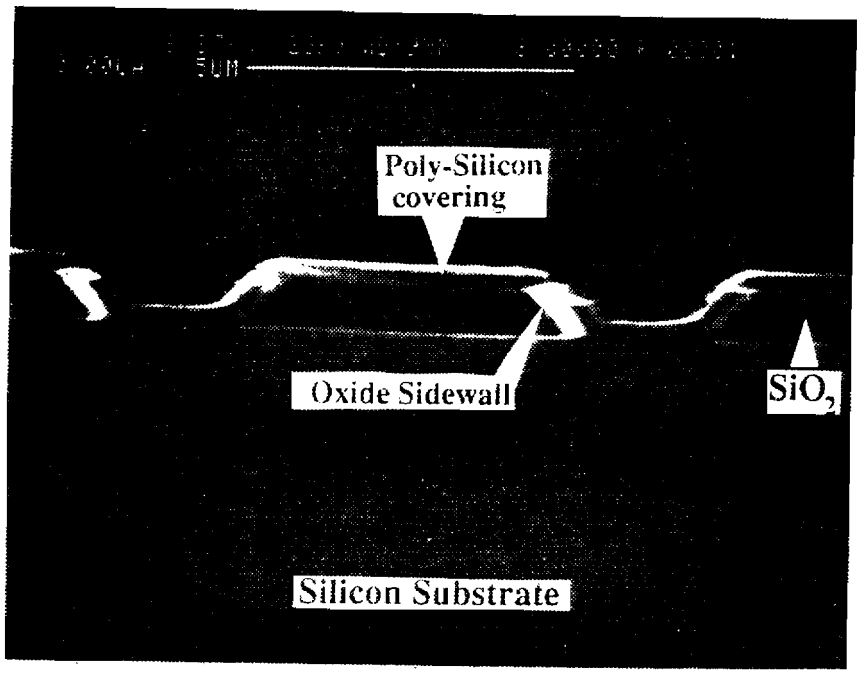


Figure 2.18. SEM photograph showing RIE etched oxide side walls in Freon 115 with normal soft baking at 90" C. (a thin poly-silicon is deposited on top of the etched seed holes for better SEM picture.).

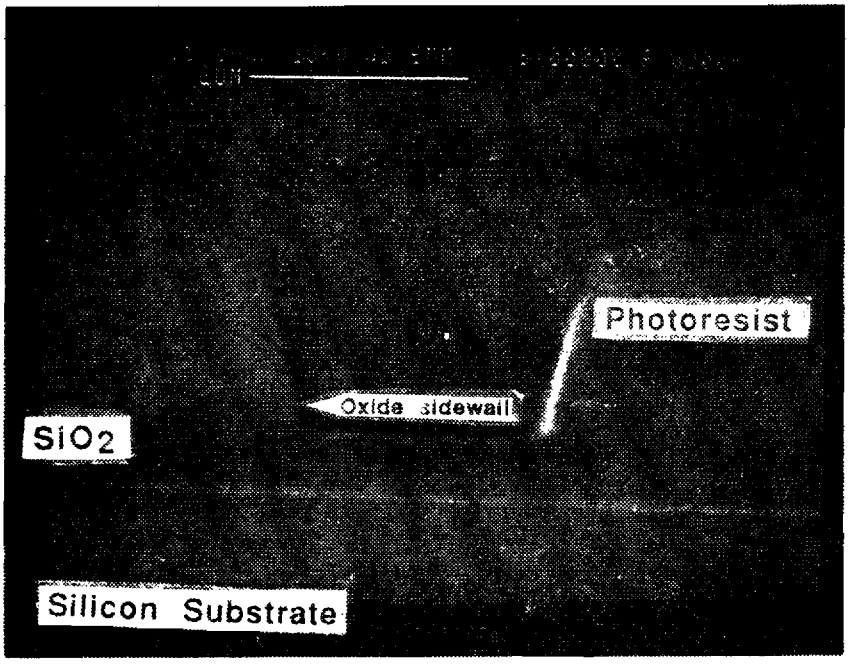


Figure 2.19. SEM photograph showing virtually vertical oxide sidewalls (75") by RIE with Freon 115 with better photoresist profile by soft baking at 110" C.

III. Application of MELO Silicon

3.1. Single Crystal Silicon Membrane Formation

Due to the fact that the aspect ratio (ratio of lateral growth over vertical growth) of ELO silicon is inherently close to unity, the minimum thickness of MELO silicon to form a flat small area silicon diaphragm needs to be a little greater than half of the SiO_2 width while the length can be of any size. Therefore, with a single SiO_2 island (Figure 1.1), the diaphragm is limited to a very narrow dimension of 1 μm to 20 μm of almost any length and thickness. For a wider and thin membrane formation with a single SiO_2 island, quite a long deposition time silicon epitaxy and subsequent planarization step are required That is not very economical and will not be acceptable from the manufacturer's point of view.

Therefore, for reasonably wide (50 to 500μm) and thin (10 to 25 pm) diaphragms, a modified membrane structure needs to be employed. A wide and thin diaphragm can be constructed by MELO silicon on several oxide strips, between which several narrow seed holes are formed, combined with V-groove self-limiting etch-stop as shown in Figure 2.1(d). The V-groove etch-stop technique makes use of the different etch rates &pending on the crystal orientation . The etching should then be limited by the oxide strips and the slowly etched crystallographic planes in the original seed windows between the oxide strips. When the photo mask is parallel and perpendicular with the <100> directions the etch is limited by the {110} planes since the silicon crystal etch rate is in the order of (100) > (110) > (111). The thickness of the diaphragm will be still controlled by the MELO growth rate which is approximately 0.1 μm/min.

The thickness variation from the crystallographic etch-stop in the exposed seed windows between the oxide islands needs to be minimized in order to optimize the uniformity of the diaphragm. Minimizing the number of the seed windows is one way to reduce the variation of the diaphragm thickness. Another way to improve the uniformity of the diaphragm is to minimize the seed windows between the oxides since the V-groove depth is proportional to the seed window width. This is limited by the photolithography limit and the minimum seed window. To work comfortably at Purdue University Solid State Laboratory, a range of 2 μm was selected.

Fabrication of the thin and wide diaphragm starts with an n-type (100) silicon wafer of 10-15 ohm-cm that was thermally oxidized and then 2 μm wide rectangular seed holes were patterned into the oxide in the <100> directions. The thickness of the SiO_2 islands was about 1 μm and their other dimensions werc 5 μm wide and 1000 μm long. Selective Epitaxial Growth (SEG) of silicon was used to fill seed holes with single crystal silicon without any nucleation of polycrystalline silicon on the etch-stop oxide. As growth proceeds, single crystal silicon is grown out of seed holes both vertically and laterally across the SiO_2 to form an MELO silicon film. Figure. 3.1(a) shows the structure of MELO formation on the oxide islands with a flat top surface of the MELO film. After merging of the ELO, the growth was terminated once a flat top surface was obtained. The flat top MELO silicon layer over the 5 μm wide oxide islands was obtained in 80 min at 1020°C and was about 9 μm thick.

After a flat top MELO silicon was obtained, both sides of the wafer were protected by depositing layers of silicon nitride and oxide, Silicon nitride and oxide were deposited by low temperature plasma enhanced chemical vapor deposition (PECVD) for protection during the long anisotropic back-side etching. PECVD was employed instead of LPCVD technique to avoid a high temperature process for any devices that had been fabricated on the same wafer beforehand. Silicon nimde is considered to be stronger mechanically than SiO_2 and shows superior masking characteristics to wet etches. The remaining step is the formation of MELO silicon diaphragm by anisotropic wet etching through a window in the backside of the wafer. Etching patterns were photolithographically defined on the back of the wafer and the nitride etched. The anisotropic silicon etch was performed with a KOH-based etch solution (or ethylenediamine-based solution (EDP) can be used). Etching continued until it reaches the bottom side of the SiO_2 islands which act as an etch-stop layer. In the narrow seed hole regions, the etch stopped by forming V-grooves along the slowly etched cystalographic planes as illustrated in Figure 3.1(b). After the single crystal silicon diaphragm forms, the SiO_2 islands and the silicon nimde can be removed to release any compressive or tensile stress on the MELO.

As a demonstration example of the technology and its thickness control capability, several wafers were fabricated with a MELO silicon layer 9 μm thick over 5 μm wide oxide islands. Neither voids nor visible crystal defects were observed at the merging plane in the middle of the oxide islands, implying good crystal merging of the MELO silicon. Figure 3.2 shows a scanning electron microscopy (SEM) photograph of a top view and a cross section of the SEG (left side) and MELO silicon over oxide islands. Note the very smooth

top surface. The growth topology of the SEG and MELO silicon did not show any thickness difference under Nomarski illumination or by profilometer measurements.

Figure 3.3 illustrates a cross section of the 250 μm x 1000 μm MELO silicon diaphragm structure achieved after etching from the backside in a KOH-based solution at a constant temperature of 80 ± 1°C. The etch solution was a mixture of 47 g of KOH, 127 ml of DI water, and 39 ml of n-Propanol whose etch rate was about 1 μm/min for silicon and 30 Å/min for SiO_2.

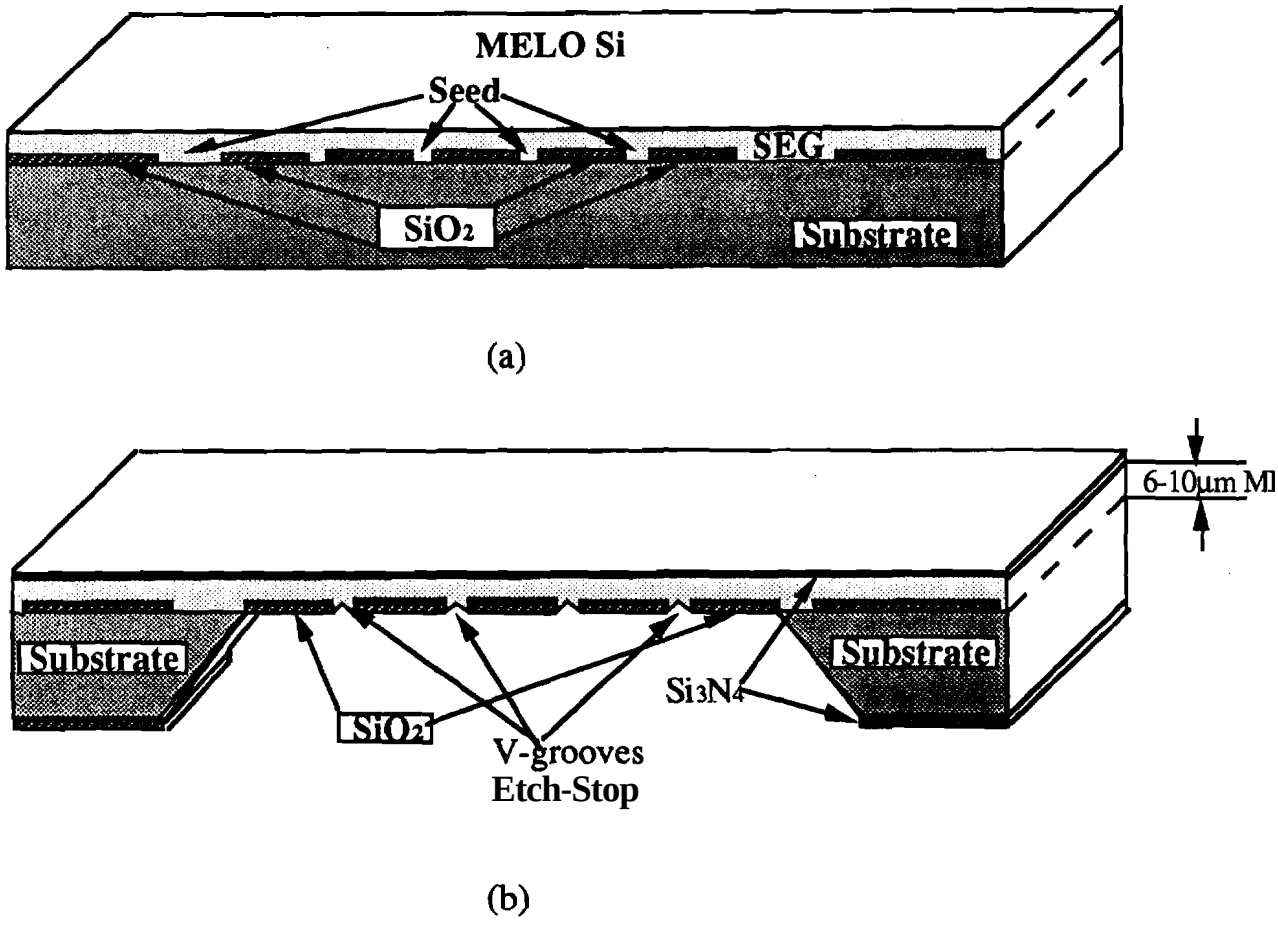
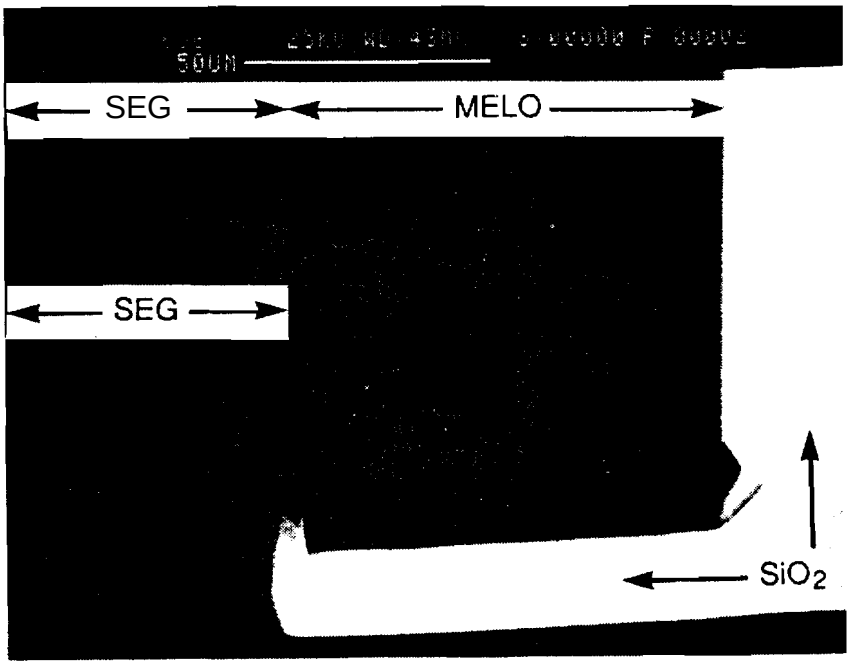
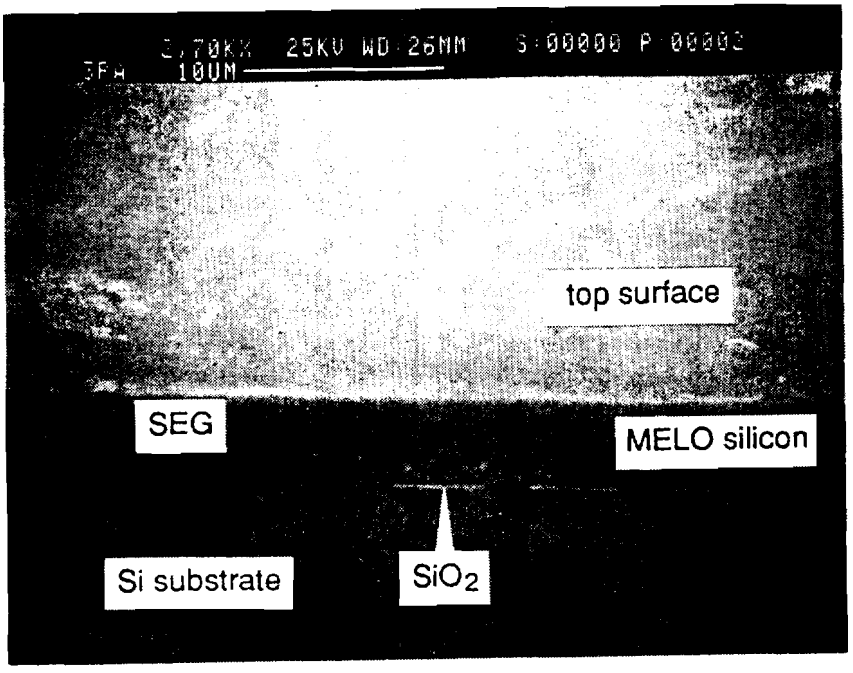


Figure 3.1. Large Area single crystal silicon diaphragms. (a) Flat top MELO silicon with oxide stripes and seed holes (b) MELO silicon diaphragm after back-side etch.



(a)



(b)

Figure 3.2. SEM photograph of SEG and MELO silicon (a) top view (b) cross section.

The measured MELO film thickness was 9 μm with a standard deviation of 0.5μm over the entire 3" wafer, indicating excellent thickness control. Figure 3.3 shows the V-groove etch-stops on the bottom of the diaphragm. The formation of ≤2 μm deep etch-stop V-grooves took place between each of the original oxide islands since the oxide seed windows were wider than 2 μm, due to wet chemical etching. However, their depth can be minimized by reducing the seed hole width to ≤1μm and by etching the seed holes with reactive ion etching (RIE). Any damage possible from the RIE can be prevented by stopping the RIE just prior to the bottom SiO_2/Si interface and removing the residual oxide by wet etching prior to SEG. The effect of the V-grooves on the stress distribution for the top-side piezoresistors is small if their depth is less than 10% of the total diaphragm thickness. The diaphragm thickness presented here can be made thinner by using narrower SiO_2 islands.

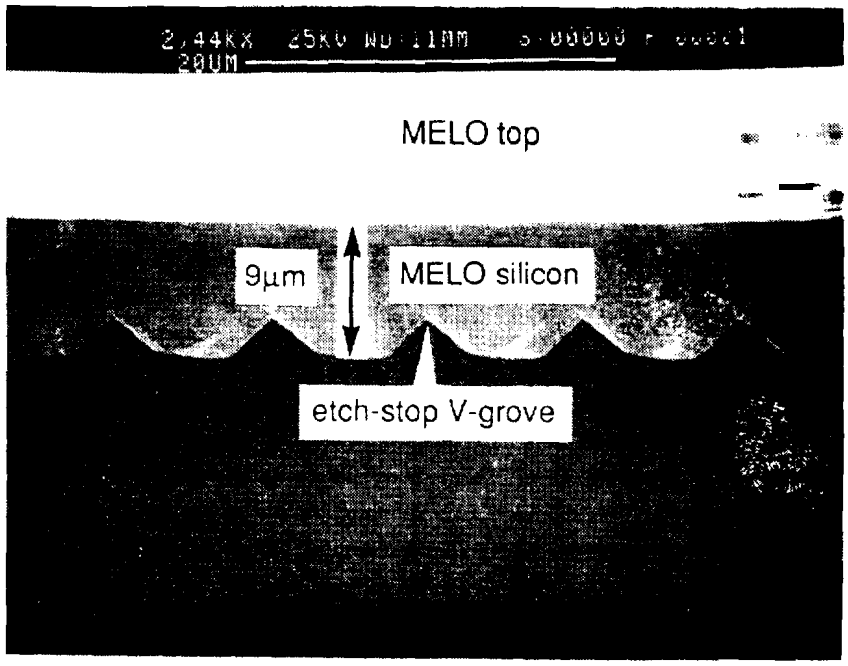


Figure 3.3. SEM photograph of cross section and top of MELO silicon membrane.

3.1.1. Controlling the V-Groove Depth into The Membrane

The relatively wide and thin single crystal silicon diaphragms are formed by exploiting the advantages of merging of advancing ELO fronts and the formation of V-groove self limiting etch-stop during the back side etch. Controllability of the depth of the V-groove etch stops is essential when forming the beams from backside etching. Figure 3.4 illustrates two cases where the V-groove is terminated. Two factors are considered when controlling the V-groove etch depth; interfacial bond strength at the SEG/SiO_2 interface and the SEG seed hole width. In the first case, a weak bond at the SEG/SiO_2 interface will increase the etch rate of silicon around the oxide in the anisotropic KOH etchant and not stop at bottom edge of the oxide. Therefore the depth of the V-groove etch stop will increase. In the second case, a large seed hole defines the opening size of the V-groove and, therefore, the depth of the etch stop. Reduction of the etched V-grooves can be accomplished by strengthening the interfacial bond and by tightening the width of the seed hole.

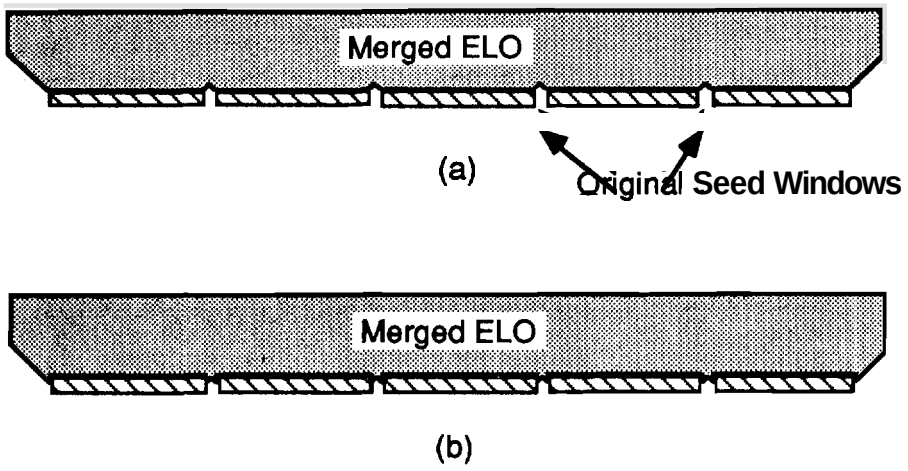


Figure 3.4. A wide thin diaphragm formation using MELO silicon combined with V-groove self-limiting etch stop: (a) with normal MELO silicon; (b) with the improved SEG/SiO_2 interface.

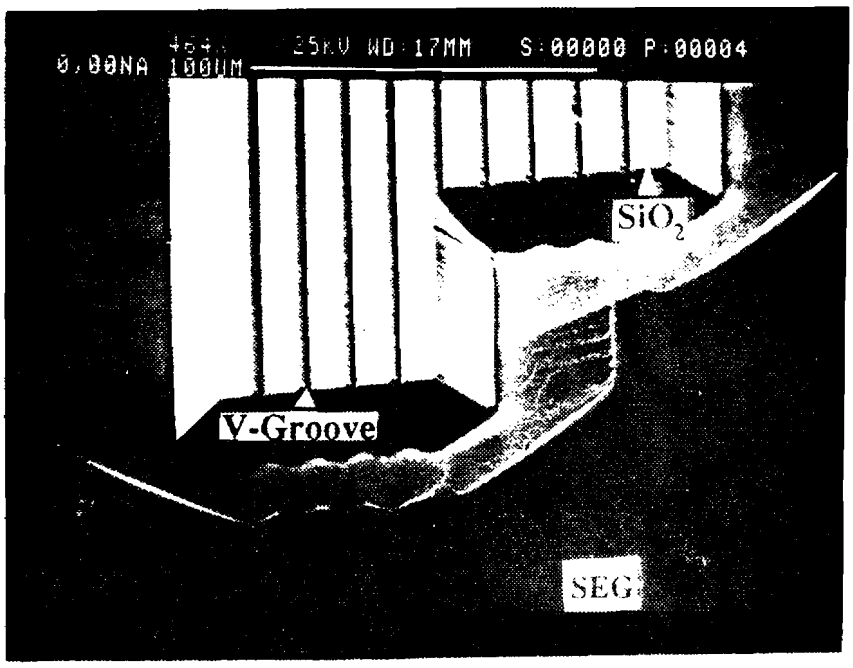
An attempt was made to minimize the effects of the V-grooves on the topology of the beam. First, to limit the depth of the V-grooves into the membrane we need to ensure a stronger bonding between the SEG silicon and the oxide sidewall so that while etching we can expose the etch limiting <110> planes earlier along the oxide edges. Secondly, since the V-groove depth is proportional to the width of the seed window, a reasonably narrow (2μm) seed windows were selected.

SEG/SiO_2 interface has been investigated due to the large interfacial leakage current observed in the SEG/ELO IC fabrication. The increase in the interfacial states is a result of the weak atomic bonding formed between the SEG silicon and the oxide wall. Evidence of the weak bonding includes the enhancement in the impurity diffusion down the sidewall and the silicon etch rate increases along the SEG/SiO_2 side walls. Possible explanation for the existence of the weak bond can be based on the following reaction, occurring at the interface during the epitaxial growth.

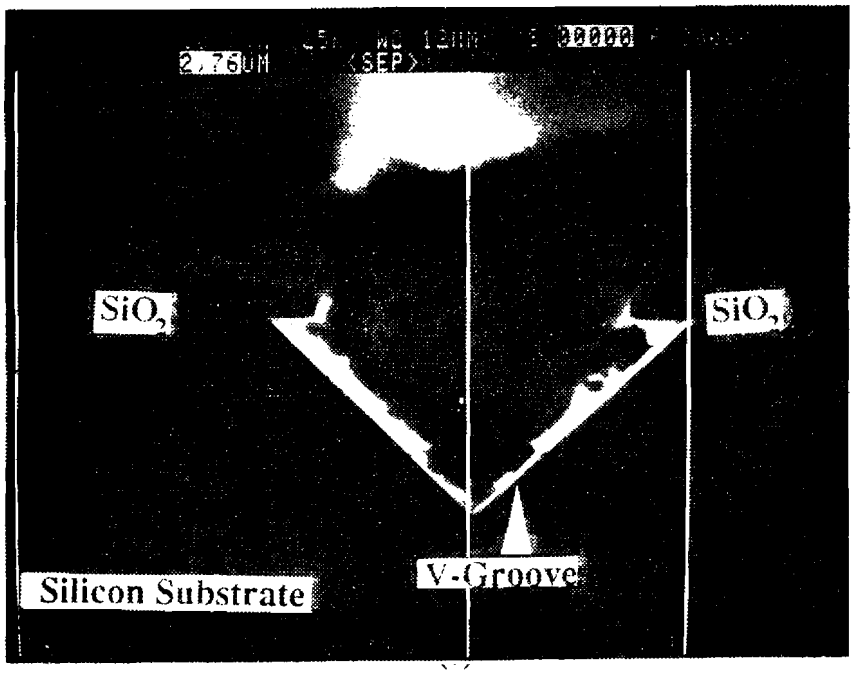
$$SiO_2 + Si \dashrightarrow 2\,SiO\,(g)$$

This reaction etches away both the silicon atoms and the oxide atoms at the interface, which, in effect, leaves a sheet of atomic voids and therefore results in a weak bonding from incomplete bond formation. Figure 3.5(a) shows the silicon near the SiO_2 strips etched faster, hence deeper than other parts of the SEG. Figure 3.5(b) shows how this causes the undercut of the SiO_2 and therefore deeper V-grooves.

Recent articles have stated that the interface shows improvement after a post epitaxial oxidation treatment (PEOX). This indirectly implies that the interface can be healed by normal post-epitaxial re-oxidation. During the re-oxidation, the interface becomes oxygen-rich and close to a thermally oxidized silicon surface which typically shows complete and strong bonding with few interface states. Taking advantage of this improvement, the PEOX process can be included into the normal ELO/MELO film process without further complexity.



(a)

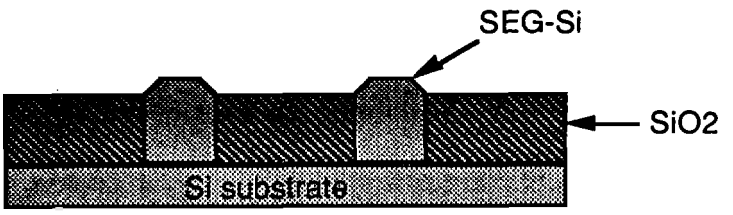


(b)

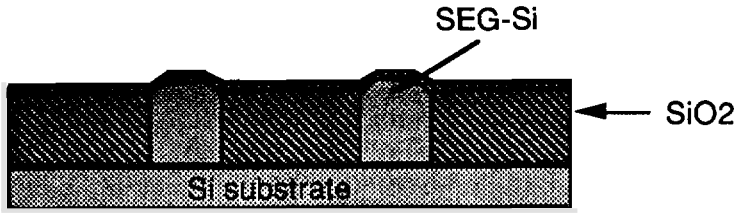
Figure 3.5 KOH etching of MELO to from V-grooves (a) SEM photograph showing enhancement of etching of silicon near silicon /oxide interface (b) SEM photograph showing the cross-section of the v-grooves having considerable amount of undercutting.

To incorporate this PEOX process into the SEG/ELO and MELO process the following approach illustrated in Figure 3.6, was attempted. Seed holes were patterned by wet etch followed by SEG growth. The duration of EPI growth was set such that the SEG coming out of the seed hole just begins to spread laterally over the oxide [Figure 3.6(a)]. Then, a layer of thermal oxide was grown on the SEG/ELO [Figure 3.6(b)]. At this step, the oxygen molecules will diffuse down the SEG/SiO_2 interface, fill the atomic voids created by the above mentioned reaction, and at the same time, completing the interfacial bonds. The thermal oxide was removed by BHF and then the ELO islands were planarized by chemical mechanical polishing (CMP) to remove any planes other than the <100> exposed on the top surface of the remaining SEG inside the seed hole [Figure 3.6(c)]. Finally MELO was grown from these post epitaxial oxidation treated seed holes [Figure 3.6(d)] To investigate the effect of PEOX treatment on limiting the V-groove depth while etching, the wafer was put into KOH etchant for a short period of time after removing the thermal oxide from the top of the ELO islands. Finally the wafer cross section was examined under SEM to investigate whether there was an early exposure of the etch limiting <110> planes at the sidewall of the oxide islands.

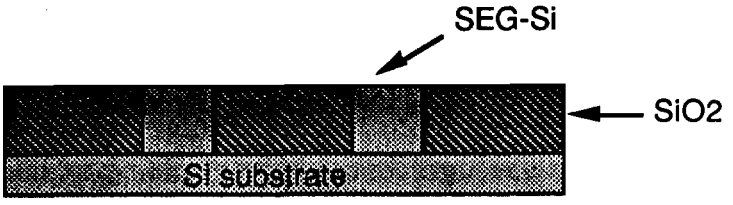
Thicker oxide was chosen so that the etch can be stopped while the silicon is still left in the oxide step of the seed hole. Since the etch rate of silicon in KOH is about 1μm/min., it was very difficult to stop the etch so that silicon was left in the oxide step. When the oxide side wall is slanted either by wet etch or RIE, early exposure of the etch limiting <110> planes at the side wall of the oxide step was not noticed even though the SEG/ELO grown from these seed holes were subjected to PEOX treatment [Figure 3.7(a)]. Even a 60 second KOH etching has resulted in a small amount of undercutting [Figure 3.7(a)]. However the etching characteristics of silicon near the oxide interface showed considerable improvement. As shown in Figure 3.7(b), the equal etch of both SEG silicon away from oxide and SEG silicon near the oxide strips was observed. This indicates that the SEG/oxide bonding at the interface has been improved by this PEOX process.



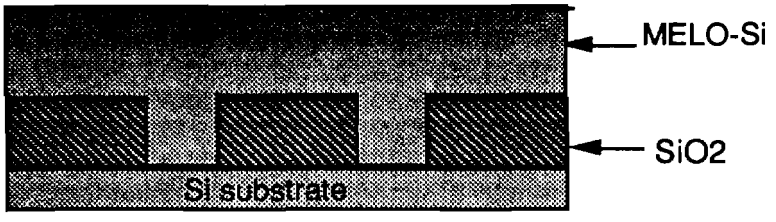
(a) SEG/ELO growth to top surface of oxide islands



(b) Oxidation to strength SEG-Si/SiO2 side walls.

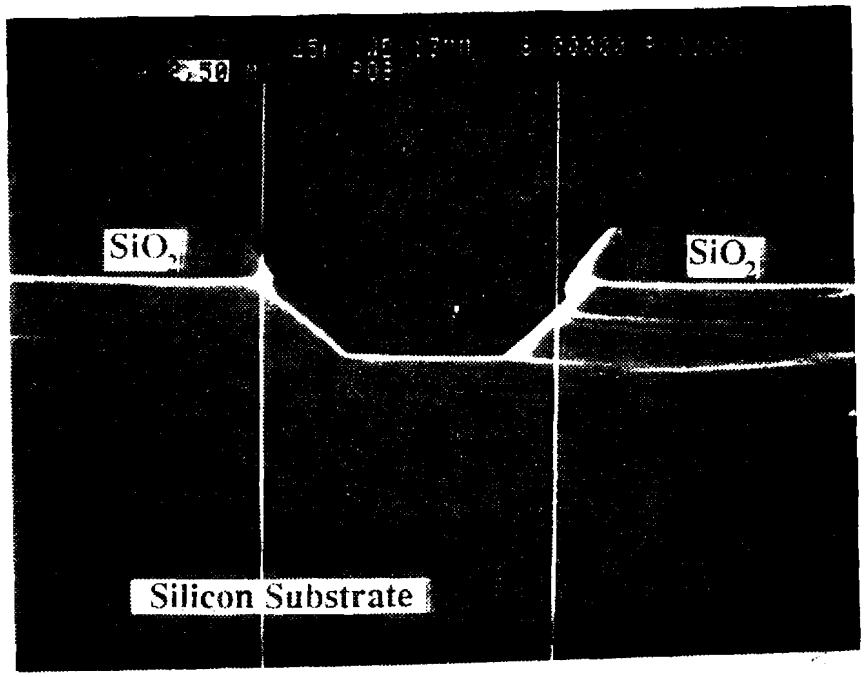


(c) Removal of oxide layer in BHF and after CMP

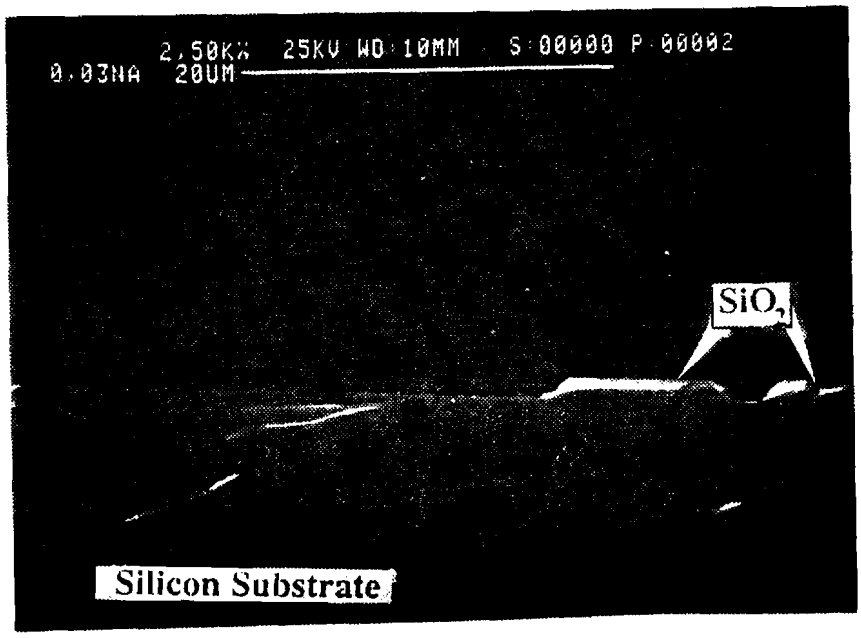


(d) Continuation of ELO/MELO growth to flat top

Figure 3.6. The SEG/ELO/MELO process including PEOX process.



(a)



(b)

Figure 3.7 KOH etching on PEOX treated seed holes.(a) SEM photograph showing the cross-section of the v-groove formation in Freon 115 etched seed hole.(b). SEM photograph showing equal etching of silicon in KOH near and away from oxide interface.

An attempt was made to investigate the effect of **PEOX** treatment on V-groove formation on **SEG/ELO** grown from more vertical oxide side walls. An 1μm thick thermal oxide was grown on (100) n-type wafers. The seed windows were etched by RIE with Freon 116 gas plasma for **200min** at **1000W** and 300 **mT** (about **500Å** of oxide was left and removed in BHF dip). Positive photoresist AZ 1350 was used as a masking material during this etch. Figure 3.8 shows the **SEM** photograph of the etched seed hole cross-section. Here the oxide side walls are almost vertical and the masking photoresist remained intact.

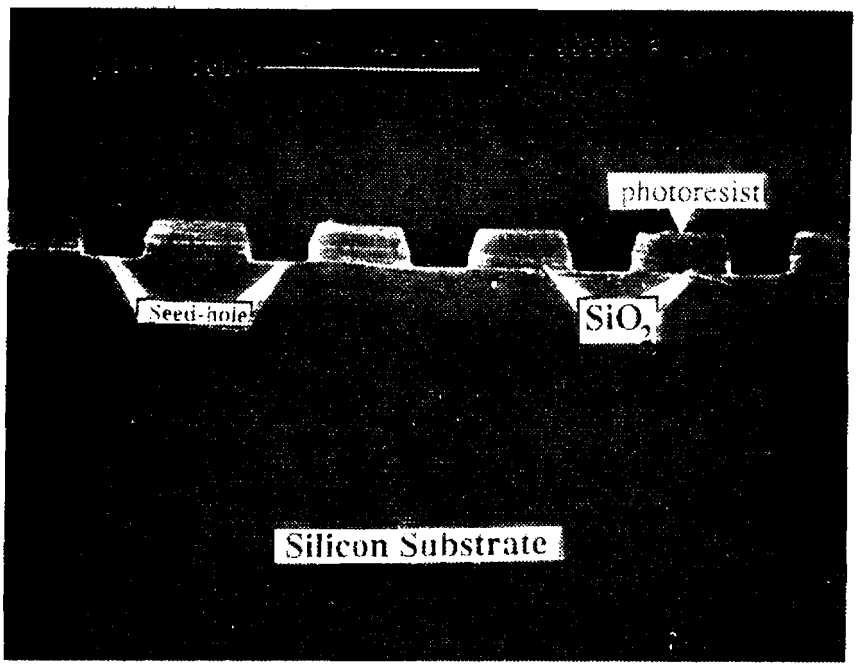


Figure 3.8. **SEM** photograph showing the cross-section of the RIE (Fr 116) etched seed holes.

The SEG/ELO used for these tests was grown for 20 min at 920' C, 150 Torr with 1.76 slpm HCl and 0.44 slpm DCS, resulting in 1.4 μm of growth. Figure 3.9 shows an SEM photograph of the top view of the ELO island grown from the RIE etched seed windows. The ELO spread was about 0.2p.m over the oxide surface. The wafer was put into a wet oxidation tube for an hour at 1000° C. After this oxide was removed in a BHF dip, the wafer was thoroughly cleaned in piranha. Then the wafer was put into anisotropic KOH etchant for a shot time (40sec). The cross section under SEM analysis shows the starting of the V-groove formation inside the oxide step [Figure 3.10(a)]. But a longer etch (3 min. long) has propagated the V-grooves to the bottom of the oxide sidewall without any undercutting [Figure 3.10(b)]. With further narrowing the seed hole width and using PEOX treatment on seed holes with vertical side walls will eventually keep the V-grooves inside the oxide side walls.

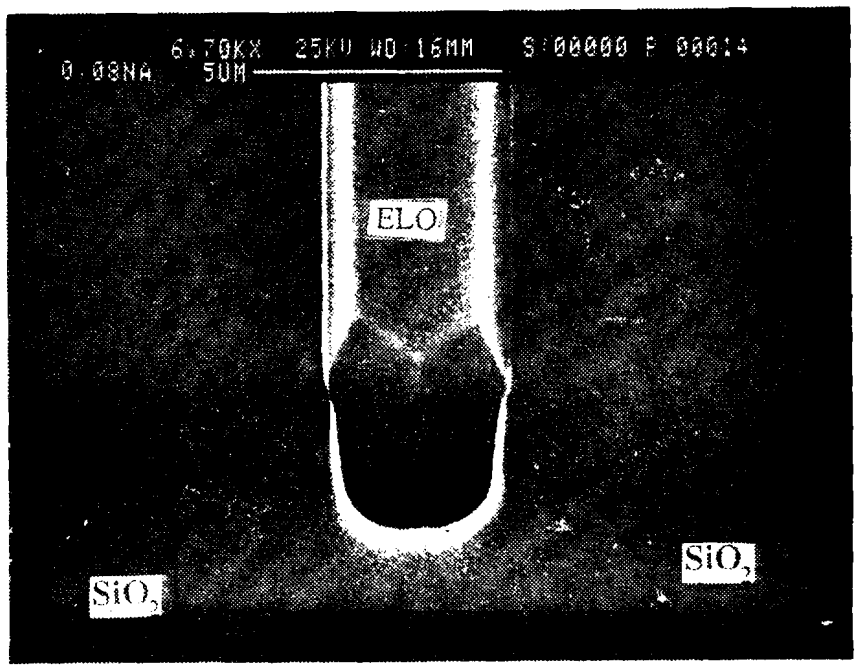
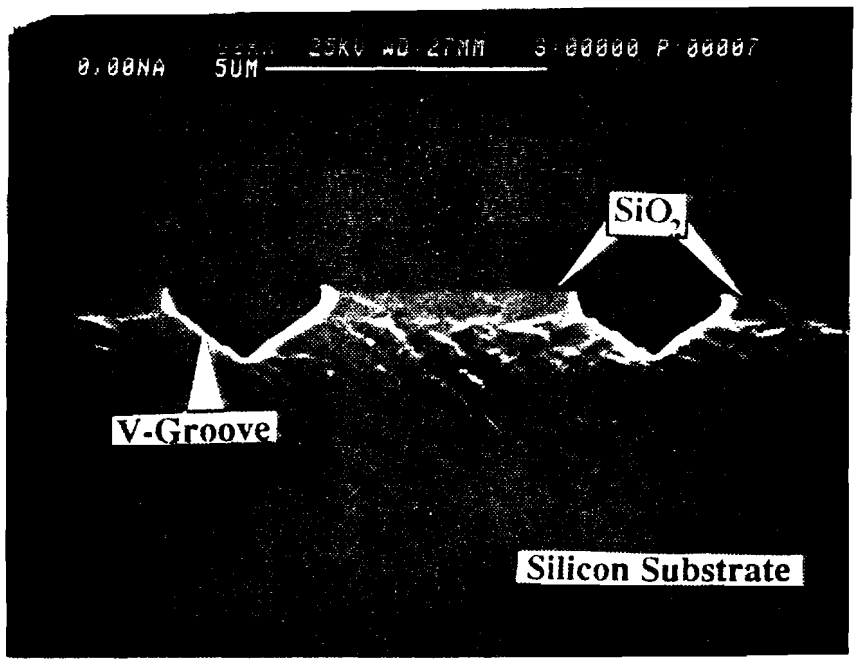
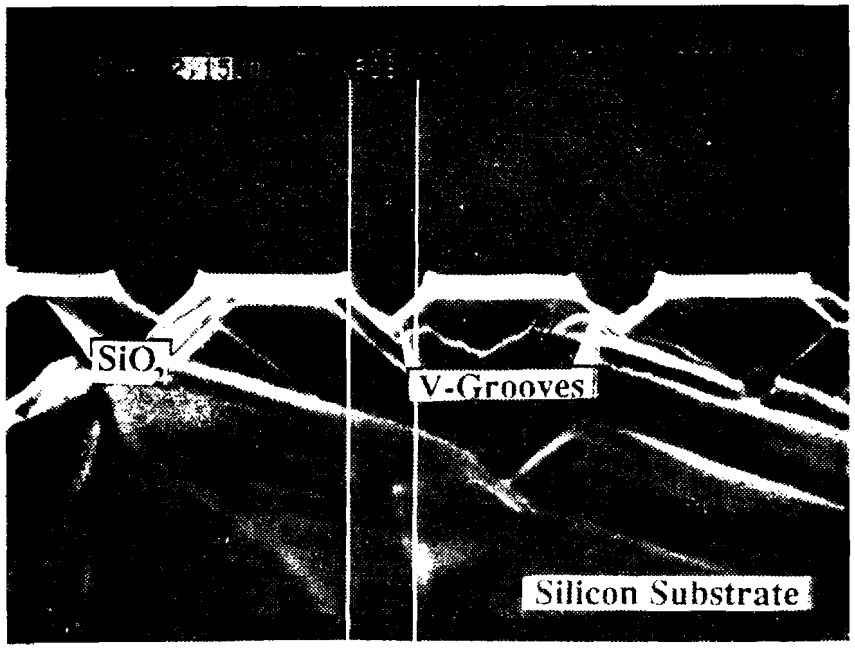


Figure 3.9. SEM photograph showing the top view of the ELO island grown from the RIE etched seed holes.



(a)



(b)

Figure 3.10. SEM photographs showing the cross-section of the V-grooves formed in the seed holes (etched by Freon 116) during KOH etching. (a) Cross-section after 40 second of etching. (b) After 3 minutes of etching.

3.2. Design of Chemical Etching System

The necessity to design a chemical etching system for the KOH etchant was due to two points: (1) the controllability of the operating temperature, and (2) the presence of the alcohol (n-propanol) additive. First, since it has been known that the etch rate of the KOH etchant increases as the temperature increases, a stable temperature during KOH etching ensures a small fluctuation in the etch rate. Therefore, a temperature controller, monitoring the etching system, was required to maintain a steady temperature. Secondly, the fact that n-propanol is contained in the KOH solution means that alcohol vaporization will occur at 80°C after some time. Although n-propanol (boiling point of ~97.3°C) will not totally evaporate at 80°C, a controlled environment helps to sustain the content of the alcohol in the etchant. Thus, a semi-enclosed system prevents the n-propanol from escaping too quickly. Note that this also promotes a safety feature during etching because excessive alcohol vapor can be a potential danger. Next, the arrangement of the etching system will be described as well as its optimization for temperature control. Incidentally, the same system may also be used for EDP etching solutions; this will become apparent as the system is being described.

3.2.1. Beaker-Within-Beaker Arrangement

A bath type system is a very typical heating arrangement and has been used for many years. At the commercial level, a bath system with a temperature controller is priced nominally between $890 (lower model) to $3500 (top model). To prevent adding cost to the experiment, an attempt was made to use the existing hot plate (Thermolyne Type 1000) and temperature controller as part of the etching system. The only other module missing from the etching system is a container that holds the etchant. Although a simple beaker may be used as the container, an insulation surrounding the etchant is desirable in order to maintain a steady temperature. Because the experiment will be performed under a ventilated hood, which has a varied air flow velocity, the insulation will keep the etchant from cooling at various rates. A proposed schematic of the etchant container was created and illustrated in Figure 3.11.

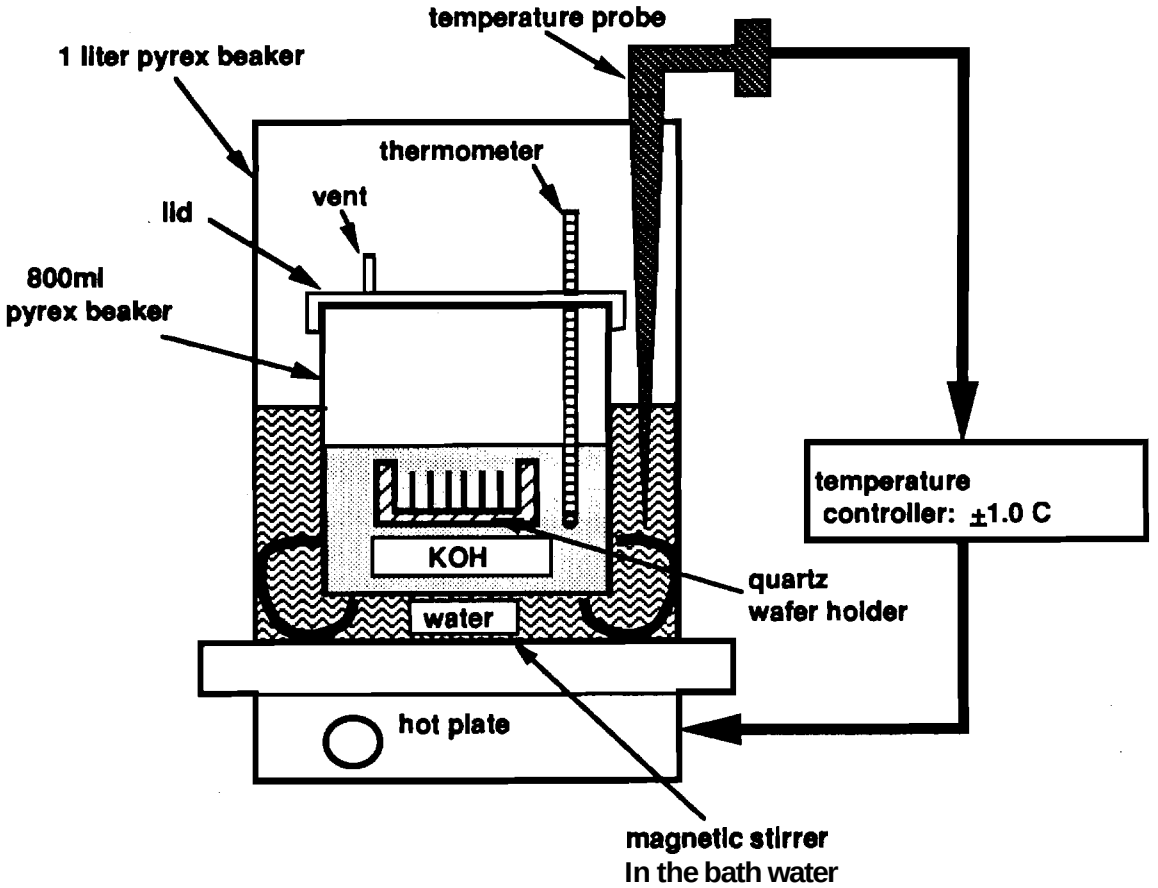


Figure 3.11. KOH etching system using **beaker-within-beaker** arrangement and Omega temperature controller.

There are a few characteristics in Figure **3.11** to note. First, a thennocouple is placed in the water bath instead of in the KOH solution because the water bath acts as a buffer between KOH **etchant** and the cool air as well as a constant heating source. To keep a steady temperature, the temperature controller adjusts the cycling of the hot plate and the magnetic **stirrer** according to the measured water-bath temperature. To let the heat flow throughout and around inner beaker, the inner beaker must be slightly raised; this also allocates a space under the inner beaker for stirring bath water. Hence, the feature promotes **constant heating** along the side and bottom of the inner beaker. Therefore, when the system is at equilibrium, the **etchant** will be heated close to the temperature of the bath water. To be certain that the **etchant** was reaching to close the water bath temperature, a mercury thermometer is placed inside the **etchant** through an opening in the lid. Second, a

vent is built into the lid to sustain pressure equilibrium. Lastly, the KOH etchant is agitated by the hydrogen released while silicon is being etched.

As mentioned before, the same system can be modified for the EDP etchant. There are two crucial properties of the EDP etchant that must be considered in the etching system. First, stirring the EDP etchant does affect the etch rate, and second, EDP etchant (thus, the etch rate) is affected by the exposure to oxygen or air during etching. Therefore, to incorporate both features into the etching system, nitrogen gas can be piped into the etching solution through the mercury thermometer opening. By blowing nitrogen into the etchant, the EDP solution is agitated while a large portion of air in the inner beaker is pushed out through the small vent. Note that the system is by no means air tight; however, the amount of air introduced to the etchant is minimized by blowing nitrogen into the semi-enclosed etching container. If a mercury thermometer is desired to monitor the etchant temperature, a third hole can be built into the lid for that purpose. Yet, as alluded to above, the temperature in the inner beaker should reach that of the water bath at equilibrium. The characteristic profile of temperature versus time needed to investigated for the etching system. Next, the optimization of the Omega temperature controller is presented.

3.2.2. Optimization of Omega Temperature Controller

The temperature controller primarily has a 2-wire thermocouple input and two outputs (SP1 and SP2). The two outputs are different in that SP1 is a solid state driver (SSD, 5V DC pulsed output) for an external DC controlled solid state relay (SSR240DC10) and SP2 is a 3A mechanical relay. Since there is only one input to the hot plate, through the power cord, only SP1 was enabled. If another system such as a cooling module is also used, then it may be controlled by SP2 mechanical output. The hot plate is a Thermolyne Type 100, which has a built-in magnetic stirring controller. The magnetic stirring cycle is enabled only when the heating cycle is on; it is disabled during the off cycle or when the stirring rate is manually turned off. Because the hot plate has its own heating controller, the heating power was set to the highest value (700W) in order to prevent conflicts between the heating controller of the hot plate and the temperature controller. Thus, the hot plate was always on relative to its controller and was disabled only by the temperature controller. With a brief description of the specifications of the temperature controller and the hot plate, the characteristic of the warm up and steady state profiles will be reviewed.

The tuning of the KOH etching system is basically a trial and error process. The temperature controller primarily has five parameters that can be varied for each output (SP1 or SP2). There are three elementary approaches to adjusting the system. First, the factory setting can be used to recalculate a new temperature controller setting. Second, if the new setting fails to give the desired temperature range, another setting can be obtained by using the built-in autotune during warm-up. Third, if the system still fails to give the desired result, another new setting is obtained by autotuning around the setpoint (or push-to-tune). If none of the three gives the appropriate process control, the best temperature profile is selected among the three approaches and, then, fine adjustments are made to any of the five basic parameters, accordingly.

Since a large portion of the KOH solution was water, initial experiments were carried out using water only. Thereafter, KOH solution was used to verify that the etching system was controlled within the requested temperature range. It was found that autotuning during warm up could not be done for this particular system due to the long proportional cycle time required (> 82 sec, max. limit). Instead, the system was autotuned by push-to-tune such that a semi-desirable temperature control was obtained. Yet, overshoot at initial warm up caused the system to stabilize at a slow rate; therefore, a derivative approach control, which enabled proportional cycling during part of the warm up, was done. Thus, the system optimizes at a warm up time of 50 min. to 1 hour. It is able to sustain the etchant temperature at $80 \pm 1^{o}C$ even though the bath water varies by as much as $\pm 3^{o}C$. This shows that the bath water does indeed buffers and heat the etchant to a constant temperature. However, it is cautioned that because the system is situated under a vented hood, the system can vary more than desired if the air flow in the hood changes frequently. Lastly, the system is tuned for a certain amount of KOH etchant and, therefore, bath water. A system lag is detected if more water is used in the bath, i.e. $\geq$ 850 ml of bath water. With the system optimized, the KOH characteristics may be evaluated as explained in the next section.

3.3. KOH Etching Characteristics

There are two types of anisotropic etching depending on the pattern: concave etching and convex etching. Generally, in concave etching, the measuring parameters to consider are vertical and lateral etch rates. In anisotropic etching, it is commonly desirable to have a large vertical etch rate for substrate wafer etching and to have small lateral etch

rate in order to reduce mask compensation of lateral undercuts. In convex etching, corner undercuts are usually observed for KOH etchant. Because a rectangular mesa is usually preferred, many designs have been attempted to suppress the corner undercuts by means of adding a compensation mask at each convex comer. The corner compensation mask basically buffers the convex comers from undercuts during the etching of the mesa. The essential result after etching the mesa with a comer compensation mask is a more rectangularly shaped proof mass. The convex corners can be analyzed by using a two-level Taguchi (or factorial) experiment fur two factors. Then, the results are used to better predict the corner compensation mask size such that the corner protrusion is minimized. Note that two indirect objectives are stated by the experiment: (1) minimizing the comer compensation mask means tightly controlled, therefore, repeatable process and (2) minimizing comer protrusion means better estimates of the mass proof weight for the accelerometer. In the next few sections, some general properties of the KOH etchant for (100) wafer with rectangular patterns will be reviewed, and then the experimental results concerning parameter variation are presented.

3.3.1. General Properties

Before continuing into discussing the experimental results, there are a few properties, previously observed in last year's work as well as in related articles, that should be kept in mind during processing. These properties may be grouped as possible sources of error that varies processing results by a certain standard deviation. So, to minimize the error, precaution must be taken before and during KOH etching. Two distinctive features that have been frequently observed come into mind: (1) cleanliness of the wafer surface before KOH etching and (2) orientation dependence of mask alignment as well as that of the initial wafer.

In the first case, the wafer must be ultraclean because any particle situated on the wafer acts as an "apparent" masking pattern. Therefore, the KOH solution will etch anisotropically around that speck of particle(s). Whether or not the particulate is removed from its initial site during etching is not important because a depression has already been made in the beginning and will continue to exist. Thus, a black pyramid will form on the surface after the etching is completed. So, it is important that both the wafer and the etching apparatus are thoroughly cleaned. The cleaning technique for a wafer is the standard piranha clean ($1H_2SO_4:2H_2O_2$) for 10 to 15 min. and then 10 min. DI (deionized) water

rinse. Next, a quick (max. of 20 sec) BHF dip followed by at least 10 min. rinsed under running DI water is done. Note that to do the BHF dip the protective mask cannot be oxide, and indeed, the mask used is plasma enhanced vapor deposited nitride (PECVD). For the apparatus, the clean is a 20-minute soak in aqua regia solution ($3HCl:1HNO_3$) followed by a rinse in running DI water for at least 10 min. In addition to the cleanliness of the wafer surface, the orientation of the mask alignment as well as the initial wafer is also crucial to obtaining consistent performance.

For the second case, since KOH etching is orientation dependent, any mask misalignment can give unwanted results. On a large scale, mask misalignment can be depicted when a rectangular mask is aligned either to <110> or <100> direction. In the former case, the sidewalls are smooth while, in the latter case, they are striated. In this annual summary, the analysis will be limited to <110> mask alignment. When misalignment occurs on a smaller scale, it is not readily observed since the etchant basically creates a larger concave trench and a smaller mesa convexly. In other words, the etchant looks for <111> limiting planes which circumscribe the concave pattern, and the mesa that is surrounded by a concave pattern has effectively a smaller dimension than the initial pattern. Since the final mesa is effectively smaller from the misalignment, the convex comer facets will also change its dimensions though not necessarily its plane of facet, (212). Note that the same misalignment implies that the lateral etch rate "appears" to have increased. If it is desired to reach a certain underside pattern after some time of etching, the "apparent" lateral etch rate will increase undercutting the underside pattern. This is especially true for long etch time such as substrate wafer etching. Without an accurate equipment to orientate the mask relative to the wafer, the wafer flat is used as a visual reference. However, orientating relative to the wafer flat implies that the wafer flat is orientated properly in the first place. Therefore, alignment technique along with the initial wafer misalignment adds error to etching performances. In short, care must be taken before KOH etching especially in cleaning and pattern alignment. Next, the parameter variation of the experiments is discussed.

3.3.2. Effect of Parameter Variation

To determine the dimensions of the corner compensation mask for the accelerometer, an experimental etch was necessary to estimate the comer undercut etch rates. However, additional experiments were performed to characterize the behavior of the

KOH solution. To ensure that the temperature variation in the etchant had small effect on the etch rate, a temperature controller with a bath setup was used (refer to Section 3.2). The following experiments using KOH solution were performed: (1) rough estimate of etch rates and undercuts with a maximum temperature variation of ±5°C, (2) effects of etch rates and comer undercuts by varying KOH and n-propanol contents and with low temperature variation, ±1°C, and (3) aging effect of the solution during about 6 hour etch. The effect of using a tuned process on the mass proof of the accelerometer with a compensation comer mask, estimated from the first experiment, will be described in Section 4.2. Note that the first experiment used p-type (100) wafer while all other experiments used n-type (100) wafers in a water/KOH/n-propanol solution set for 80°C.

3.3.2.1. Experiment 1: Etching Under ±5°C Variation

In the first experiment, the solution contents (in weight percent) were 63.25% H_2O, 13.34% n-propanol, and 23.41% KOH. The experiment was performed without an optimal tuning of the temperature controller; therefore, a maximum temperature variation in the solution was found between ±5°C for an hour etch. A 2" p-type (100) wafer with LPCVD nitride mask was used. The mask &sign is shown on Figure 3.12, which includes both concave and convex features as well as <110> and <100> alignment patterns. The mask shown is primarily used to determine KOH etching characteristics. Yet, for this particular experiment, only the <110> alignment pattern was interested. Tencor alpha-step surface profilometer was used to measure the vertically etched depth, and an SEM (scanning electron microscope) was used to measure eight different characterizing parameters around the convex corner, covering an area of eight dies per wafer. The different SEM measurements are illustrated in Figure 3.13. Besides quantitative observations, some qualitative observations, such as surface morphology, were also made by using the SEM. The measured parameters are basically converted to terms, such as etch rate, etc., that can better describe the etching characteristics and, therefore, determine the comer compensation mask. Next, a brief explanation will be given to the measured parameters and then the results of the experiment will be revealed.

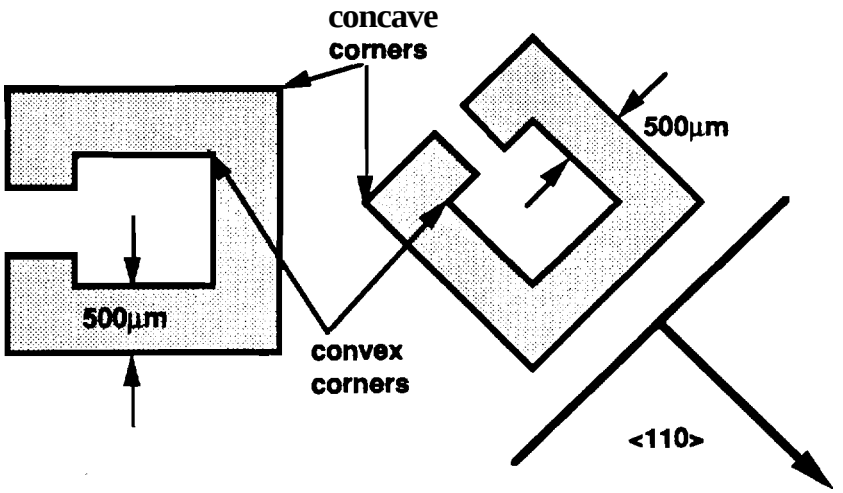


Figure 3.12. Concave/convex characteristic patterns

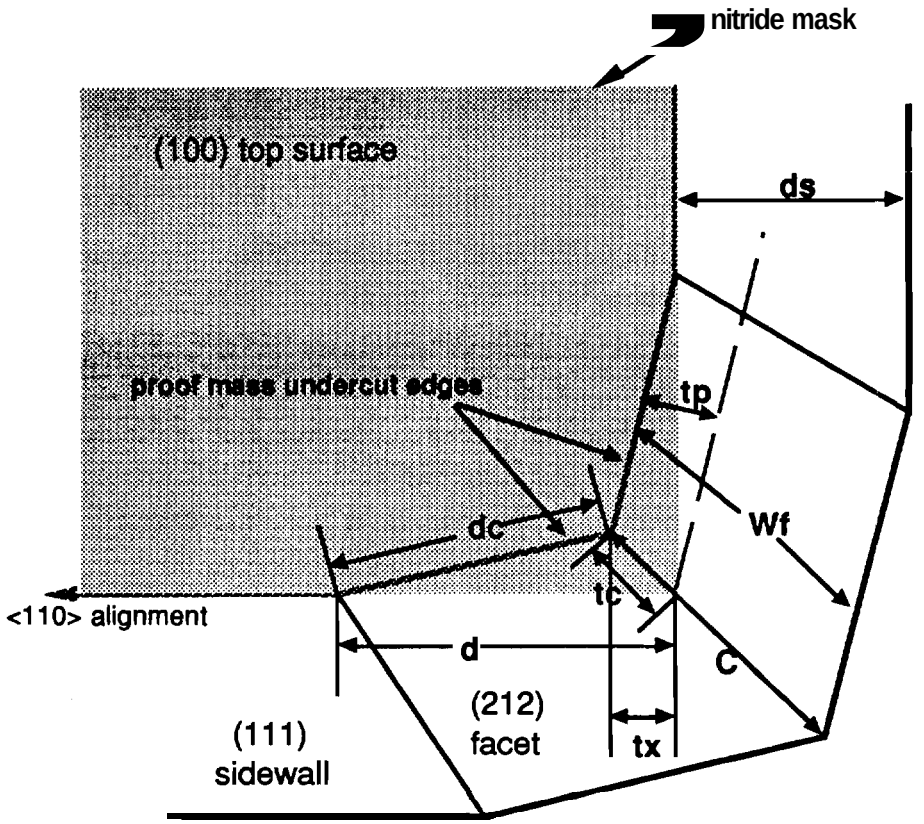


Figure 3.13. Top view of a convex comer with SEM-measuring parameters.

Starting with the easiest parameter, the vertical depth of the etch (measured by the alpha-step profilorneter) can be divided by the etch time to obtain the etch rate. From Figure 3.13, the SEM measurements are either top (surface) projections of the inclined surfaces or traces of the inclined planes on the (100) surface. Since many times the desired etch depth is known, it seems appropriate that the depth should be included when designing the corner compensation mask. Therefore, d and tc are divided by the vertical height to obtain relative undercut (or relative comer undercut) and relative tip undercut, respectively. It will be explained in Section 4.2 how these values are used to calculate the corner compensation mask. Parameters dc and tx axe alternative parameters to d and tc, respectively, because they can be converted through geometric relations. Note that dc and tc are at an angle relative to the sides of the mesa; therefore, they are perhaps more difficult to align for measurement. To verify the sidewall plane and the comer faceting plane, ds and Wf are measured to determine (by the right triangle law) the angles of intersection between the inclined planes and the (100) plane. C parameter can also be used to determine the angle between (100) plane and the intersecting line of the corner facets (the corner tip). tp is measured out of interest. For this experiment, these parameters were measured and used to approximate an initial corner compensation mask.

Averaging eight dies, the vertical height, tc, tx, ds, Wf, C, and tp had less than or equal to 5% deviation from their mean values. However, d and dc had approximately 6% deviation. Although one may reason that if d and dc are smaller in values, then the measurement error should be greater. Yet, that is not the case since tc, tx, and tp are in the 10-20μm range while d and dc are in the 50-70μm ranges. Therefore, it is inconclusive from the experiment as to why d and dc have a larger variation within a wafer. Speculation of the cause includes small misalignment of the mask relative to <110> and low resolution of the mask definition. Using the mean value only, the estimated etch rate, the relative comer undercut, and the relative tip undercut were found to be 0.92 μm/min, 1.25 μm/μm, and 0.36μm/μm, respectively. To verify the sidewall plane and the comer faceting plane, the angles of intersection were 56.80 and 49.30, which corresponded to the expected value of 54.740 for (100) to (111), and 48.190 for (100) to (212), respectively. Without going into detail, the comer compensation mask had an overall square dimension of S_T=280μm, and it overlaps the corner of the mass proof by a square dimension of d_Δ=175μm (refer to Section 4.2 and Figure 4.2.1 for corner compensation mask). The comer compensation mask was developed using an untuned etching system because initial observation of the accelerometer was necessary. In short, percent variation (from the mean) within a wafer is

less than or equal to 5% for most SEM measured parameters and the etched depth, and parameters specifically related to the convex comer (d and dc) have a greater variation.

3.3.2.2. Experiment 2: Etching Under ±1°C Variation Using Two-Level Taguchi Design

The second experiment was a two-level Taguchi (factorial) setup where KOH and n-propanol were the varied factors. The high and low levels (in weight percent) of each element were 33% and 23.4% for KOH, respectively, while for n-propanol 15% and 13.3%, respectively. The etching system were controlled to 80±1°C. Four 2" n-type (100) wafers with PECVD nitride mask were used, one for each run. Again, the same mask, Figure 3.12, was used. Note that four runs were performed with an etch time of two hours. The same parameters in experiment 1 (Section 3.3.2.1) were measured in this experiment, except twelve dies were measured per wafer (or run).

Like the first experiment and refemng to Figure 3.13, only d and dc parameters had greater than 5% deviation per wafer for all runs. All other parameters, excluding tc and tp, remained less than 5% except for tx. It may be hypothesized that tx, d, and dc could have an increased percent deviation per wafer due to the type of mask used. This can be supported by the fact that no measurement was made on tc and tp because the nitride mask comer (overhanging the comer undercut) could not be clearly defined and, therefore, referenced during measurement. Furthermore, it was difficult to pinpoint the beginning of the faceting plane from the (111) sidewall ford and dc measurements. Using the average of each parameter, descriptive values were determined and listed on Table 3.1. Note that the values for experiment 1 are listed as well.

From Table 3.1, the averaged results in each run show that at a low level of n-propanol, variation of the KOH has little effect on the vertical etch rate, -0.98 μm/min. At a high concentration of KOH, variation in n-propanol has small effect on relative comer undercut. Therefore, the dimension of the comer compensation mask decreases when KOH is increased close to 30% in the presence of n-propanol. However, at low concentration of KOH, increasing n-propanol also decreases mask size but the vertical etch rate is decreased as well. In the same table, note that the angles of intersection for both the (111) sidewall and (212) facet, relative to (100) plane, are very close to the expected values. No specific comparison can be made for relative undercut or for relative tip undercut. To better analyze

the sources of variation, an **ANOVA** (analysis of variation) calculation is performed on the collected data using the SAS (Statistical Analytical System) software.

Table 3.1: Values determined from averages of measured parameters.

	KOH	N-Prop.	Vert. ER (µm/min)	Cross Sec.: a (100):(111) degree	Cross Sec.: b (100):(212) degree	Riv Undrcut (µm/µm)	Riv. Tip Undrcut (µm/µm)
Experiment 1: Etching Under +/- 5°C Variation							
Uncontrolled W#Z (p-type)	23.41% 479m	13.34% 39ml	0.92	56.8	49.3	1.25	0.36
Experiment 2: Etching Under +/- 1°C Variation Using 2-Level Taguchi Technique							
RUN #1 W#EXP1-n5 (n-type)	23.41% 47gm	13.34% 39ml	0.97	54.4	47.5	0.70	0.26
RUN #2 W#JCCM19 (n-type)	23.38% 48.2gm	15.00% 45ml	0.84	53.4	47.0	0.62	0.23
RUN #3 W#JCCM18 (n-type)	33.00% 78.1gm	13.35% 46 ml	0.98	53.8	47.2	0.59	0.24
RUN #4 W#JCCM20 (n-type)	33.03% 80.6gm	14.92% 53ml	0.88	53.4	47.6	0.59	0.23
Expected Values			~1	54.74	48.19		

**Note: Water content to tach run is exactly 127ml.

Using ANOVA, all measured parameters, shown on Figure 3.13, were evaluated separately. The main effects are KOH and n-propanol. The sources under consideration are the main effects and the interaction of the main effects. Of the measured parameters, only the vertical depth, (111) sidewall top projection (ds), comer facet top projection (Wf), and line of intersection at the comer (C) can be modelled to accountable sources by ANOVA. The other parameters (d, dc, and tx) are not properly modelled by ANOVA because the error variation accounts for more than 10% of the total variation. Recall that tp and tc could not be measured in the second experiment. For the four parameters modelled, the ANOVA results show that the vertical depth (thus, the etch rate) can be significantly affected by KOH, n-propanol, and/or the interaction of the two with a confidence level greater than 95%. In other words, the variance (variation divided by the degrees of freedom) due to a source compared to the individual error variance is large enough to be significant at a 95% confidence level using the F test. However, the percent contribution of each source to the total variation is the greatest for n-propanol, ≥ 94%. Therefore, if the vertical etch rate needs to be adjusted for any reason, the first variable to adjust is the alcohol content. The (111) sidewall top projection (ds) is at least 95% significantly affected by KOH and n-propanol, but not by the interaction of the two constituents. Again, the percent conmbution of variation is the greatest for n-propanol. For both Wf and C, the same conclusion is made as that for parameter ds. Therefore, it seems changes in the alcohol content can cause a mean shift to vertical etched depth, ds, Wf, and C parameters, especially to the etch rate.

When the overall variation (all collected data of the same type) due to the error source accounts for more than 10% of the total variation, as in the cases for d, dc and tx, the experiment basically has not considered all possible sources that make up the total variation. That is, besides KOH, n-propanol, and the interaction of the two components, there must be other sources that are causing the error variation to be large. Yet, even with a large error, the ANOVA (more specifically the F test) performed on d, dc, and tx shows that the three parameters can to be significantly affected by the n-propanol. This does not indicate that n-propanol has the most percentage of contribution to the total variation and is, therefore, the first factor to be adjusted when a mean shift occurs. Instead, it simply implies that one can expect some mean variation (relative to the large error variance) in the parameters d, dc, and tx when the alcohol content is varied at the two levels. In conclusion, ANOVA results support the observations made from Table. 3.1. They demonstrate that n-propanol can significantly affect all parameters. However, n-propanol is not a major contributor to the total variation when looking at parameters related to the comer undercut, i.e. d, dc, and tx, while it is a large variation contributor for etched depth (thus, etch rate),

ds, Wf, and C. Note that d (or dc) and tx are related to relative undercut and relative tip undercut, respectively. As it will be explained in Section 4.2, d, dc, and tx can still be used to determine the comer compensation mask despite their large error variation. Next, the aging effect of the KOH etchant is described.

3.3.2.3. Experiment 3: Effect of Aging Etchant Under ±1°C Variation

From experiment 2, it was found that n-propanol can affect the etch rate (low n-propanol increases etch rate). Since no supporting evidence can justify in changing the content of KOH for the purpose of reducing relative undercut and/or relative tip undercut, the content used in experiment 2, run #1 was used in the third experiment. Note that the same ingredient was also used in experiment 1. In the third experiment, the first set of accelerometer mask (based on experiment 1 results) was used to look at the aging effect of the KOH solution, 63.25% H_2O, 13.34% n-propanol, and 23.41% KOH. Four pieces divided from a 3" n-type (100) wafer with PECVD nitride mask were used; after 2.3 hrs of initial etching of the first piece, one piece (of the three remaining pieces) was added to the solution at every 1.5 hour. For the 6-hour etched piece, the vertical etch rate was 0.98 μm/min. This is consistent with that obtained in the second experiment, run #1, which is set for only a 2-hour etch. In addition, lateral undercut was observable after a 6-hour etch; however, it was not measurable because the overhanging mask layer has broken off. For pieces etched after 2.3 hr., 3.8 hr., and 5.3 hr. age of the solution, the vertical etch rates were found to be similar, -0.85 μm/min. Refer to Table 3.2 for list of results.

From the results of this experiment, it can be concluded that if the solution has been used to etch other wafers continuously for an effective time of approximately 2 hours, the strength of the etch rate deteriorates by at least 13%. However, less than 4% of etch rate reduction was found among the wafers added after the initial 2.3 hour of etching. Therefore, it seems that the etch rate is most dominated by the initial etch strength of a fresh solution than that of a used solution. This is especially supported by the fact that the 6-hour etched piece in the third experiment has a comparable etch rate to the 2-hour etched piece (run #1) in experiment 2. The same fact indirectly implies that the etching system has a tuned process since similar etch rates can be observed in two different experiments. The reason for the etch rate reduction after 2 hour usage of the solution is inconclusive because the experiment does not target for sources of variation but targets for the overall effect after the etchant is used. Thus, it is concluded that the initial strength of a fresh etchant

dominates the effective overall etch rate for either 2 or 6 hour etch and that the weakness of a used etchant is not seen unless a new wafer is added thereafter.

Table 3.2. Aging KOH Etchant Vertical Etch Rates -- determined from average of data.

	KOH	N-Prop.	H2O	Vert. ER (µm/min)
Experiment 3: Aging Etchant Under +/-1ºC Variation				
fresh solution (6hr tot. etch) (n-type)	23.41% 47gm	13.34% 39ml	63.25% 127ml	0.98
after 2.3 hr (2hr tot. etch) (n-type)	"	"	"	0.85
after 3.8 hr (2hr tot. etch) (n-type)	"	"	"	0.83
after 5.3 hr (2hr tot. etch) (n-type)	"	"	"	0.86
Experiment 2: Etching Under +/-1ºC Variation Using 2-Level Taguchi Technique				
RUN #1 W#EXP1-n5 (2hr tot. etch) (n-type)	23.41% 47gm	13.34% 39ml	63.25% 127ml	0.97

3.3.2.4. Summary of Parameter Variation

In summary, an etching system with a steady temperature fluctuation regardless of its range gives very little etch rate variation within a wafer, as demonstrated between experiments one and two. However, from the same experiments, it is possible that the difference in the mean etch rates is due to the range of temperature variation even though the wafers are lowly doped by two different impurities. Therefore, by excluding the temperature variation factor through tight control of the etchant temperature, a second experiment designed by a two-level Taguchi (or factorial) technique is analyzed by ANOVA using a SAS program. The ANOVA results show that given the level of variation of KOH and n-propanol, the etch rate is mostly varied by the n-propanol contribution even though both factors and their interaction do cause significant variation (as compared to the individual error variation) at the 95% confidence level. However, the relative corner undercut and relative tip undercut was not properly modelled using the ANOVA technique because the error variation was too large. This indicates that not all sources that affect the corner parameters (d, dc, tx) have been considered besides the KOH and n-propanol factors. Moreover, since large percent variation (standard deviation divided by the mean) have been observed for the corner parameters in the first experiment as well, the fact that other sources exist is further supported. The second experiment has also demonstrated that there is not a need to change the weight percent content of either KOH or n-propanol because the variation of the comer parameters are due to other undetected sources and no advantages are gained if either content are increased. Note that the solution content used in experiment one gives both high vertical etch rate and lower relative corner undercuts in experiment two run #1 with a tuned etching system. Looking at the aging effect of the KOH solution in the third experiment, it is found that the change of etch rate (or the etchant strength) is not observable or significant when a fresh solution is initially used to etch the wafer. This is verified by a comparable mean etch rate obtained in both the two-hour etch in experiment 2 (run #1) and the 6-hour etch in experiment 3. However, if a new wafer is etched in a used ($\geq$ 2.3 used-hours) etchant, the reduction of the vertical etch rate indicates that the solution strength has weakened. In addition, lateral undercut can be observed when the etch time increases. Specific lateral etch rate was not measurable in experiment 3 because the overhanging nitride had broken off. Finally, the results of all experiments are used to determine the comer compensation mask; the discussion is carried in the following section.

3.4. Corner Compensation Design and Back Etch

In this section, the etch back of the proof mass, including the the design of the convex comer compensation mask, is covered. First, a brief description on calculating the comer compensation mask is described. Then, a list of different mask dimensions is presented for two of the three experiments discussed in section 3.3. Critics are delivered on these calculated results as well as the experimental outcome of the first comer compensated accelerometer mask used in an actual accelerometer fabrication.

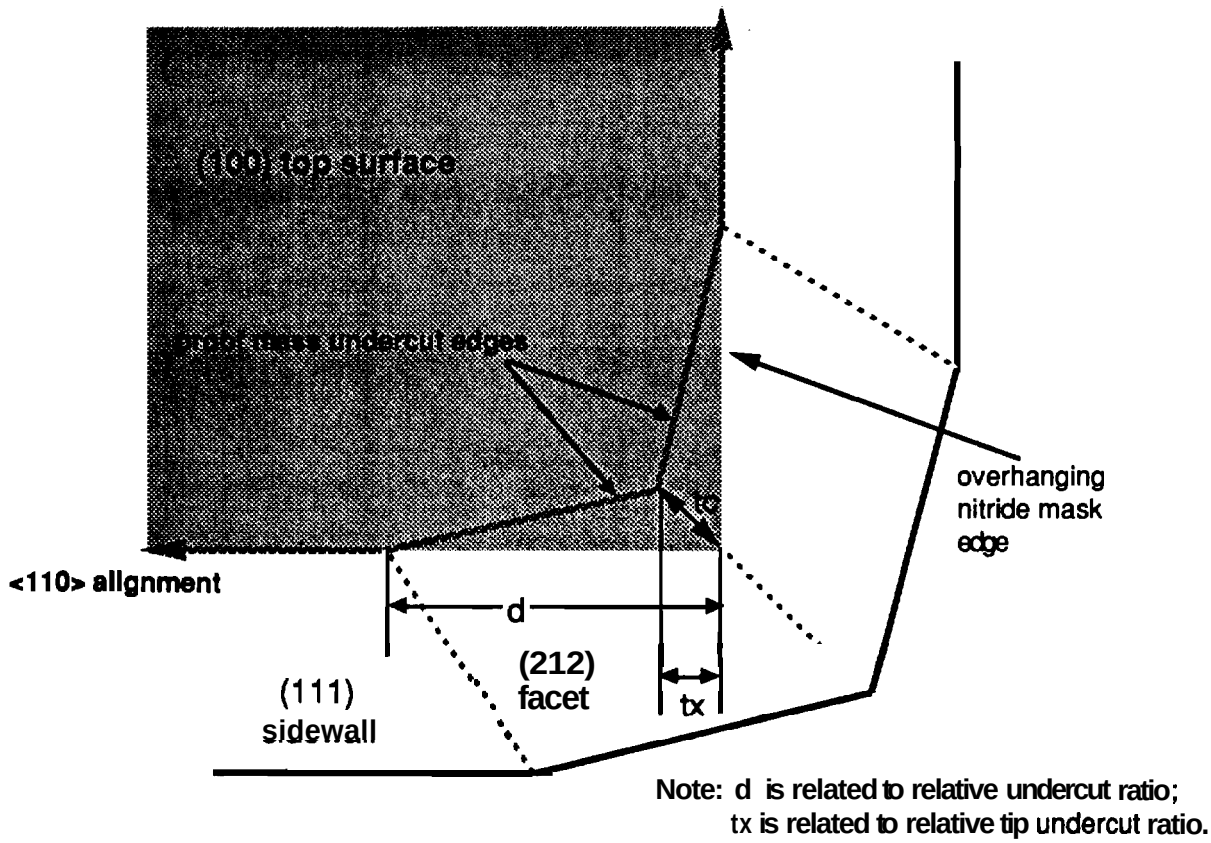


Figure 3.14. Top view of a convex comer with parameters used to design corner compensation mask

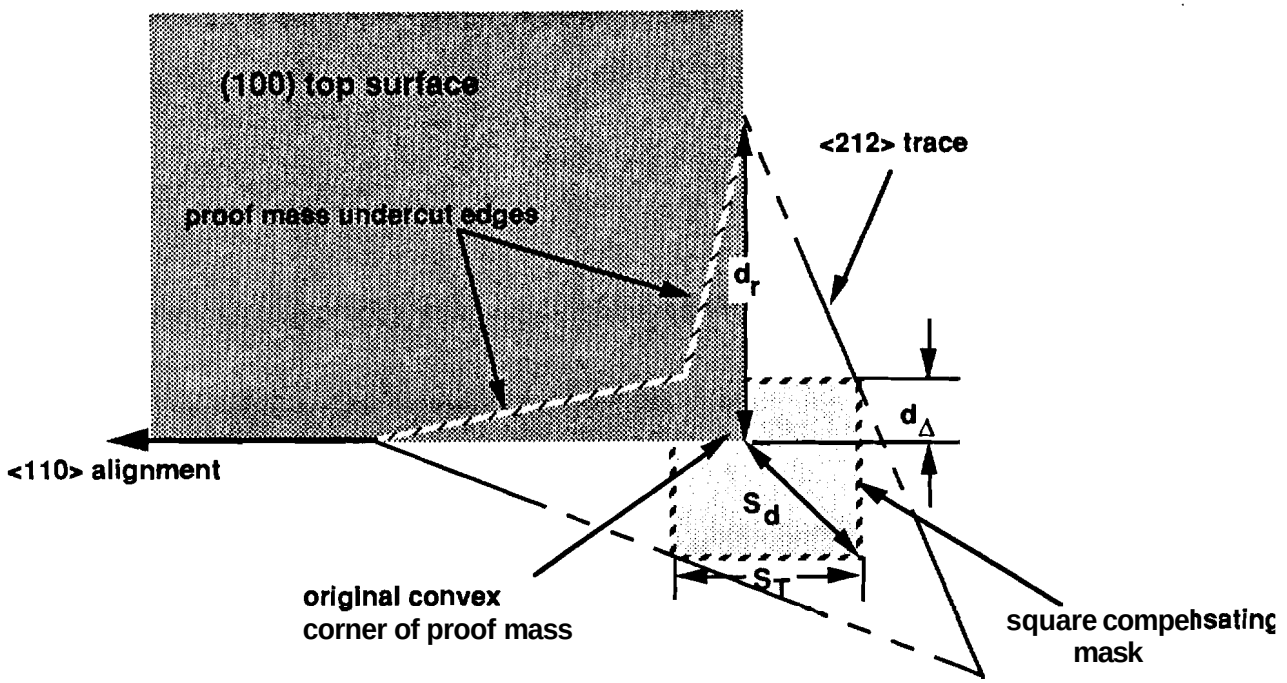


Figure 3.15. Top view a square comer compensation mask using <212> traces.

To calculate the comer compensation mask, relative comer undercut (d divided by the etched depth in Figure 3.14) is used to determine the length, dr, in Figure 3.15. dr defines a point along the sides of the 90° comer to begin drawing <212> traces. Then, the relative tip undercut (tc divided by the etched depth in Figure 3.14; tc is derived from tx geometrically) determines the diagonal length, Sd, of the square compensating mask starting from the mesa comer (Figure 3.15). Thus, the dimension (S_T) of the square mask bounded by the <212> traces and the overlapping dimension (d_Δ) can be found through geometry.

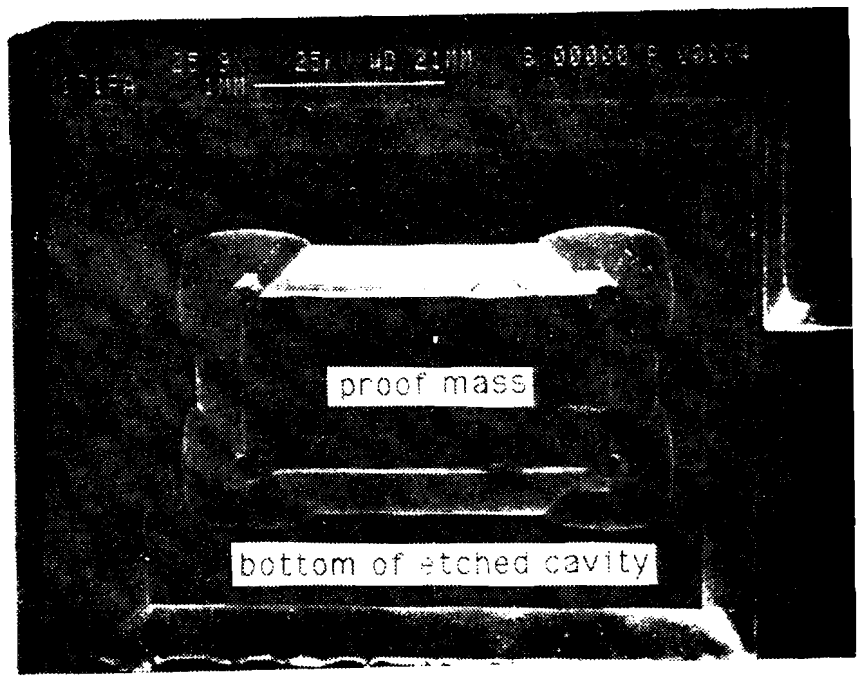
Recall that two experiments were performed to observe and determine characteristics of convex comers in the KOH etchant (Section 3.3). Using the described mask calculation above, each run in both experiments had an estimated comer compensation mask, listed in Table 3.3. Because an initial comer compensation mask for the accelerometer was needed before the completion of the second (more temperature controlled) experiment, a comer compensation mask based on the first experiment was made. This particular comer compensation mask will be called Ccmask #EXP1. Ccmask #EXP1 was tested out in an actual fabrication of an accelerometer.

Table 3.3. Corner compensation dimensions based on averaged data

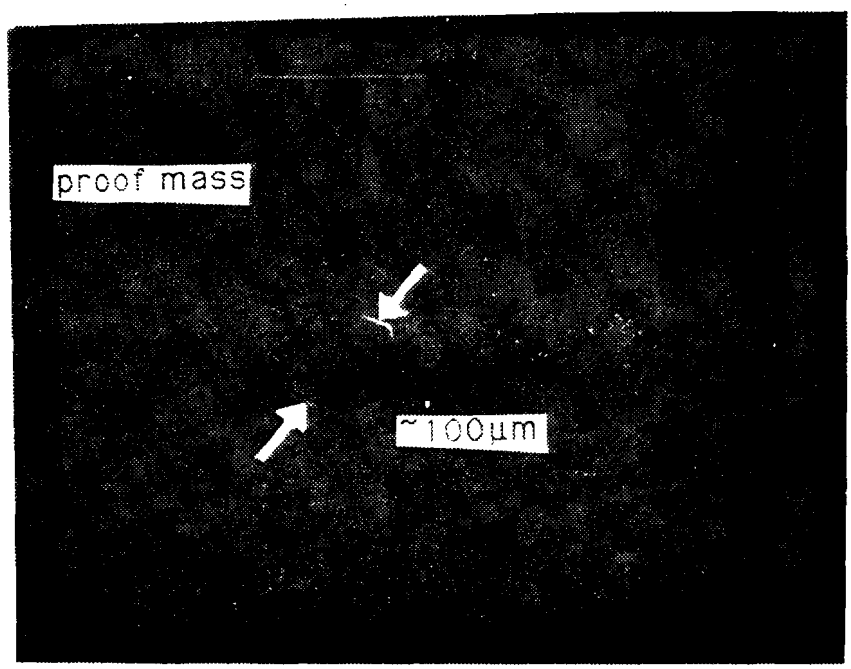
	KOH	N-Prop.	Vert. ER (μm/min)	Riv Undrcut (μm/μm)	Riv. Tip Undrcut (μm/μm)	Hask Dimensions dA (μm)	ST (μm)	Area (μm^2)
Experiment 1: Etching Under +/-5°C Variation								
Uncontrolled W#2 (p-type)	23.41% 47gm	13.34% 39ml	0.92	1.25	0.36	175.2	272.2	43397.8
Experiment 2: Etching Undrr +/-1°C Variation Using 2-Level Taguchi Technique								
RUN #1 W#EXP1-n5 (n-type)	23.41% 47gm	13.34% 39ml	0.97	0.70	0.26	46.5	116.5	11410.0
RUN #2 W#JCCM19 (n-type)	23.38% 48.2gm	15.00% 45ml	0.84	0.62	0.23	40.3	102.3	8841.2
RUN #3 W#JCCM18 (n-type)	33.00% 78.1gm	13.35% 46 ml	*0.98*	0.59	0.24	20.8	85.5	6877.6
RUN #4 W#JCCM20 (n-type)	33.03% 80.6gm	14.92% 53ml	0.88	0.59	0.23	28.8	90.8	7415.2

**Note: Water content in each run is 127ml.

Therefore, an actual accelerometer with Ccmask **EXP#1** was etched for 6 hours (at 80±1°C) to test Ccmask **#EXP1** in a solution with 63.25% H_2O, 13.34% n-propanol, and 23.41% KOH. Although the compensation mask was large enough to protect the corner from undercutting, it was found that the mask dimensions determined from the first experiment are larger than necessary as shown in the **SEM** photo, Figure 3.16. Notice that the left over rounded corners are at least 100μm in diameter.



(a)



(b)

Figure 3.16. (a) Back view of a 6-hour etched proof mass using Ccmask #EXP1 at 80±1°C; (b) An enlarged view of one comer in (a) proof mass.

Refemng to Table 3.3, the difference between the S_T value based on experiment 1 and that based on experiment 2 is on the same order. Therefore, since this experiment was performed under similar conditions as experiment 2 (run#1), except for the total etch time, the outcome shows that a reduced comer compensation mask can be used instead. Thus, a reduced comer compensation mask, based on experiment 2 (run#1), has been made; this mask will be called Ccmask #EXP2-1. Recall that lateral undercutting was found in experiment 3 in section 3.3 but not measured. Similar lateral undercuts were observed along the sides of the proof mass when Ccmask #EXP1 was tested. For a 6-hour etch of Ccmask #EXP1, the lateral etch rate is –0.08 μm/min. Thus, the alignment of the front side to the backside of the accelerometer must account for the lateral undercut of the etch from the backside. In short, Ccmask #EXP2-1, which is a reduced version of the first comer compensation mask, has been made and is currently being tested out in the next accelerometer fabrication.

IV. Purdue MELO Accelerometer (AP-1)

4.1. Design of MELO Accelerometer (AP-1)

The Purdue MELO Accelerometer (AP-1) fabrication process, including other electronic devices, consists of 9 masking steps as listed in Table 4.1. Each masking step and its design are described in this section. The design and layout of the Purdue MELO Accelerometer (AP-1) was accomplished with help of the Delco Electronics engineers.

Table 4.1. Ap-1 mask levels

Mask #1 - Alignment Marks after MELO step
Mask #2 - Seed Window Patterns for MELO Silicon
Mask #3 - Piezoresistor Pattern
Mask #4 - Base (in BJT device) Pattern
Mask #5 - Emitter (in BJT device) Pattern
Mask #6 - Metal Contact Pattern
Mask #7 - Metal Pattern
Mask #8 - Front Delineation for Bridges and Proof Mass
Mask #9 - Back Etch Pattern

The size of Purdue MELO Accelerometer (AP-1) is 3000 μm x 4000 μm including metal bonding pads. Its physical dimensions are similar to that of the SASD accelerometer fabricated by Delco Electronics. Also, the bridge dimensions (width, thickness, and length), proof mass size, and piezoresistors characteristics (junction depth, size, and sheet resistance) were designed to be of similar values. Such a design makes a comparative analysis with SASD accelerometer possible. The accelerometer was situated within a 7000 μm x 7000 μm (272 x 272 mil^2) die . The reason for sizing the die larger than the size of AP-1 is to allow the AP-1 to be mounted on the ASD accelerometer back-plate. AP-1 then can be tested by the same testing equipment used on the ASD accelerometer at Delco Electronics. The additional space on the AP-1 die allows the fabrication of other electronic devices such as resistors, diodes, BJT devices, capacitors, and gate-controlled diodes for evaluating the MELO silicon material quality as well as process procedures. The total layout of the AP-1 die is illustrated in Figure 4.1.

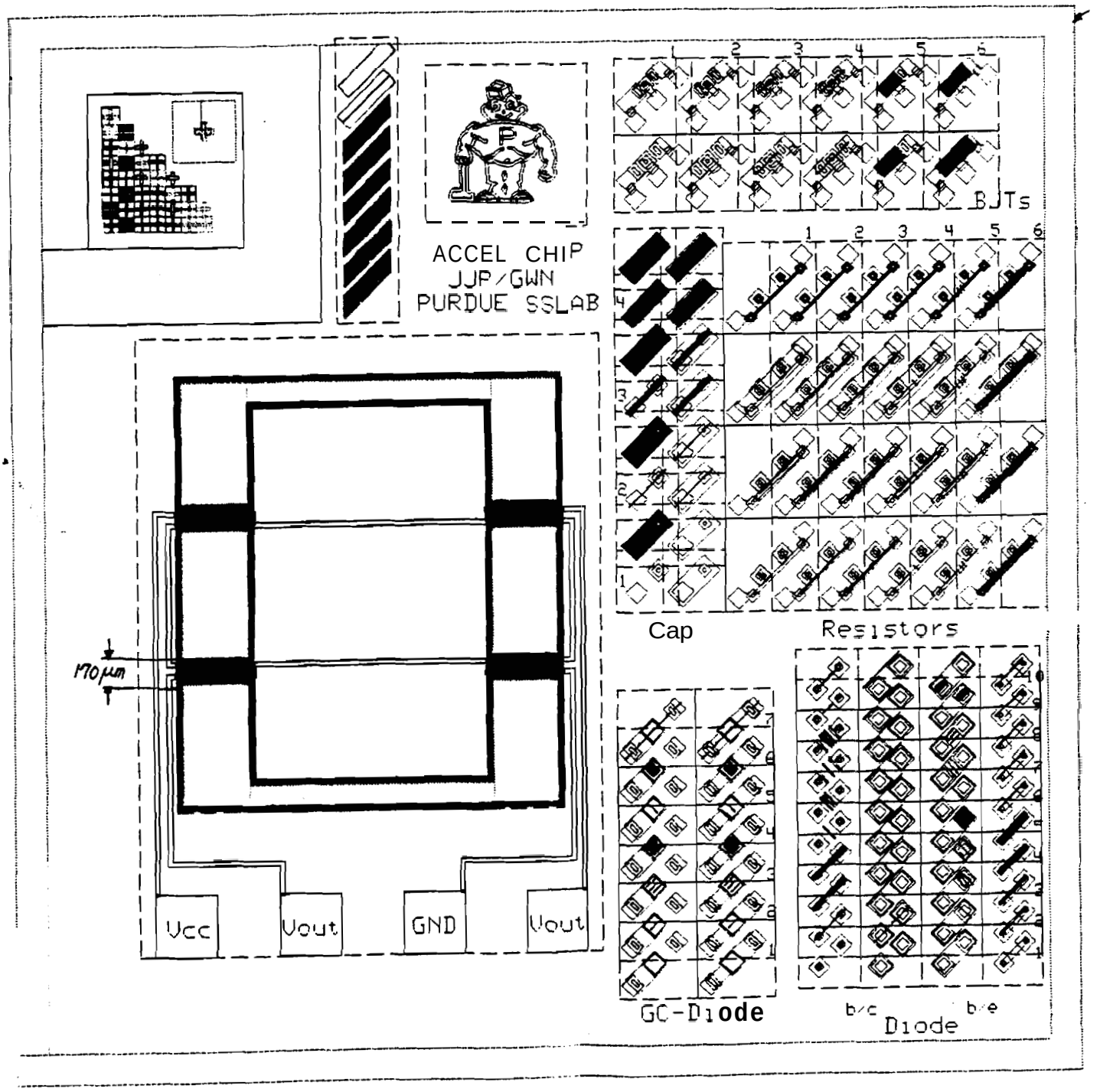


Figure 4.1. Layout of Purdue MELO accelerometer (AP-I) die. The die six is 7 x 7 mm^2 (272 x 272 mil^2) and accelerometer size is 3 x 4 mm^2. There are other

electronic devices, in addition to the accelerometer, for evaluating the MELO material and process procedures.

The MELO silicon for the bridge formation was formed surrounding the proof mass so that it allows more tolerance for masking steps and provides more mechanical strength until the bridges are defined by front delineation. The width of the silicon dioxide strips was determined as 5 μm and the space between them as 2 μm in order to work comfortably in the Purdue University Solid State Laboratory. Seed windows are aligned to the <100> direction for the best quality MELO silicon. The p-type piezoresistors are aligned to the <110> direction for their highest sensitivity; i.e. the most resistance change induced by the stress applied. The beam dimension was determined to be 10 μm thick, 200 μm long, and 40 μm wide, which is similar to the Delco's SASD version accelerometer.

Piezoresistors were designed to have a sheet resistance of 212 Ω/° and a junction depth of 1 μm. The general rule is to make the junction depth of the piezoresistors less than or equal to 10% of the silicon diaphragm thickness. Since the ion implant is done without an oxide buffer layer, the ion implant had to be done at the least possible energy available at Purdue University Solid State Laboratory, 25 KeV, in order to achieve a shallow junction depth. The resistance value of one resistor was determined such that the stress sensitivity of the piezoresistors is reasonably good while the temperature sensitivity is low. SUPREM III process simulator was employed to determine the ion implant dose and drive-in time for the desired junction depth and sheet resistance at 25 KeV. The dose of the boron as 1 x $10^{15}/cm^2$ and wet oxidation drive-in at 1000°C for 30min were selected. As shown in Figure 4.2, the peak carrier concentration and junction depth of a poezoresistor become 1 x $10^{19}/cm^3$ and 1.0 μm after 30 min drive-in. Its corresponding sheet resistance is 212 Ω/square and the resistance of each piezoresistor would be 3 kΩ since 15 squares were employed in one piezoresistor. The U-shape piezoresistors were selected for an easy metal connection and higher sensitivity as compared to the I-shape. The drive-in time was divided into two parts so that BJT devices can be fabricated at the same time.

The thickness of the thermal oxide mask for the boron and arsenic ion implant was also determined by SUPREM III process simulator. The value was chosen such that 95% of the implanted boron will be masked by the oxide. For the piezoresistors, the boron dose is 1 x $10^{15}/cm^2$ and 4000 Å of thermal oxide is necessary. By the same token, for 1 to 3 x $10^{13}/cm^2$ of base dose and 1 to 3 x $10^{15}/cm^2$ of emitter dose, 1500Å and 1000Å of thermal oxide are needed respectively. The first 15 min. drive-in for the piezoresistors was done with the base drive-in after both boron implant steps were completed and the next 15 min. drive-in was done with the arsenic drive-in. The collector contact region was patterned and implanted with the emitter with the same mask level (mask #5) so that an ohmic contact can

be made to the collector. The test devices were fabricated on SEG and MELO silicon and were tested for silicon material characterization. The number and location of the silicon dioxide strips under the MELO silicon are varied such that their effect on the device character can be analyzed.

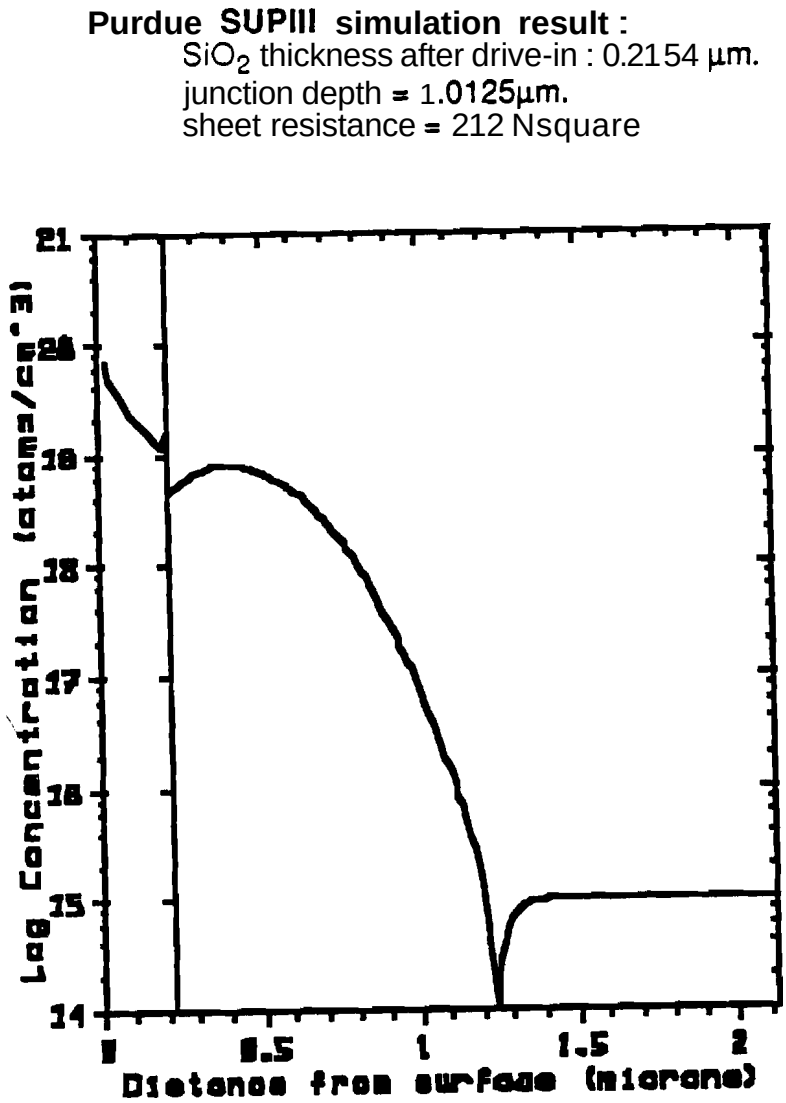


Figure 4.2. The SUPREM III output plot for determining the boron ion implant dose, energy, and drive-in parameters. The resulting junction depth and sheet resistance of a piezoresistor become 1.0μm and 212 Ω/square respectively.

After the emitter drive-in, the metal contact was defined (mask #6) and metal deposition was performed. Al-1%Si was deposited using a Perkin-Elmer Sputtering System at 100 Watts, 8 mTorr, for 30min, resulting in 2500Å thick metal. The effect of the metal deposition and the following processes for the passivation layer will be discussed later in this chapter in more detail. The metal is then patterned and annealed at 400°C for 20min. At this stage, the devices are ready to be tested but the accelerometer needs further processing steps.

The next step is the fabrication of a thin MELO silicon diaphragm by KOH back-etch. The front circuits and metal pattern need to be protected during a lengthy KOH etch. Here, neither LPCVD nitride nor thermal oxide can be used because their process temperature is much higher than the Aluminum melting point. Therefore, either plasma nitride or oxide was deposited on both sides of the wafer as a protection on the front side and as a mask on the back side. Passivation of the metal pattern turned out to be one of the most critical steps in fabricating successful accelerometers. The problems associated with metal passivation and their solutions are discussed in the following section.

The back-side etch windows were patterned (mask #9) for KOH etch using a thick (–6pm) A24620 photoresist as a mask. They can be patterned by reactive ion etch, BHF wet etch, or combination of both. The front side was also protected by a thick (–6pm) AZ4620 photoresist while patterning the back side. It is important to pattern the etch windows without damaging other passivation areas since the damage on the passivation layer would be attacked during a long KOH etch, resulting in the etched metal and silicon. It is also important to remove the nimde or oxide layer completely from the patterned area for a uniform KOH etch over a wafer. If a thin nitride/oxide layer is left in some patterns, then it will cause a considerable non-uniform etch over a wafer. Also additional KOH etching time is required for removing the layer. This longer etch time will enlarge the etch window by having more lateral undercut and result in a low yield.

The front side wafer delineation can be done either before KOH back etch or after. With the first version of the AP-1 design, the front delineation was to be done before KOH etching because KOH etching was determined to be the very last step in order to avoid any further lithography steps due to the weakness of the thin silicon diaphragm. However, by attaching the accelerometer wafer, after KOH etch, to another back plate wafer it became possible to have an additional lithography step due to its enhanced mechanical strength. Therefore, the front delineation after KOH etch became possible as well.

4.2. Metal Passivation in KOH etch

Front-side passivation of Al-Si, during 6-hour long back-side KOH etch, turned out to be one of the critical steps in fabricating MELO accelerometer successfully. The strength and durability of the passivating layer depend on the metal deposition, metal pattern, surface cleaning, passivating material and its thickness, etching solution, and the etching temperature. A series of experiments were performed in order to improve the metal (Al-Si) passivation and the etching results are described in this section.

(a) AI-Si Lift-off vs. Wet Etch

It has been known that the metal lift-off procedure can cause sharp spikes at the metal edges when the lithography is not done carefully. Nevertheless, Al-Si lift-off procedure has been preferred in some applications over wet etching for metal pattern definition because of its simplicity. In addition, Al-Si passivation was usually not required for research level device fabrication since the device is fabricated and tested only for its characterization, not packaged and then put into a system. The devices on a wafer or a die can be tested on a probe station regardless of the possible existence of the spikes at the Al-Si testing pad edges. Therefore, the importance of avoiding the spikes at the AI-Si edges and difficultiesof Al-Si metal passivation were not realized until a complete accelerometer was fabricated.

Metal lift-off is normally performed by soaking the metal deposited wafer in acetone until the underlying photoresist gets desolved and the top unwanted metal is lifted off leaving a metal pattern. In order to speed up the process, the wafer is sometime placed in the ultrasonic cleaner (USC). This USC treatment turned out to make the spikes even worse because it breaks the Al-Si edges more abruptly than that of simple acetone soaking. The USC process also can produce small particulates of the lifted Al-Si and these particulates can cause micrometer range bumps by sticking on the patterned Al-Si surface as shown in a SEM photograph (Figure 4.3). Figure 4.4 (a) illustrates the Al-Si metal surface roughness at the edge as well as on the metal layer caused by lift-off process even after plasma nitride/oxide deposition. The measurement was performed by Tencor Alpha-step surface profilometer after Al-Si sputter deposition at 8 mTorr (with the starting base pressure of 3×10^{-7} Torr) on the patterned photoresist, lift-off, and plasma oxide/nitride deposition. Unfortunately, these spikes caused by the Al-Si lift-off process continue to maintain their sharpness even after a thick passivation layer deposition. Figure 4.4 (b)

illustrates a 1 μm high spike on the Al-Si metal layer after passivation layer deposition. Their height could be as high as several micrometers.

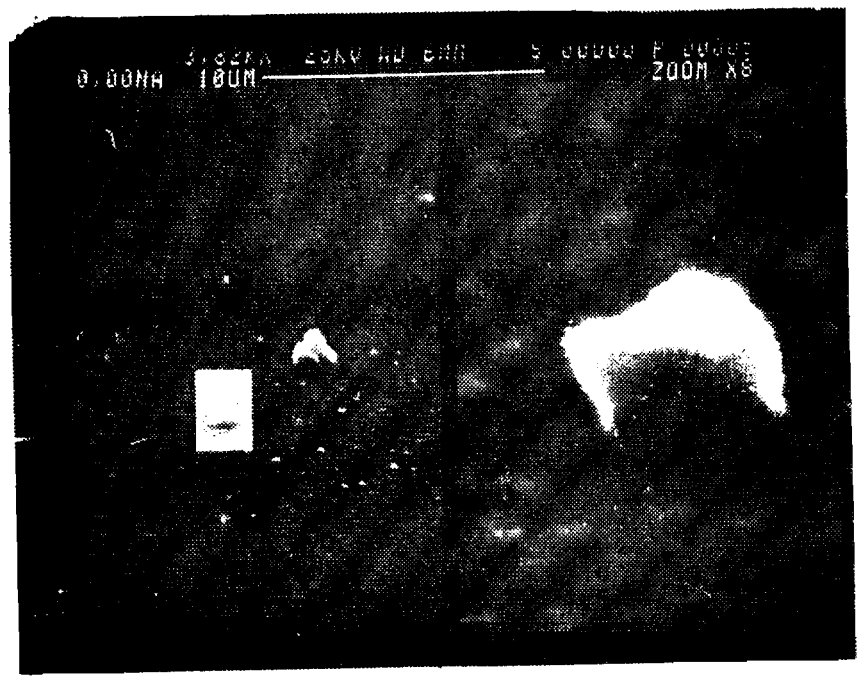
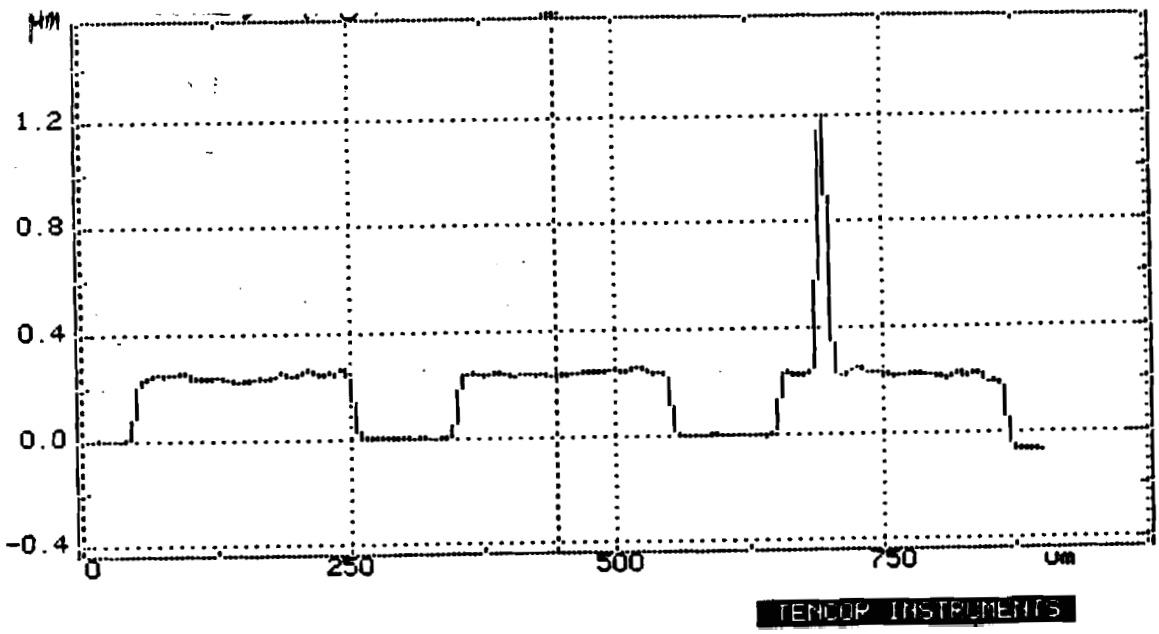


Figure 4.3. A SEM photograph of Al-Si particulates sitting on the metal layer after lift-off.

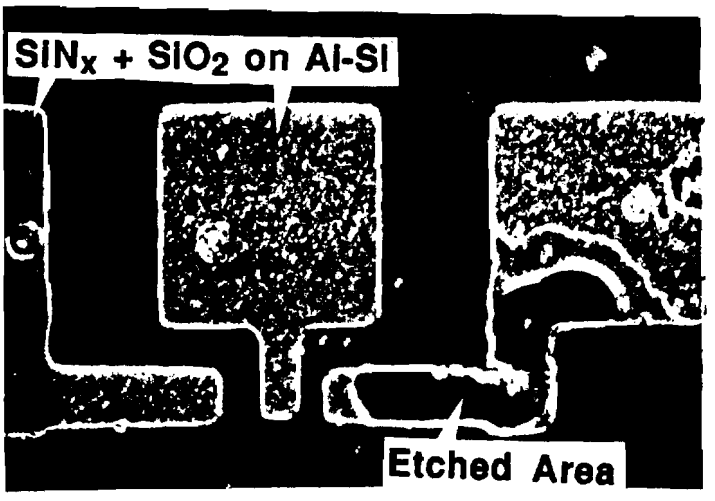
(a)



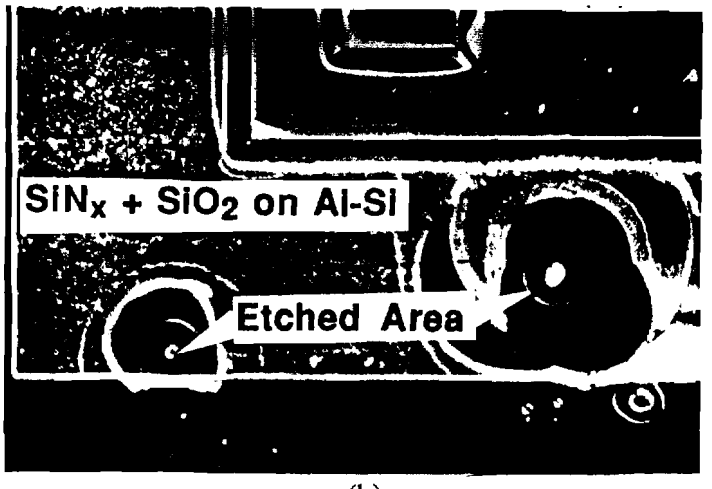
(b)

Figure 4.4. Al-Si Metal spikes caused by a lift-off process. After Al-Si sputter deposition at 3 x 10-7 Torr, lift-off, plasma oxide deposition, and plasma nitride deposition. (a) spikes on the metal layer as well as at the edge. (b) 1 pm size spike.

Even when the spikes are covered by the passivation layer, they are not covered conformally and a break-through can occur from the side of the spikes faster than on the passivated surface. In this case, during KOH etch, the weaker passivation layer was damaged by the KOH etch solution and Al-Si became exposed. Once the Al-Si is exposed to KOH etch solution through the the damaged passivation layer, Al-Si is then etched rather fast by the KOH etch solution. Figure 4.5 illustrates couple of examples of the etched Al-Si metal pattern by KOH etch solution after deposition of plasma oxide and nitride as passivation layers. Therefore, Al-Si wet etchin was employed instead of lift-off.



(a)



(b)

Figure 4.5. Example of the etched Al-Si metal layer by 15 min KOH etch after passivation. (a) etch starting from a comer. (b) etch starting from an metal edge as well as from the top.

(b) Chamber Base Pressure Before Al-Si Deposition

The original quality of the sputter deposited Al-Si is important as it is related to the degradation of the passivation layer. Previously Al-Si was deposited by sputtering the Al-Si source target at 8 mTorr with a base pressure of $3x1V^{7}$ Torr and the deposited Al-Si was good enough for electrical testing of the devices. Argon gas was used for making a plasma. However, Al-Si deposited at the above condition resulted in a rough surface and later caused a degradation of the passivation layer. Whereas sputtering of the AI-Si layer at lower base pressures ($< 2x10^{-7}$ Torr) yielded a better, very smooth and shinny surface which made the subsequent passivation layer hold much longer during KOH etch using the same passivation layers. Therefore, the Al-Si deposition base pressure was set as low as possible and a pressure near $2x10^{-7}$ Torr was usually obtained. Table 4.2 shows an improvement in yielding good accelerometer dies with a lower base pressure of the Al-Si deposition chamber.

Table 4.2. Number of good MELO accelerometer dies after 5-hour KOH etch with different Al-Si deposition pressure and different passivation layers for comparison.

Sputter Deposit Base Pressure (Torr)	Single PECVD SiN_x (about 3 μm)	PECVD $SiN_x/SiO_x/SiN_x$ (2μm/1μm/0.7μm)
2 x 10 -7	10 out of 26	40-47 out of 50
3 x 10 -7	< 15 out of 50	< 25 out of 50

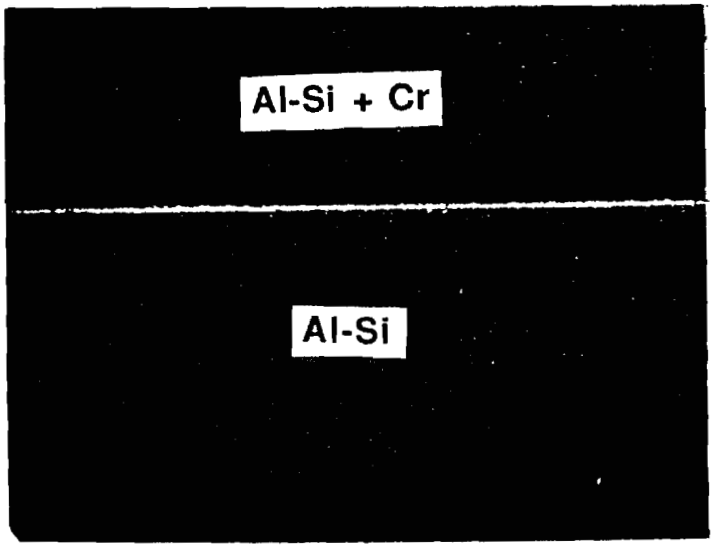
As illustrated in Table 4.2, the lower base pressure in the Al-Si deposition chamber improved the accelerometer fabrication yield considerably. Even though the number (from $3x10^{-7}$ Torr to $2x10^{-7}$ Torr) doesn't seem to indicate a big difference in the pressure, the lowering of the base pressure takes 8 to 10 hours of extra pumping time. This longer pumping would remove the water and oxygen contents from the sputtering chamber, hence the quality of the deposited Al-Si metal improved with this lower base pressure. Degradation of the Al-Si layer deposited at near $3x1V^{7}$ Torr became obvious after the Al-Si annealing at 400°C which is a moderately high temperature processe. In fact, this annealing process have participated in making the Al-Si metal surface rough and resulting in a degradation of the passivation layer during KOH etch. However, a very recent surface measurement of the Al-Si layer deposited at $2.2x10^{-7}$ Torr followed by annealing at 400°C

for 20 min. revealed that the surface does not become very rough after the annealing step. Therefore, the original Al-Si layer quality from the deposition seems to play the main role to the surface roughness more than the following annealing step.

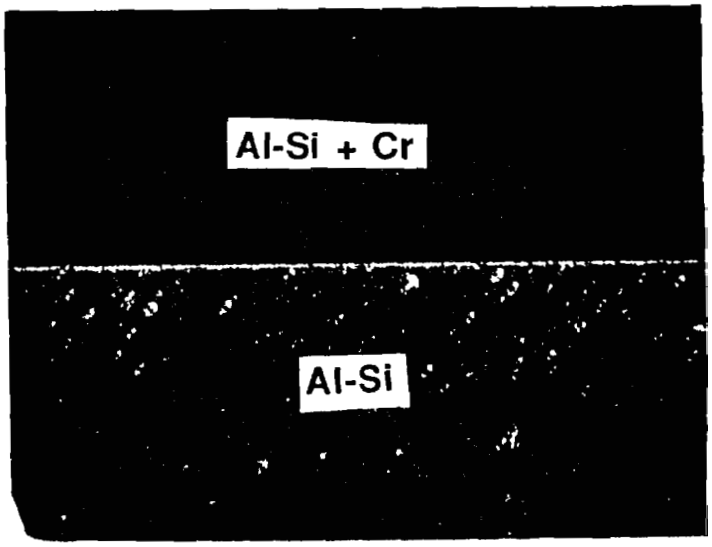
(c) Al-Si + Chrome Double Metal Layer

Al-Si deposited with the base pressure of $3x10^{-7}$ Torr, which was the typical base pressure, seemed very difficult to passivate with plasma oxide or nitride in the early stages. Chrome(Cr) was employed to examine if the passivation could be improved since Chrome has been known to give a smoother surface than Al-Si. Figure 4.6 shows the different smoothness between Al-Si layer and Al-Si+Cr layer. Particularly, after plasma oxide deposition the Al-Si surface clearly became rougher than the Chrome surface deposited over the Al-Si layer as shown in Figure 4.6 (b). Since Cr has a smoother surface, it was protected better with the same passivation layer than Al-Si in a KOH etch solution. However, Al-Si was not replaced by Cr because of the following reasons. First, Cr is known to make a poor ohmic contact with the silicon substrate and hence only used as a gate metal for MOSFET devices instead of contact metal. Secondly, Cr is known to have a higher resistance than Al-Si with a metal path, which is the case with MELO accelerometer layout. At last, it was difficult to bond Al wire on the Cr bonding pad. Therefore, Cr could not be used as a metal layer but as a protection layer on Al-Si during the KOH etch.

Next, Cr was employed for covering the Al-Si pattern. Al-Si and Cr were deposited consecutively and patterned with a negative photoresist for a wet etch process. Then Cr and Al-Si were etched in that order for patterning, resulting in the structure shown in Figure 4.7 (a). Cr on the Al-Si layer can be easily removed by a wet Cr etch without damaging the underneath Al-Si layer after the KOH back etchis finished. However, Cr deposited on the Al-Si and patterned using the same mask did not have perfect coverage and any exposed Al-Si, particularly at edges, was attacked by KOH etch. Figure 4.7 (b) is a picture the Al-Si layer covered by the identically patterned Cr layer with the plasma nitride passivation layer on it. Figure 4.7 (c) shows the Al-Si layer being etched by KOH etch solution starting from the edge.

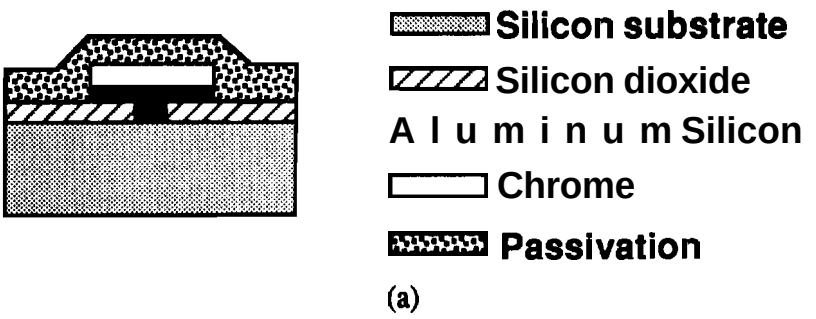


(a)

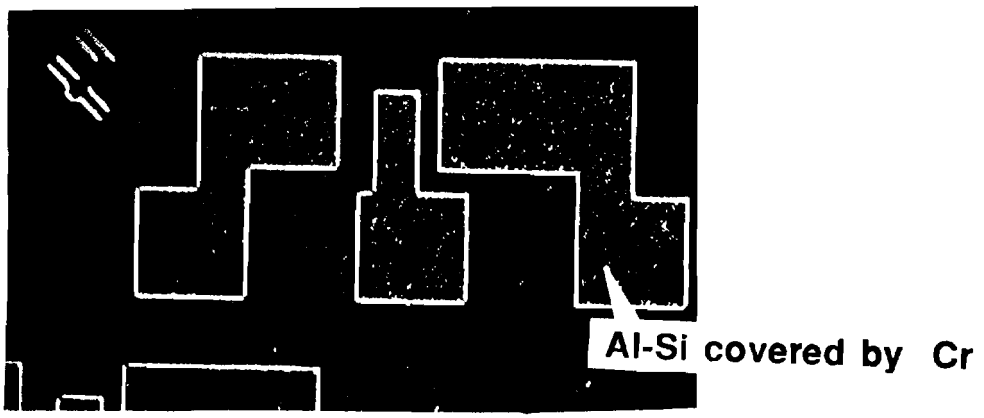


(b)

Figure 4.6. Comparison of Al-Si and Al-Si + Chrome metal layer. (a) Before plasma oxide deposition. (b) After plasma oxide deposition.



(a)



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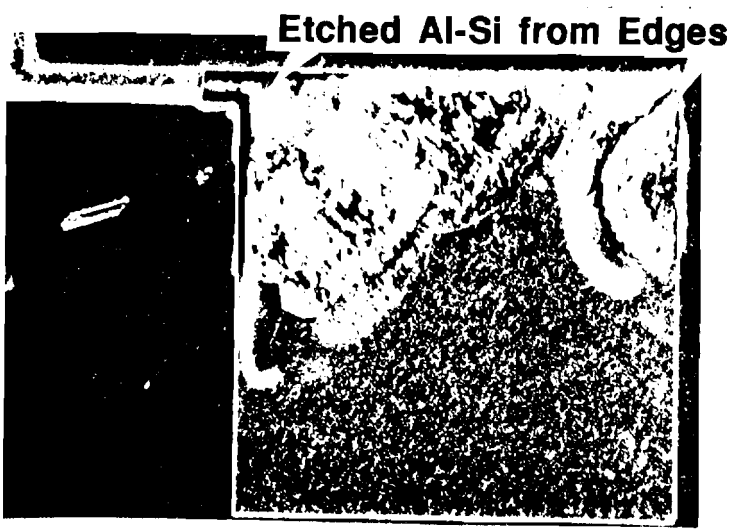


(c)

Figure 4.7. Al-Si plus Chrome double metal layer with identical dimension. (a) A cross section diagram. (b) Al-Si and Chrome are deposited and patterned together. (c) Al-Si exposed at the edge gets etched by KOH etch.

A slight modification in the mask, by making the Cr patter slightly larger than Al-Si pattern, will resolve the exposed Al-Si edge by covering the Al-Si edges better. With the identical mask, Al-Si edge coverage was med by patterning Al-Si and overetching Al-Si to make it narrower followed by depositing and patterning Chrome. Figure 4.8 (a) depicts the cross section diagram of the resulting structure. This method somewhat improved the Al-Si coverage but it was difficult to cover all the Al-Si edges without losing the original Al-Si dimension considerably. Figure 4.8 (b) and (c) show the top view of this structure where most of Al-Si was covered by Cr except one edge. After a long KOH back etch, some of the uncovered Al-Si edges were etched and it depends on the alignment error.

After a smooth and shinny Al-Si deposition was achieved by depositing Al-Si with a lower base chamber pressure, around $2x10^{-7}$ Torr, Cr was not required any more. If Al-Si is still not protected by a passivating layer, a Cr protecting layer can be added in the process. In this case, Cr can be deposited over the patterned Al-Si on the whole front side of a wafer, without being patterned, and passivation layer can then be deposited. This will not only protect the surface better but also provides more mechanical strength after the KOH back-etch is completed.

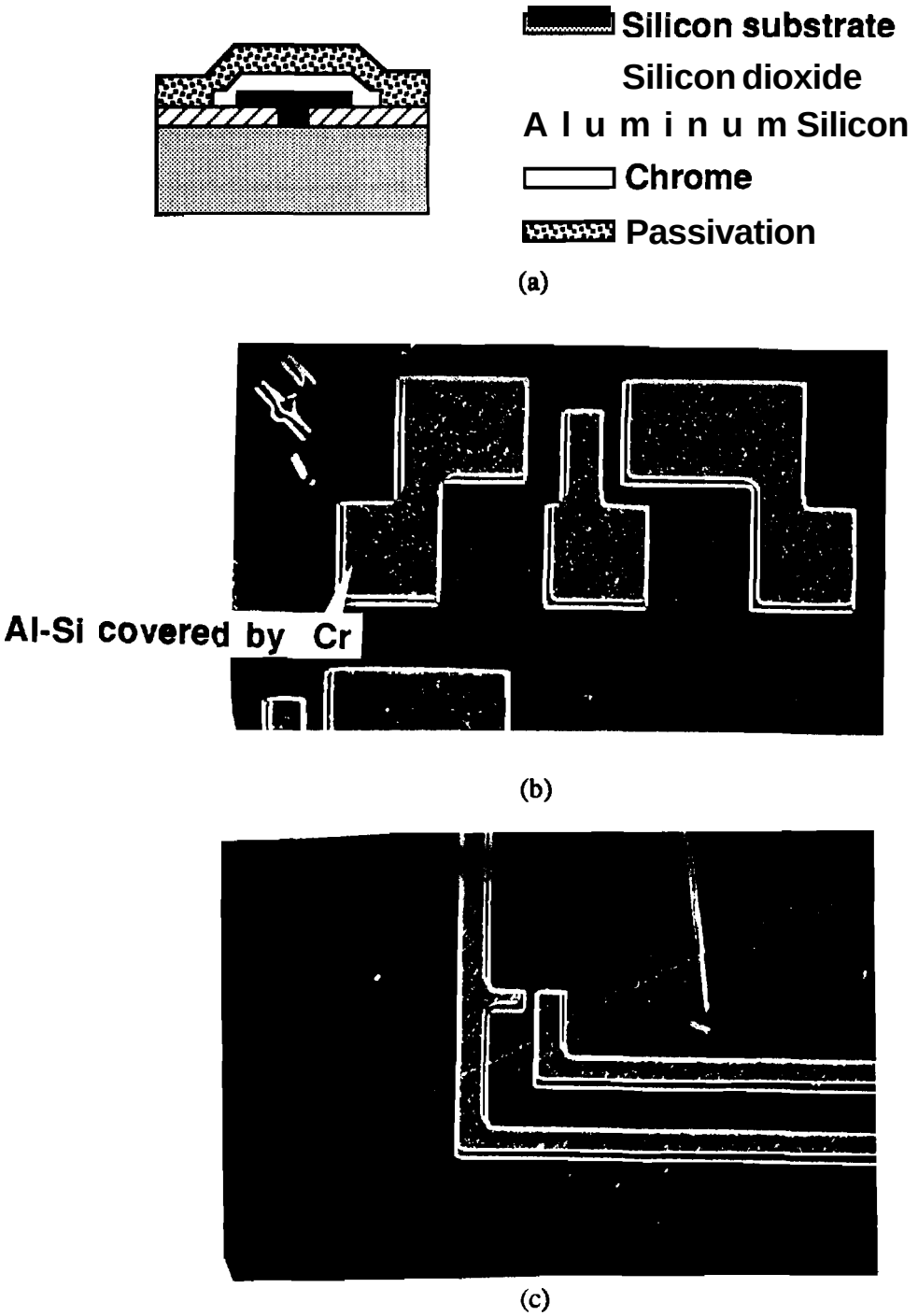


Figure 4.8. Al-Si plus Chrome double metal layer in which Al-Si is deposited and patterned by overetching first then Chrome is deposited and patterned. (a) A cross section diagram. (b),(c) A top view showing that most edges were covered by Cr layer except one direction.

(d) PECVD vs. LPCVD

From the previous etching experiments without deposited Al-Si, silicon nitride deposited by low pressure chemical vapor deposition (LPCVD) at 800°C served 8s the best passivation layer with a minimum lateral undercut. Also, LPCVD nitride can be deposited more conformally and hence should be able to protect the metal edge better than PECVD nitride. However, LPCVD nitride can't be used with Al-Si due to its high temperature requirement. Alternative passivation layers at low temperature are silicon nitride/oxide (SiN_x/SiO_x) deposited by plasma enhanced chemical vapor deposition (PECVD). The low temperature process required for the passivation layer is due to the the choice of the metal, Al-Si, which is easily available and goad for silicon IC processing. Due to the difficulties of the Al-Si passivation during silicon micromachining, many researchers tried to employ different metals such as gold, molybdenum, titanium, or silicided metal. Gold is quite a stable metal in anisotropic etching solution and other metals can survive at higher temperature, like 800°C, so that LPCVD nitride can be used as a passivation layer. Table 4.3 shows the differences between PECVD and LPCVD nitride film characteristics.

Table 4.3. Comparison of PECVD and LPCVD nitride film characteristics.

	PECVD Nitride	LPCVD Nitride
Deposition Temperature	~ 300 °C	~ 750 °C
Surface Coverage	Less Conformal	Conformal
Required Thickness	≥ 2 μm	~ 0.2 μm
Cracks appear	≥ 3 μm	≥ 0.4 μm
Lateral Undercut	more than LPCVD	small

As shown in Figure 4.6(b), Al-Si metal layer seemed to react with gases during PECVD oxide deposition resulting the rough Al-Si surface and degradation of the oxide. It is not clear how and why the PECVD oxidation reacts with the Al-Si layer to degrade the passivating layer and will need more experiments to confirm the results. Therefore, PECVD nitride, instead of oxide, was deposited on the Al-Si layer as the first passivation layer. A thick (> 3 μm) PECVD nitride seemed to work quite well as shown in Table 4.2. However, too thick of a passivation film applies stress to the silicon wafer and may result in cracking during the KOH etch. Therefore, PECVD $SiN_x/SiO_x/SiN_x$ multiple layer was

applied instead of one thick passivation layer so that PECVD oxide can act as stress relief material between the nitride sandwich. According to the results in Table 4.2, the multiple layer seems to work the best thus far, but the whole deposition takes a much longer time than a single passivation layer deposition because the PECVD chamber and electrodes need to be cleaned before subsequent deposition.

(e) Cleaning of the Wafer and PECVD System

Cleaning the wafer is very important throughout the whole fabrication process because an uncleaned surface will cause an unxpected roughness, resulting in degradation of the passivation layer during a KOH etch. Cleaning the surface after every lithography step, patterning, and etching should be done with much care. Piranha ($1H_2SO_4 + 1H_2O_2$) cleaning is one of the best methods for cleaning the wafer during the device fabrication. However, it can't be used after Al-Si depotition because it attacks the Al-Si layer. After the metal layer ia patterned by wet etch, the negative photoresist can not be removed by acetone (ACE) rinse. It can be removed by warm Nophenol followed by rinsing in tetrachloroethane (TCA), ACE, methanol (METH). During this rinse, Nophenol needs to be cleaned thoroughly from the wafer front to achieve a clean surface before depositing a passivation layer. When Nophenol is exposed to water, it will make foam and may leave some residue even after a long rinsing with deionized (DI) water. Any residue before depositing a passivation layer can cause a dagradation of the passivation layer. Cleaning the wafer and apparatus is also important because KOH etch is sensitive to the cleanness of them. After depositing PECVD nitride and patterning back etch window, cleaning with piranha was avoided in order to minimize any possible damage to the surface of the passivation layer. The wafer was cleaned only by soaking in solvents. This might contribute to generating pyramids on the back of the etched diaphragm after the KOH etch since KOH etch is quite sensitive to the cleanness.

PECVD chamber must also be cleaned very well in order to obtain a stoichiometric plasma nitride passivation layer without many defects. Typically, PECVD deposition chamber is cleaned by $CF_4 + O_2$ plasma etch after each deposition run. However, $CF_4 + O_2$ plasma etch is not enough to remove the residue from the electrodes and sometimes scrubbing the electrodes is necessary particularly to remove the carbon deposited during $CF_4 + O_2$ plasma etch. Scrubbing the electrodes and wiping the electrodes with solvents improved the PECVD nitride quality as a passivation layer.

4.4. Front Delineation and final structure

Two different methods were tried for passivation and front delineation. The first design was made such that all lithography steps would be completed before KOH back-side etching. Figure 4.9 (a) illustrates the cross section diagram of the structure just before the front delineation is performed. In this first design, a PECVD oxide layer was deposited on the front side and patterned using the front delineation mask (mask #8) after Al-Si metal patterning. Then a PECVD nitride layer was deposited on both sides of the wafer. While protecting the front nitride with a thick photoresist, the back etch pattern was defined. When the back-etch was completed using KOH, the wafer was placed in the reactive ion etch (RIE) chamber for the front delineation.

As the front PECVD nitride is etched away, the patterned PECVD oxide is exposed and used as a mask while etching silicon for front delineation. The etch rate of, PECVD oxide, PECVD nitride, and silicon with sulfur hexafluoride (SF_6) at 500watts was found to be 0.02μm/min, 0.1μm/min, and 0.5μm/min respectively. The PECVD oxide thickness can be optimized such that top Al-Si bonding pads will be exposed when the silicon etching is completed. If the PECVD oxide is thicker than desired and left after front delineation, then it can be etched with a BHF wet etch. This way, when the back-etch is done, the front delineation can be completed without any further lithography process. Therefore, no photolithography step was allowed after the thin silicon diaphragm was fabricated since the thin diaphragm can be easily damaged. However, with this design some accelerometers were damaged during KOH etch because of the thick steps introduced by the patterned PECVD oxide and nitride passivation was not thick enough to protect sides of those steps. The PECVD nitride deposited after patterning the oxide became weak at those steps and was etched during a long back-side KOH etch. This design would work better if the oxide step was reduced.

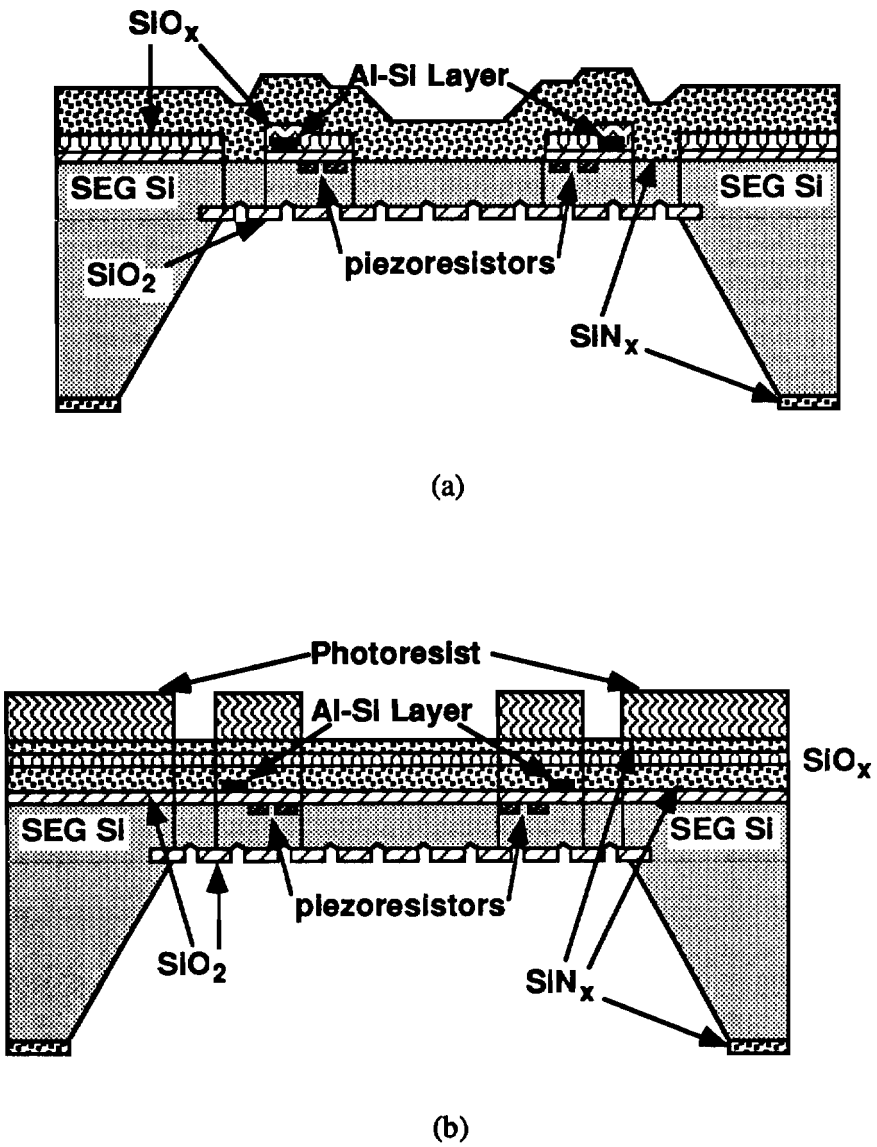


Figure 4.9. Cross section diagram of two different approaches for the front delineation. (a) Front delineation is patterned on PECVD oxide before the KOH back etch. No lithography step is performed after the KOH etch. (b) KOH etch is performed followed by a front lithography step for the front delineation.

The second method is to perform the back-side **KOH** etch before the front delineation. Figure 4.9 (b) shows the cross section diagram when the wafer is reasy for the front delineation. In this approach, triple layers of PECVD nitride/oxide/nitride was consecutively deposited on the front of the wafer after the metal was patterned. Without patterning the front layer, the back of the wafer was passivated and patterned for **KOH** etch. When the **KOH** etch was completed, the wafer was then attached to a back-plate wafer for a mechanical support. With the back plate wafer attached, the accelerometer wafer can proceed photolithography steps even though it still requires much care.

Triple layers of PECVD nitride/oxide/nitride were then etched by RIE using SF_6 before the front delineation lithography. The front delineation was patterned with a thick (AZ4620) photoresist such that the photoresist can be used as a mask during front delineation by RIE using SF_6. After the front delineation is completed, the photoresist on the top can be removed by a plasma ash without damaging the wafer. The front lithography worked quite well with the back plate wafer intact and the front delineation was successful as long as the top photoresist stays intact during the front delineation by RIE. The front lithography can still avoided if the PECVD oxide can be patterned after the first nitride deposition (Figure 4.8 (b)) and it will be tried in the near future.

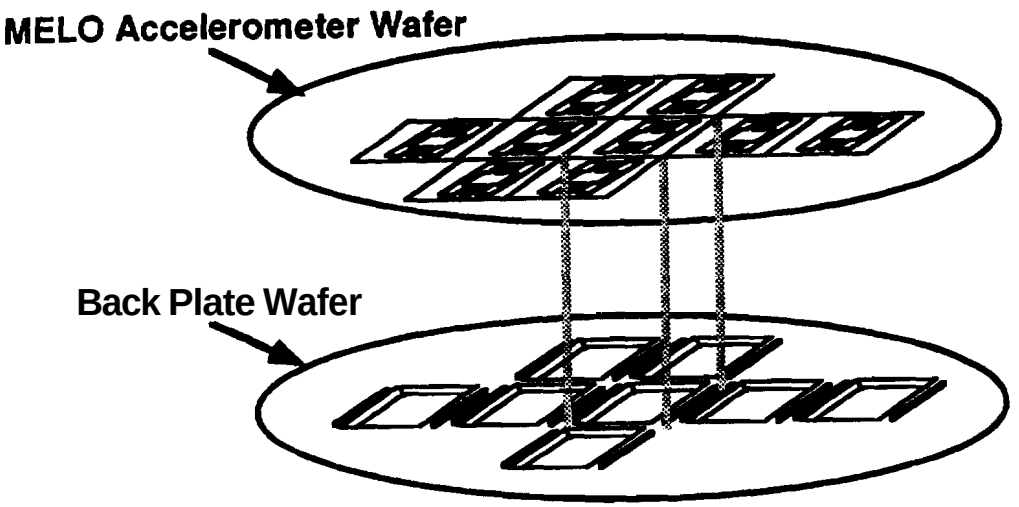


Figure 4.10. A schematic picture showing MELO accelerometer (AP-1) wafer is attached on the Delco Electronics ASD back-plate.

4.5. Testing of MELO Accelerometer (AP-1)

Once the front delineation was completed, the wafer was removed from the back plate wafer and attached on the Delco's 4" back plate wafer for testing as shown in Figure 4.10. Delco's back plate has a pattern of basins aligned for each die to limit the movement of the accelerometer proof mass. The wafer was then cut into dies along the die border and each die was packaged and bonded with aluminum wire. The package was placed on the testing station for the electrical output (DC and AC analysis) with respect to the applied acceleration.

A set of 12 completed accelerometers were delivered for testing in 1991. The testing results revealed that the design needed to be modified. There were two major reasons. First, the lateral undercut of the PECVD nitride was considerably more than expected in the initial design. Therefore, back etch window became wider than the original design and the <111> sidewall planes intersected on SEG silicon outside of the SiO_2 etch-stop area . This caused the exposed SEG silicon around SiO_2 etch-stop area to be etched through while MELO diaphragm was protected perfectly by SiO_2/V-groove etch-stop. Figure 4.11 is a SEM photograph of the back of the MELO silicon diaphragm where SEG silicon was exposed due to the overetched PECVD nitride back-etch mask. The back-etch window was aligned to <110> direction and the ending <111> sidewall was supposed to form and intersect on the SiO_2/V-groove etch-stop area. However, <111> sidewall intersected on the SEG area out of the etch-stop area and the exposed SEG silicon was etched when the etch continued. Particularly when the exposed SEG silicon occurred on a part of the accelerometer bridge, the whole accelerometer was ruined because of a broken bridge, hence the electrical output could not be obtained. Therefore, in the second design, the excess lateral etch was taken into account and more tolerance to the wafer thickness variation was designed into the mask #9.

Secondly, during the front delineation, SF_6 RIE etches isotropically vertically and laterally and therefore changed the bridge width and length. The longer the RIE is, the more lateral etch occurs. When the beam width became narrower, due to lateral etch by SF_6 RIE, the piezoresistors and the Al-Si metal line on the bridges were attacked. Also, when the beams became longer than desired, the stress distribution changed substantially and the concentration of the stress shifted away from the piezoresistors. Figure 4.12 shows the problems with the first design and the better results with the second design. Figure 4.12 (a) clearly shows that the piezoresistor is out of the beam end line where the most stress would

be induced. Figure **4.12** (b) shows that the middle of the piezoresistor is aligned to the beam end line.

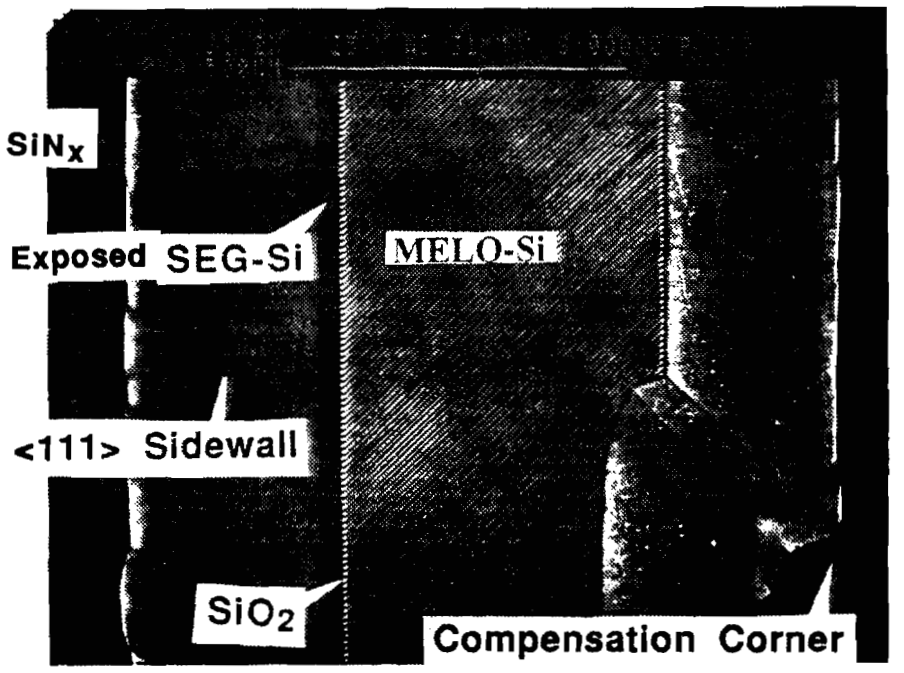
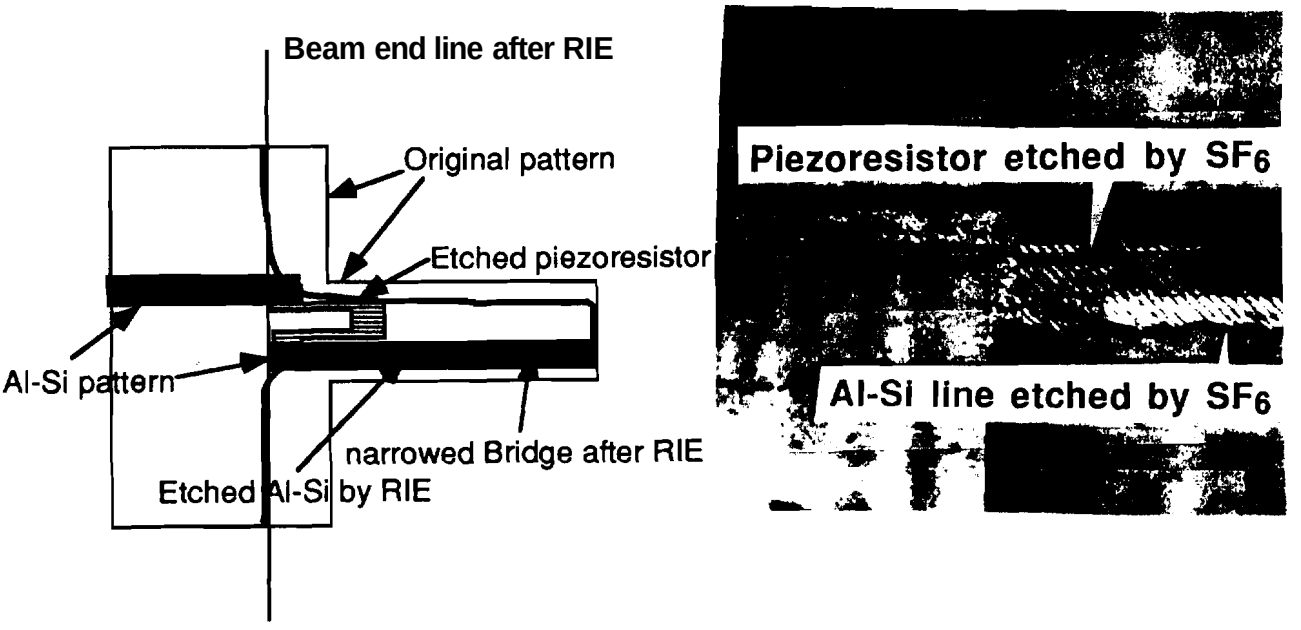
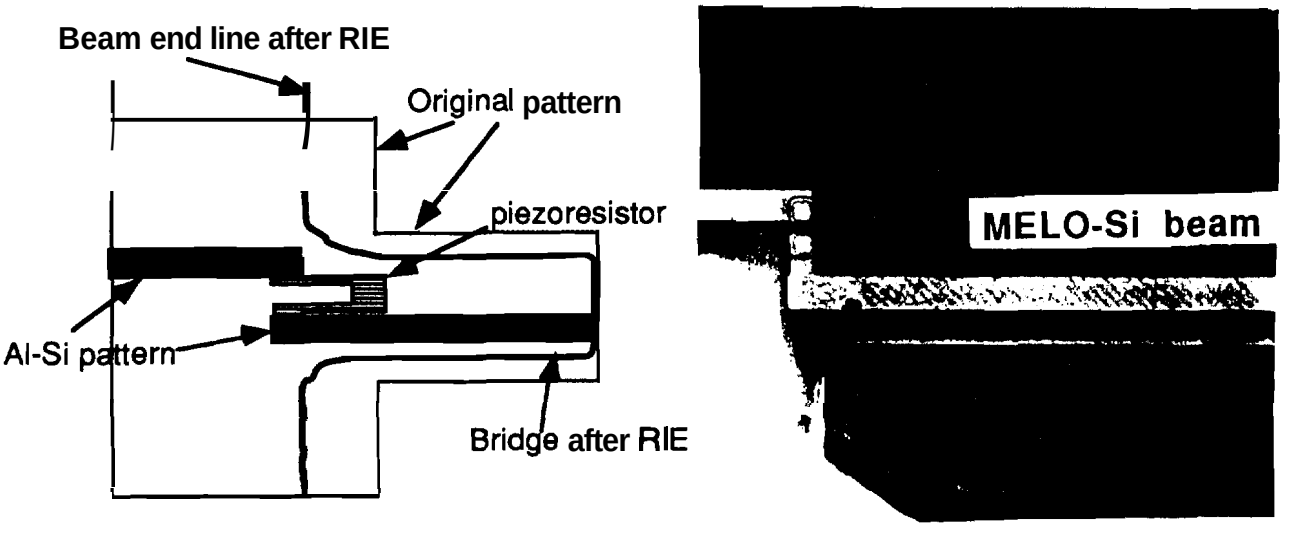


Figure **4.11.** A SEM photograph of the back of the MELO silicon diaphragm. An excessive lateral undercut of the **PECVD** nitride in the initial design caused the <111> side wall to intersect on the SEG region out of the SiO_2 area



(a)



(b)

Figure 4.12. Comparison of the first and second design in the AP-1 bridge structure. (a) A schematic diagram and photograph of first design showing excessive lateral etch by RIE using SF_6. (b) A schematic diagram and photograph of second design showing the improvement after RIE using SF_6.

Figure **4.13** shows the crack that occurred parallel to the line where <111> back-side etch plane intersected on the top {100} surface. This problem was resolved by reducing the front delineation pattern window dimension (mask #8).

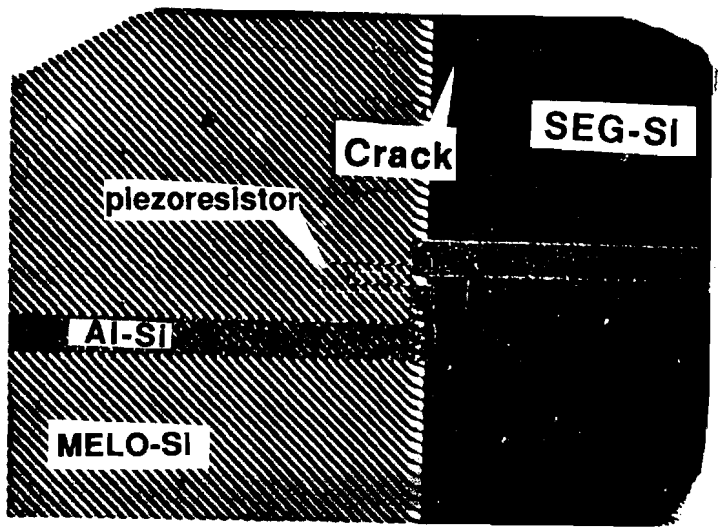


Figure **4.13.** A photograph showing the crack occurred on the top SEG area due to the excessive lateral etching during the KOH back etch which made <111> side wall intersect with the SEG area out of SiO_2 area.

Another possible cause of the low yields in accelerometer fabrication was the crack on the MELO silicon diaphragm due to the thermomechanical stress from the thick passivation layer during the KOH back etch (Figure **4.14** (a)). This can be reduced by making the front passivation layer thinner. Having Chrome on the surface may enable thinning the passivation layer since the Chrome makes the front surface smoother, protects the underneath patterned Al-Si, and provides additional mechanical strength after KOH back etching.

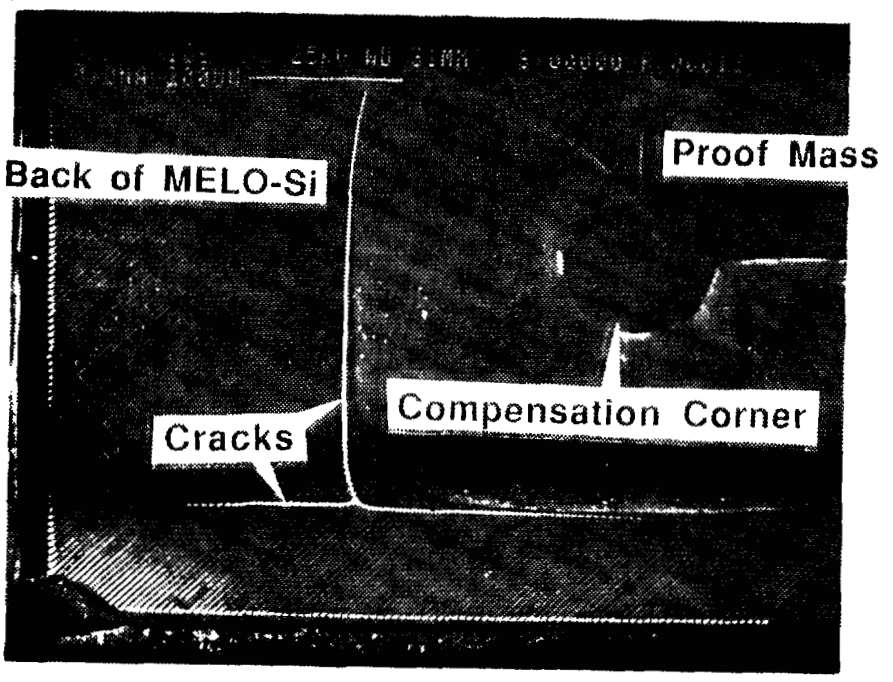
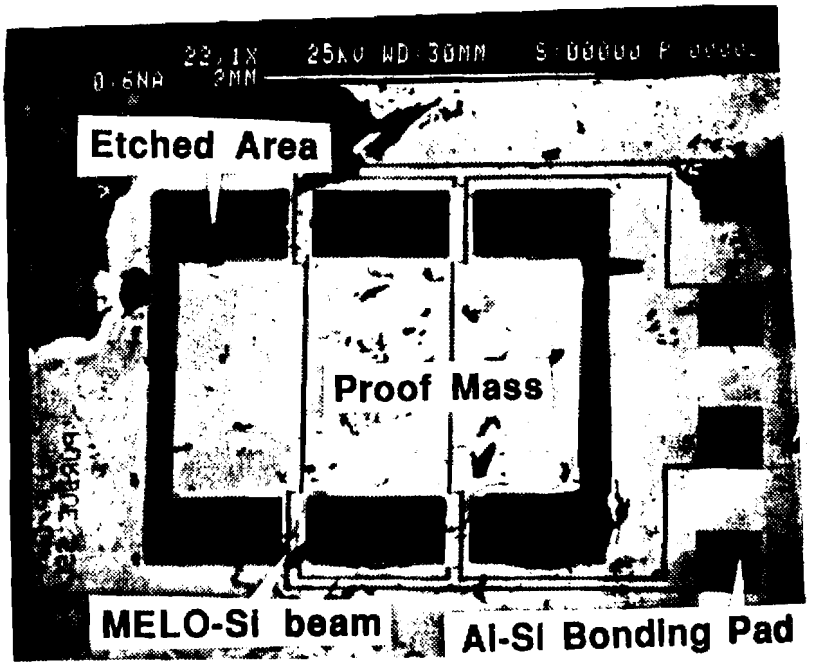


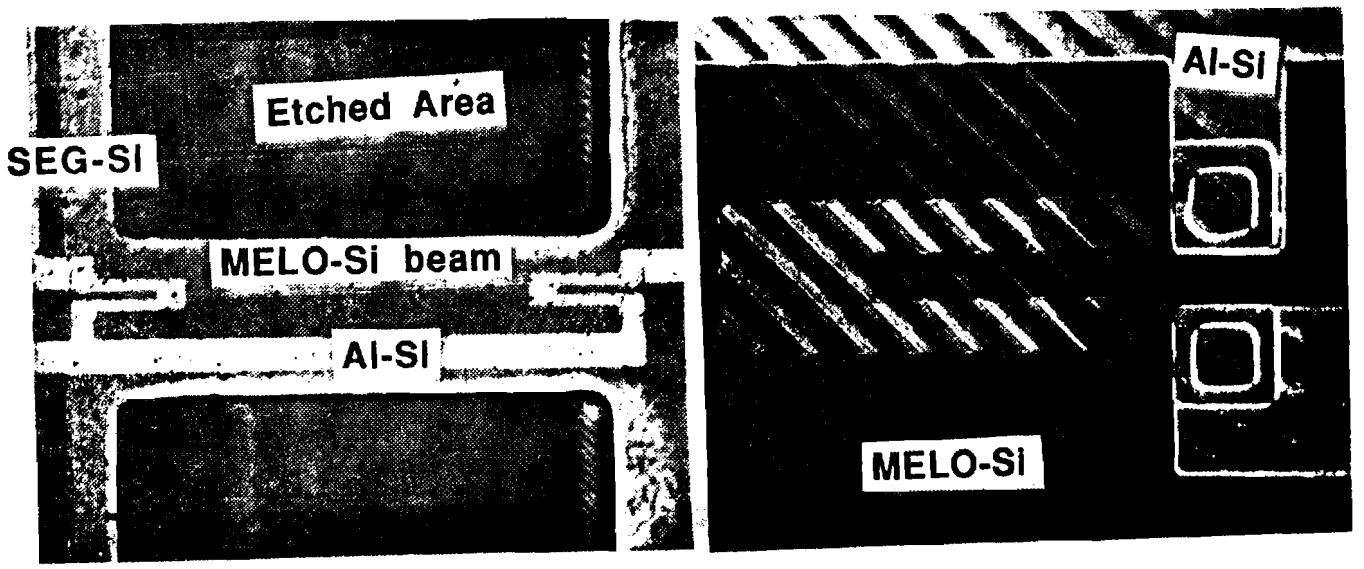
Figure **4.14.** A SEM photograph of the crack occurred on the MELO silicon diaphragm during KOH etch. It is not parallel to the SiO_2 strips but to the intersect of <111> side wall and the top <100> plane.

4.6. Final Fabrication Procedure

The resulting final structure is shown in Figure **4.15.** The final fabrication procedure is described in Figure **4.16** and its across section diagrams are illustrated in Figure **4.17.**



(a)



(b)

Figure 4.15. The resulting final structure. (a) SEM photograph of top view, (b) one bridge with piezoresistor with an enlarged view of the piezoresistor by Nomarski microscope. The seed window lines are shown by shadow.

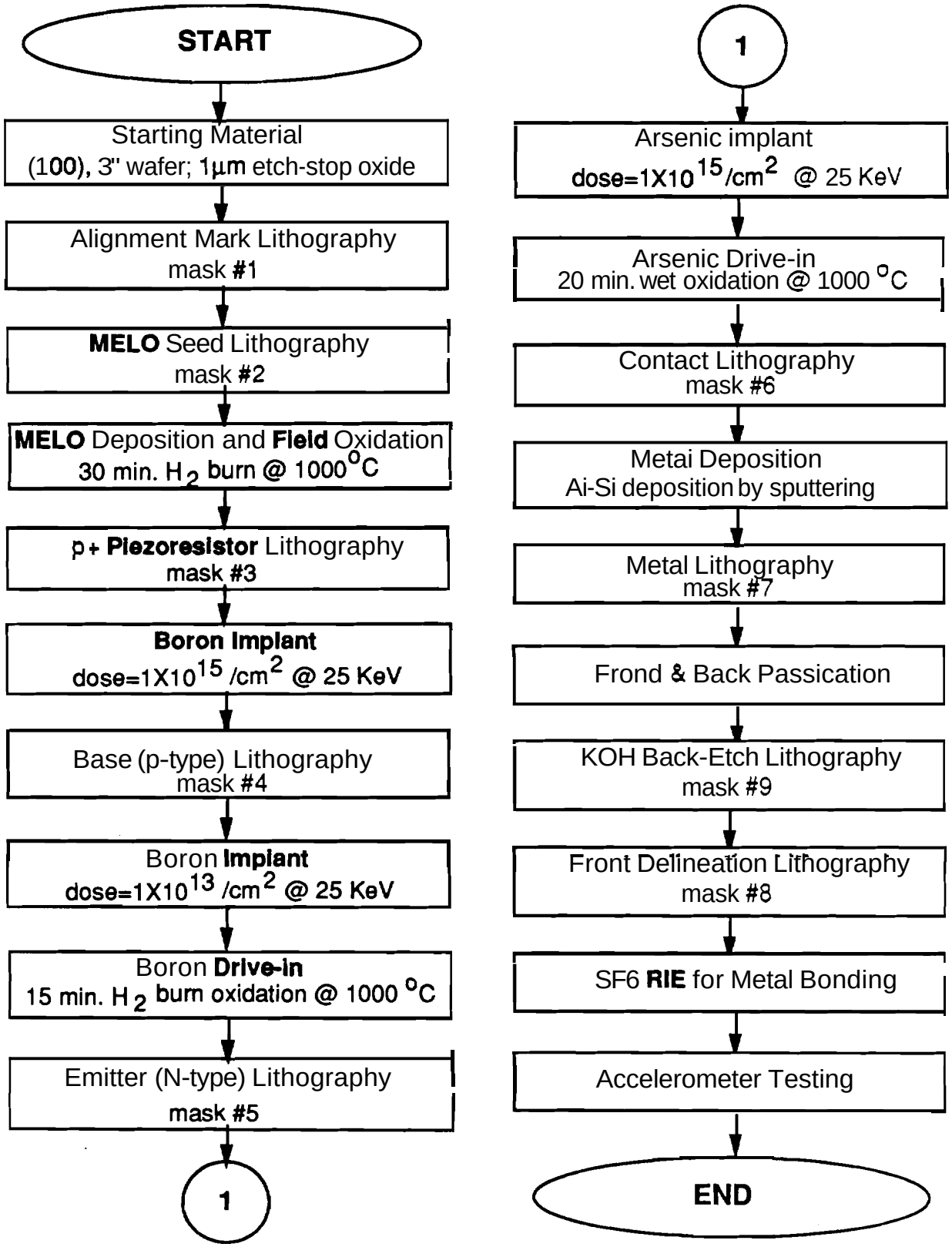
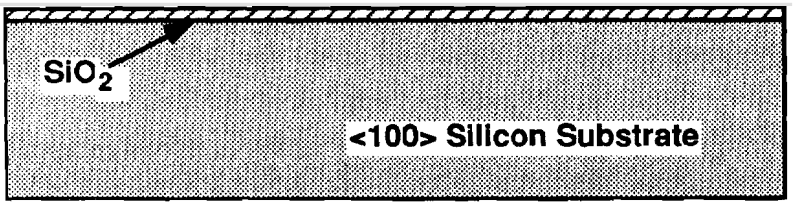
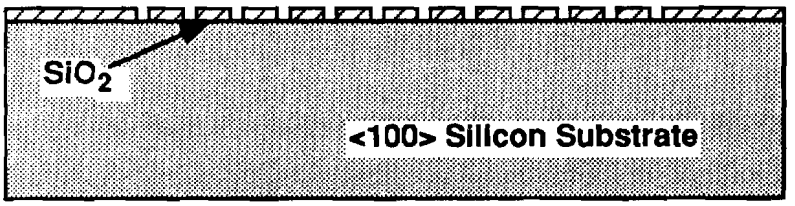


Figure 4.16. Final fabrication procedure.



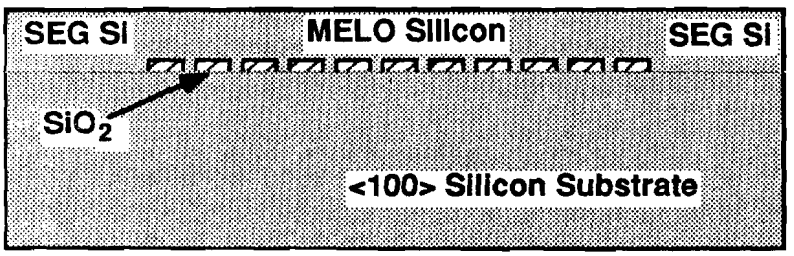
(a)

: OxideDep.
Pattern Alignment Marks
- mask #1
Field Oxidation



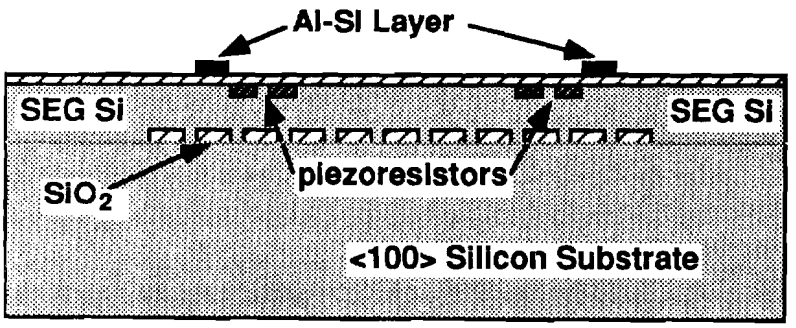
(b)

Pattern Seed Window
Along <100> Direction
for MELO silicon Process
- mask #2
2 µm seed width,
5 µm oxide width



(c)

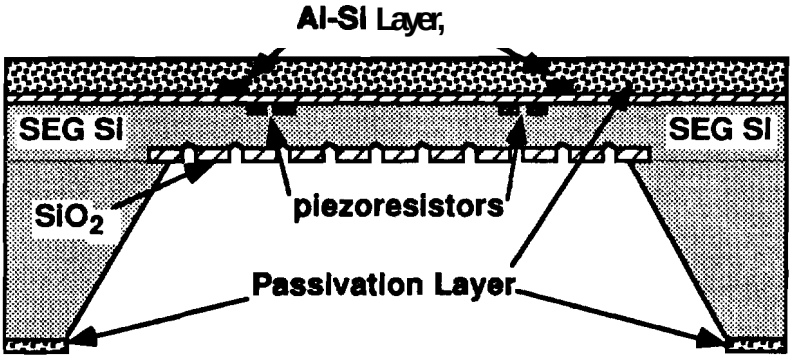
Selective Silicon Epitaxy
for 10 µm MELO silicon
Growth Rate: ~ 0.1 µm/min.



(d)

Piezoresistor fabrication
- mask #3
Base and Emitter Pattern
- mask#4 and 5
Contact Pattern - mask #6
Al-Si Metal Pattern - mask #7

Figure 4.17. Cross section diagram of the MELO accelerometer fabrication procedure.

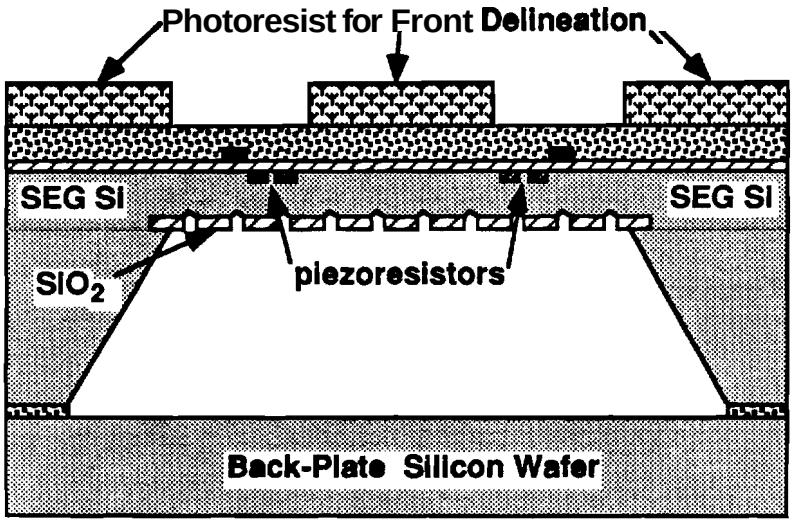


(e)

PECVD Nitride deposition as a **Passivation** layer on top and as a mask on the back side

Pattern **Back** for KOH Back-Etch
- mask # 8

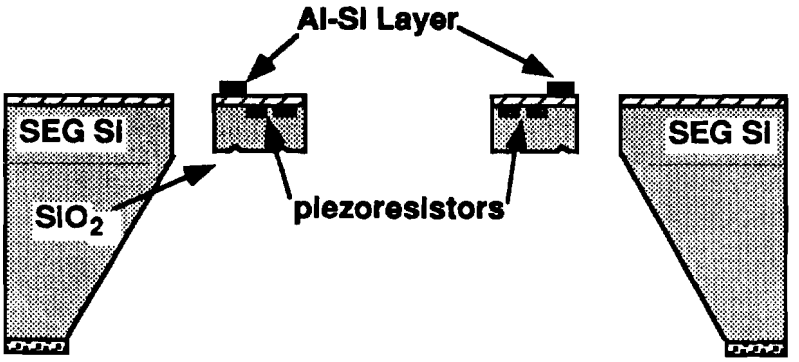
KOH Back-Etch for **MELO** Silicon Diaphragm Formation



(f)

Attach to the Back-Plate for a Mechanical Support

Pattern Front Delineation
- mask #9
AZ4620 Thick (~6 µm) Photoresist **Uaed** as a Front Mask



(g)

Fornt Delineation by Reactive **Ion** Etch (RIE) with SF_6

Photoresist Removal by Plasma Ash

Removal of Seed Pattern Oxide

Attach to the ASD Back-Plate and Test Accelerometer

Figure 4.17. Cross section diagram of the MELO accelerometer fabrication procedure (con'd).

V. Summary

This chapter presents a summary of the results of the work performed over the 1991 calendar year. Described was the successful fabrication of 9 μm thick, 250 μm x 1000 μm MELO silicon diaphragm. The standard deviation of the MELO silicon across a entire 3" wafer was 0.5μm indicating the excellent thickness control and that the uniformity has been maintained consistently. In order to be able to develop the SEG/MELO technology for an accelerometer type sensor as well as its applicability to pressure sensors, the investigation was continued based on the excellent progress made in 1990.

First, The SEG/MELO process was investigated further since the MELO silicon diaphragm is the key structure in fabricating MELO accelerometer. It was important to have excellent quality MELO silicon film for a consistent and repeatable MELO accelerometer. The MELO silicon quality was evaluated by performing a Secco defect etch on the MELO silicon film as well as by fabricating electronic devices on MELO silicon. The Secco etch revealed that further growing of MELO silicon after merging on the oxide islands heals and reduces the number of defects. The applicability of the MELO silicon to the device fabrication was examined by fabricating BJT devices, which is one of the most sensitive device to the material defects. The devices were fabricated on one merging seam and on multiple merged seams. Testing results from both base-to-emitter (B-E) diode and base-to-collector (B-C) diodes showed that the ideality factors and reverse biased junction leakage currents are comparable to the ordinary SEG devices. It indicates the MELO silicon is good enough for the majority carrier devices such as piezoresistors and MOSFETs as well as diodes and BJT devices. Table 2.2 shows the results of the fabricated BJT devices including both emitter-base and collector-base diodes. The different seed window preparation by reactive ion etch (RIE) with Freon115 and Freon116 was also investigated in order to minimize the the seed window and hence the formation of V-grooves after KOH back-etch. The width of the seed windows was controlled and made narrower than wet etched seed windows and comparable MELO silicon was grown. This will make the MELO film thickness more controllable. Any damage possible from the RIE was prevented by stopping the RIE just prior to the bottom SiO_2/Si interface and removing the residual oxide by wet etching prior to the SEG process. The postepitaxial oxidation treatment (PEOX) was investigated in the SiO_2/Si sidewall interface for reducing the V-grooves by forming the V-grooves at the sidewall edge. The interfacial bond strength at the SiO_2/Si interface

became improved by this treatment and the V-grooves start at the SiO_2/Si sidewall edge. Although this shows substantial improvement, it needs more study.

Secondly, the etching characteristics with KOH-based solution were characterized using an optimized beaker-within-beaker etching system for consistent and repeatable etching results. The temperature control was necessary because the KOH etch was sensitive to any temperature change, i.e. the vertical etch rate enhances with increased temperature. The beaker-within-beaker arrangement was employed in order to maintain the temperature of the etchant within $\pm 1^{\circ}C$ of the setpoint. The effect of the n-propanol and KOH by weight percent variation, based on two-level Taguchi experiment and ANOVA analysis, is most significant on the vertical etch rate; however, the n-propanol content has a greater contribution to the variation of the vertical etch rate than the KOH content. Furthermore, it was found that the KOH etchant does reduce in its etching strength, but this was not observed for either short or long etch times if a freshly-made etching solution was used initially. The KOH etching characteristics observed in the statistical experiments were used to determine the appropriate comer compensation mask for buffering the convex comer undercuts of the proof mass. Basically, the size of the comer compensated design can be reduced when the etching occurs under a controlled temperature environment. This was proven by etching the first corner compensation mask (designed using an uncontrolled etching system) in a controlled etching system. Therefore, a second corner compensation mask, using KOH etching characteristics observed under a controlled etching system, was designed and produced. The new mask is currently being used for the next production of the accelerometer.

At last, the &sign and layout of the Purdue MELO Accelerometer (AP-1) were accomplished. The accelerometer design was made such that it can be assembled on the ASD sensor version back-plate and tested at Delco Electronics after its completion. Piezoresistors were designed to have a sheet resistance of 212 Ω/square and a junction depth of 1 μm. Comer compensation was designed after several etch experiments were conducted to determine the appropriate parameters so that the consistent results can be obtained. Front-side passivation of Al-Si, during 6-hour long KOH etch, was investigated. Lift-off procedures used for metal delineation of the Al-Si causes sharp pikes at the metal edges which were not completely covered by the passivation layer. The metal was then attacked by KOH etch solution. Therefore, an Al-Si wet etch was employed instead of Al-Si lift-off. The original surface quality of the sputter deposited Al-Si was important as it was related to the degradation of the passivation layer. Extra pumping time, while reducing the chamber base pressure from $3x10^{-7}$ Torr to $<2x10^{-7}$, yielded a better, very smooth and

shinny surface probably due to the lower water and oxygen content. Cleaning the wafer and PECVD chamber including the electrodes are very important in order to get a near stoichiometric plasma nitride passivation layer without many defects. Layers of PECVD $SiN_x/SiO_x/SiN_x$ was the best passivation obtained thus far, even though one thick (> 3 μm) PECVD nimde seemed to work. However, too thick of a passivation film applies stress to silicon wafer and results in cracking during the KOH etch. Al-Si and Chrome double metal layer was med as a metallization sandwich since Chrome gave a much smoother surface and it lasted longer in the KOH etch solution.

Based on the above results several completed accelerometer dies were delivered to Delco for testing. The first testing revealed that the back-side etch mask needed to be modified due to the undercut of the PECVD nitride mask during KOH back etch. With the second set of masks, the accelerometer yield was improved and more dies will be delivered for testing. The SiO_2-V-groove etch stop, initially used to form the thin silicon diaphragm, worked exactly as expected, yielding high quality material and good thickness control.