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Atomic layer deposited Al_2O_3 for gate dielectric and passivation layer of single-walled carbon nanotube transistors

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High performance single-walled carbon nanotube field effect transistors (SWCNT-FETs) fabricated with thin atomic layer deposited (ALD) Al_2O_3 as gate dielectrics and passivation layer are demonstrated. A 1.5 μm gate-length SWCNT-FETs with 15 nm thick Al_2O_3 insulator shows a gate leakage current below 10^{-11} A at $-2.5\ \mathrm{V} < V_g < +7\ \mathrm{V}$, a subthreshold swing of $S \sim 105$ mV/decade, and a maximum on current of -12 μA at a reverse gate bias of -1 V. Lack of hysteresis in *IV* characteristics and low low frequency noise indicate high quality oxide-nanotube interface achieved utilizing ALD Al_2O_3 as gate dielectrics and passivation layer. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2724904]

Single-walled carbon nanotube field effect transistors (SWCNT-FETs) have attracted attention as complementary nanoscale devices to conventional metal-oxide-semiconductor (CMOS) transistors due to excellent electrical properties of single-walled nanotubes.[1,2] Since their first demonstration in 1998,[3] significant progress has been made in improving the electrical performance of these devices.[4,5] Current research in SWCNT-FETs is focused on achieving high transconductance, scaling down gate dielectrics, and eliminating hysteresis caused by various charge trapping mechanisms. An attractive research approach to improve the device transconductance and current capability while reducing hysteresis as pursued by several researchers is to utilize novel gate dielectric materials and passivation layers on SWCNTs.[4–7] Several groups have investigated new SWCNT-FET gate dielectric structures including (i) bottom gated with native Al_2O_3 dielectrics,[6] (ii) top gated with 15–20 nm thick SiO_2 dielectrics,[7] and (iii) top gated with atomic layer deposited (ALD) 8–20 nm thick high-*k* zirconium oxide (ZrO_2) (Ref. 4) and hafnium oxide (HfO_2).[5] Among the above techniques, utilizing high-*k* ALD ZrO_2 and HfO_2 as gate dielectric is very promising and has achieved near ballistic transport and ideal subthreshold swing of ~60 mV/decade. The drawbacks of these techniques are that high-*k* materials such as ZrO_2 and HfO_2 are difficult to grow and difficult to remove using standard wet etching processes due to crystallization of ALD ZrO_2 and HfO_2 after postdeposition annealing (PDA). Additionally, HfO_2 and ZrO2 are biohazard material.

Passivation of SWCNT-FETs helps stabilizing their electrical characteristics against environmental variations. Difficulty in growth and etching as well as high dielectric constant are main reasons that ALD ZrO_2 and HfO_2 are not used as passivation layer. Instead, chemical vapor deposited (CVD) Si_3N_4 (Ref. 8) and polymethylmethacrylate (PMMA) polymer[9] are utilized. However, Si_3N_4 passivation leads to electrical degradation of carbon nanotube transistor. It is also reported that PMMA passivation is not adequate to protect the nanotube channel from ambient humidity.[10]

In this letter, we report high performance and high interface quality top-gated SWCNT-FETs with Al_2O_3 dielectric films deposited by ALD technique. ALD Al_2O_3 films have been utilized as passivation and thin gate dielectric layers. The ALD Al_2O_3 is annealed after dielectric layer deposition and can be patterned with standard lithographic processes using a simple wet etching process. These nanotube-based devices achieve high on current and high transconductance with no hysteresis and low interface trap density.

We have used low frequency noise characterization as well as hysteresis in V_g-I_d characteristics for studying the interface quality in SWCNTs prior and after ALD Al_2O_3 deposition. Previous work points out to hysteresis in CNT-FETs as a method to analyze interface quality.[8,9] The problem of hysteresis measurement is that hysteresis in V_g depends on the sweeping rate of gate voltage and the range of gate voltage, which prevents measuring interface traps quantitatively. In CMOS technology, capacitance-voltage (*C-V*) measurement and low frequency noise are used to analyze the interface traps in oxide/semiconductors. Carbon nanotube interface has an extremely small gate dielectric capacitance, $C_{ox} \sim 2\pi\varepsilon_0\varepsilon/\ln(2t_{ox}/R) \sim 28$ aF/nm,[4] much lower than the detectable range of available laboratory equipment, preventing conventional *C-V* measurement as a possible characterization technique.[11] Low frequency noise is then the only quantitative method for analysis of interface traps in nanodevices.

The SWCNT-FET devices reported here, shown in the inset of Fig. 1, are fabricated on a high resistivity Si substrate ($\rho \approx 10$ kΩ) with a 500 nm SiO_2 thermal oxide. SWCNTs are synthesized on the thermal oxide by thermal CVD of methane on the substrate using commercial ferritin (Sigma) catalyst. The grown carbon nanotubes have a diameter of 1–3 nm with an approximate tube density of $2-10/\mu m^2$. Following the nanotube growth, the ALD Al_2O_3 film is deposited on SWCNTs on SiO_2 substrate using the ASM Microchemistry F-120 ALCVD™ reactor. A 15 nm amorphous Al_2O_3 film is deposited on the wafer at 300 °C followed by

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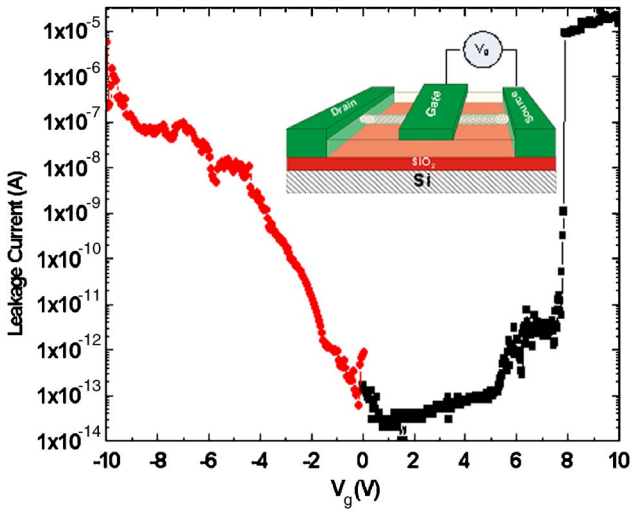

FIG. 1. Leakage current I_g (A) vs gate bias V_g (V) for SWCNT-FETs having 15 nm Al_2O_3 dielectrics. Inset: cross section of the top gate single-walled carbon nanotube field effect transistors with 15 nm thick ALD-grown Al_2O_3 as gate dielectric.

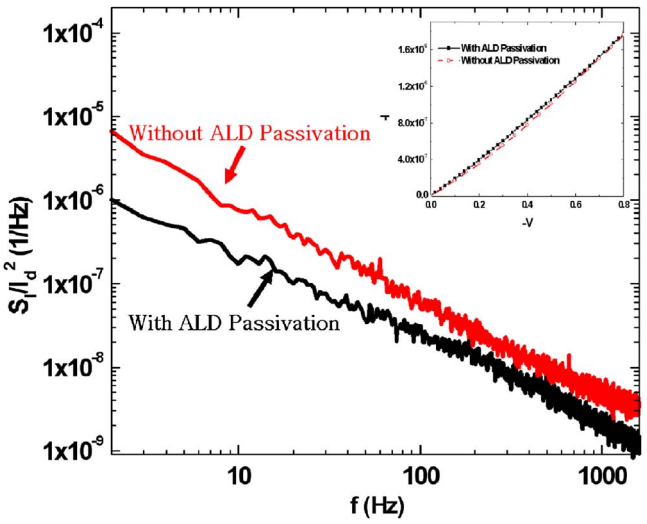

FIG. 2. Low frequency noise spectrum of current fluctuation of the pre-postpassivation of ALD Al_2O_3 SWCNTs for drain to source resistor. Inset: *IV* characteristics of pre-postpassivated SWCNT. Both resistances have the same resistance of 500 kΩ.

PDA in N_2 at 600 °C for 30 s. Figure 1 shows the gate leakage current of a SWCNT-FET having 1.5 μm gate length with two semiconducting nanotubes in the channel. As can be seen from the figure, the leakage current is very small, in the range of 10 pA–10 fA at $-2.5\ \mathrm{V} < V_g < 7\ \mathrm{V}$, about five orders of magnitude smaller than the drain current of nanotube devices. Using wet etching (diluted HF solution), the Al_2O_3 oxide on the source and drain patterns is removed while the gate area is protected by photoresist. Metal contacts are formed by electron beam deposition of Pd followed by a lift-off process. Gate metal is defined by UV photolithography followed by the deposition of Ti/Au (10/50 nm) with a minimum gate length of 1.5 μm. Ti/Au (20/450 nm) metal interconnects are finally deposited on top of the source and drain Pd contacts.

There are reports of high quality interface achieved between ALD Al_2O_3 and carbon nanotubes,[12] Si,[13] and GaAs[14] substrates. In these reports, the quality of ALD Al_2O_3 films exhibits a strong dependence on ALD growth conditions and PDA.[12–14] We have previously investigated high quality Al_2O_3 films on GaAs substrate through PDA.[14] The deposited ALD Al_2O_3 film shows highly electrical insulating characteristics, having very low leakage current density of $\sim 10^{-9}$–10^{-7} A/cm^2 for 5 nm thick Al_2O_3 at −3–+3 V gate bias. For the same oxide thickness compared to the state-of-the-art SiO_2 on Si, the leakage current density of ALD Al_2O_3 film on GaAs is similar or even one order of magnitude lower at a given gate bias. Al_2O_3 has a high band gap (~9 eV), a high breakdown electrical field (5–30 MV/cm), high permittivity (8.6–10), and high thermal stability (up to at least 1000 °C). It will also remain amorphous under typical heat treatment. In our current experiments, Al_2O_3 films are grown on CNTs using alternating pulses of $Al(CH_3)_3$ (the Al precursor) and H_2O (the oxygen precursor) at 300 °C in a carrier N_2 gas flow. Postdeposition annealing is done in N_2 ambient at 600 °C for 30 s using rapid thermal processing. Unlike ALD HfO_2 or ZrO_2, Al_2O_3 can be conveniently etched using standard wet etching (HF) techniques even after high temperature annealing.

The $1/f$ noise spectrum in metal-oxide-semiconductor field effect transistors (MOSFETs) can be used as a qualitative measure of the origin of the noise and the density and energy of the interface traps responsible for $1/f$ noise.[15,16] Similarly, measuring the low frequency noise spectrum of the SWCNTs can indicate interface trap density and energy around CNTs. In this letter, by measuring the $1/f$ noise prior to and after the deposition of ALD passivation layer, we monitor a change in the trap density around the CNTs assuming that the trapping-detrapping mechanism is responsible for noise. Figure 2 shows the I_d^2 normalized low frequency noise spectrum of single-walled carbon nanotube biased at −0.3 V prior to and after ALD Al_2O_3 passivation. By applying ALD Al_2O_3 passivation layer, the resistance value of 500 kΩ remains intact as can be seen from the *IV* curve in the inset of Fig. 2. On the other hand, the $1/f$ noise spectrum of SWCNTs passivated by Al_2O_3 is approximately one order of magnitude smaller than unpassivated SWCNTs. The small noise spectrum of the passivated SWCNTs indicates that the interface trap densities are remarkably low. Kim *et al.*[9] reported that water molecules on or near SWCNTs are the

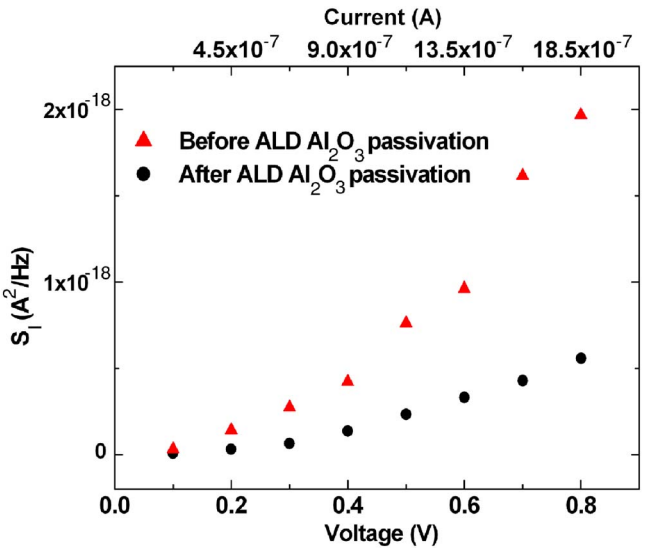

FIG. 3. Current vs current noise amplitude of S_I for drain to source resistor at 10 Hz as a function of voltage prior to ALD Al_2O_3 passivation and after ALD Al_2O_3 passivation.

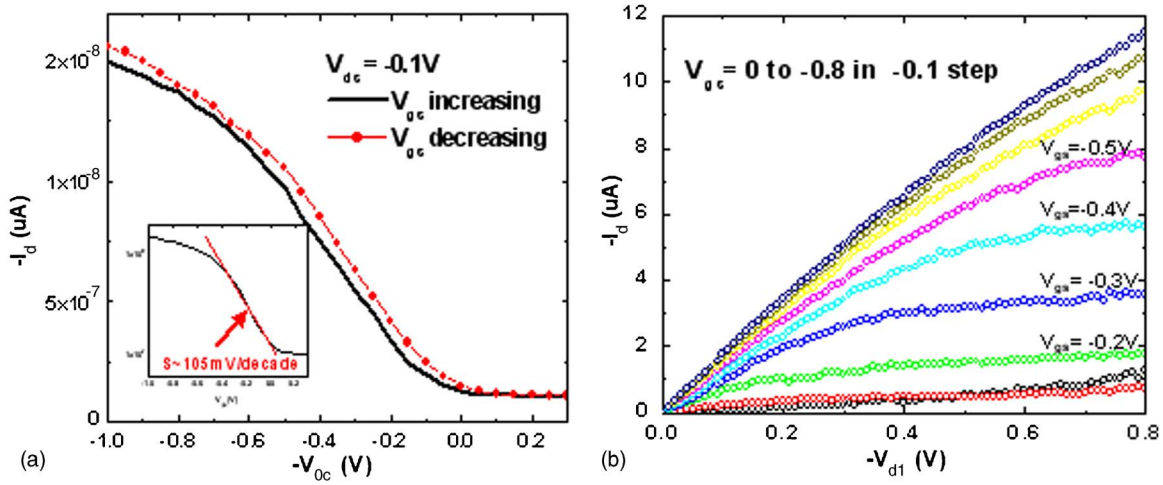

FIG. 4. Characteristics of a *p*-type SWCNT-FET with Al_2O_3 as gate dielectrics. (a) Current I_d vs V_{gs} as increasing (line) and decreasing gating sweeps (points) for a 1.5 μm gate-length SWCNT-FET at V_{ds} of −0.1 V. Inset: log-scaled current I_d vs V_{gs} curve. The subthreshold swing (S) is about 105 mV/decade. (b) Drain current vs drain bias as a function of gate bias of the same device.

primary source of interface charge traps, giving rise to large hysteresis. By passivating CNTs using ALD Al_2O_3, interface traps activated by water absorption from the ambient may be significantly reduced.

Figure 3 shows the correlation between the current noise amplitude (S_I) at 10 Hz and current (I) as a function of the applied voltage (V) prior to and after ALD Al_2O_3 passivation. The $1/f$ noise spectrum can be found according to Hooge's empirical law[17]

$$S_I(f) = \frac{q\mu_{\text{eff}}\alpha_H IV}{fL^2} = \frac{q\mu_{\text{eff}}\alpha_H I^2}{R_{\text{ch}}L^2 f},$$

where α_H is the Hooge parameter, q is the electronic charge, μ_{eff} is the effective mobility of carriers inside the channel, and L is the channel length. The resistance R_{ch} given by V/I is a constant value of 500 kΩ. In both cases (prior to and after ALD Al_2O_3 passivation), current noise amplitude (S_I) is proportional to I^2, a trend observed in semiconductor resistors. The estimated Hooge parameters prior to and after ALD Al_2O_3 passivation are 9×10^{-3} and 5.44×10^{-3}, respectively. The device with ALD Al_2O_3 passivation has superior property in noise.

Figure 4 shows the *I-V* characteristics for a 1.5 μm gate length SWCNT-FET with a 15 nm thick Al_2O_3 in the ambient environment. Figure 4(a) shows a typical I_d vs V_{gs} characteristics when V_{gs} is swept from −1 to 1 V and back to −1 V. In most of the SWCNT-FET, the direction of V_{gs} sweep and its speed will create a hysteresis response due to the interface charge traps, mainly from water molecules.[9] The amount of voltage shift depends on the interface trap density on/near SWCNTs and how fast the sweep is done. Small hysteresis observed in the Fig. 4(a) indicates that ALD Al_2O_3 suppresses the density of traps in SWCNT-FETs operating in ambient conditions. Figure 4(b) shows I_d vs V_{ds} at different gate biases. The curves resemble a conventional *p*-MOSFET characteristic, exhibiting linear region at low $|V_{ds}|$ and saturation region at higher $|V_{ds}|$. The maximum intrinsic transconductance $g_m = dI_{ds}/dV_{ds}|_{V\text{ds}=0.2\text{ V}}$ of 3 μS and the maximum on current of −12 μA are observed. The subthreshold swing (S) is about 105 mV/decade.

In conclusion, we have demonstrated the application of atomic layer deposited Al_2O_3 gate dielectric and passivation layers for high performance SWCNT-FET. The subthreshold swing of $S\sim105$ mV/decade, high transconductance of 3 μS at a drain bias of 0.2 V, and a maximum on current of −12 μA indicate that ALD-based Al_2O_3 through postdeposition annealing can be used as gate dielectric for CNT transistors. Furthermore, low level of low frequency noise and hysteresis-free *IV* characteristics demonstrate that ALD Al_2O_3 can be utilized as excellent passivation layer on SWCNTs.

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