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ANALYSIS OF THE AUXILIARY RESONANT COMMUTATED POLE INVERTER

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ABSTRACT

Walters, Eric A. M.S.E.E., Purdue University, August, 1995. Analysis of the Auxiliary Resonant Commutated Pole Inverter. Major Professor: Oleg Wasynczuk.

A study of the Auxiliary Resonant Commutated Pole (ARCP) converter and a comparison with standard hard-switched inverters is presented. A thorough description of the ARCP circuit topology is made with three switching scenarios discussed: commutation from a diode, commutation from a switch with low current, and commutation from a switch with high current. The efficiency of the ARCP inverter is attributed to the fact that switching losses are eliminated by switching under zero voltage or zero current conditions. To accomplish this task, addition circuitry is introduced which contributes to additional conduction losses. An example H-bridge is presented using both ARCP phase legs and hard-switched phase legs. Losses for each case are calculated and a comparison is made. From simulations, it is shown that the additional conduction losses introduced by the ARCP circuit are small in comparison with the switching losses found in a standard hard-switched circuit. A simulation of a three-phase example ARCP inverter is briefly discussed.

1. INTRODUCTION

The Auxiliary Resonant Commutated Pole (ARCP) Circuit was developed by General Electric Corporation R&D to be used in high-efficiency inverters. By increasing the efficiency of the inverter, not only is the power loss in the inverter reduced,,but the size and weight of the inverter can also be greatly reduced. This fact makes the ARCP technology extremely valuable in applications were size constraints are a primary concern. The ARCP achieves high efficiency by soft switching, that is by turning on or off the primary switches when the switch voltage or current are zero. Therefore, the switching loss, the product of voltage and current, is zero. This is similar to LC snubber circuits; however, in snubber circuits, load current constraints determine whether zero voltage or zero current switching can be obtained. With the ARCP circuit topology, zero switching losses are independent of the load current. In this thesis, both a conventional hard-switched phase leg and an ARCP phase leg are discussed, a comparison between the losses in a hard-switched H-bridge and an ARCP H-bridge is presented, and an application using the ARCP in a current-controlled induction motor is presented.

2. LOSSES IN HARD-SWITCHED INVERTERS

211 Introduction

The ARCP is a soft switching technology which eliminates turn-on and turn-off losses as will be discussed in the next chapter. However, prior to examining the elimination of these losses, an explanation of the switching losses of a conventional hard-switched phase leg is presented herein. The first losses to be discussed in this chapter involve the conduction losses associated with the four states of a hard-switched phase leg. Then, the analysis of two switching senarios will be explored in which the turn-on and turn-off losses associated with the transistors will be discussed.

2.2 Hard-Switched Phase Leg

The circuit shown in Fig. 2.1 is an example of a hard-switched phase leg. In this circuit, bipolar junction transistors (BJT's) are used as switches. Although BJT's are shown in this figure, other solid state devices can also be used. Examples of other solid state devices that are typically used include field effect transistors (FET's), metal oxide semiconductor FET's (MOSFET's), gate turnoff thyristors (GTO's), and insulated gate transistors (IGT's). Analysis of the losses associated with each of these device!; can vary greatly; however, the concept of switching loss which will be explored herein is universal.

In the circuit shown in Fig. 2.1, the positive and negative dc rails are labeled as $+V_{dc}$ and $-V_{dc}$, respectively. The BJT's are labelled Q1 and Q2 with their collector currents denoted as I_{C1} and I_{C2}, respectively. The base currents associated with the BJT's are labeled I_{B1} and I_{B2}. It will be assumed that the base currents, which are controlled by independent current sources, will determine if the transistors are on or off. If the base cur-

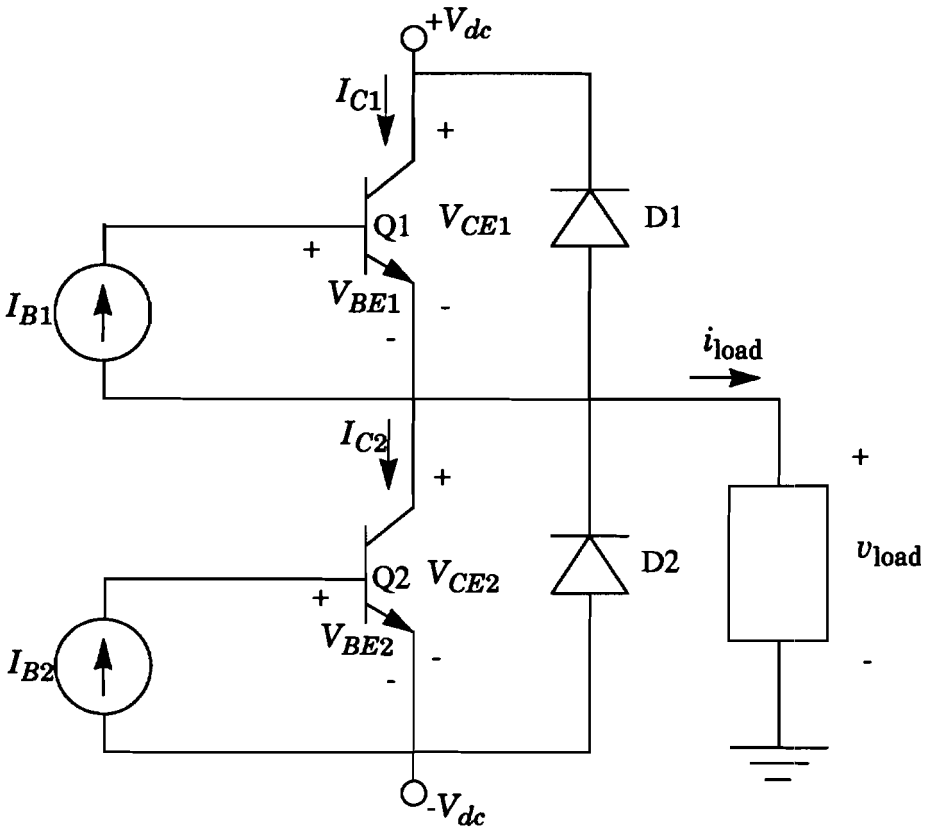

Fig. 2.1. A hard-switched phase leg using BJT's.

rent associated with one of the transistors is zero, the associated transistor will not conduct and can be omitted from the circuit; therefore, the transistor is considered to be off. The dc current gain of each transistor is h_{FE} which is defined as the ratio of the collector current to the base current, $\frac{I_{C1}}{I_{B1}}$, in the active region. If the collector current is assumed to be less in magnitude than I_{max} and the base current is set equal to $\frac{I_{max}}{h_{FE}}$, then the transistor is in the saturation region of operation as can be observed from the plot of the collect current versus the collector to emitter voltage, V_{CE}, with a constant base current shown in Fig. 2.2 [1]. From the plot shown in Fig. 2.2, it can be seen that if the transistor is supplying a load current which is less than I_{max} then the voltage drop across the transistor will be less than $V_{CE,sat}$ which is approximately 2 volts (V) for high-voltage BJT's. Therefore, the

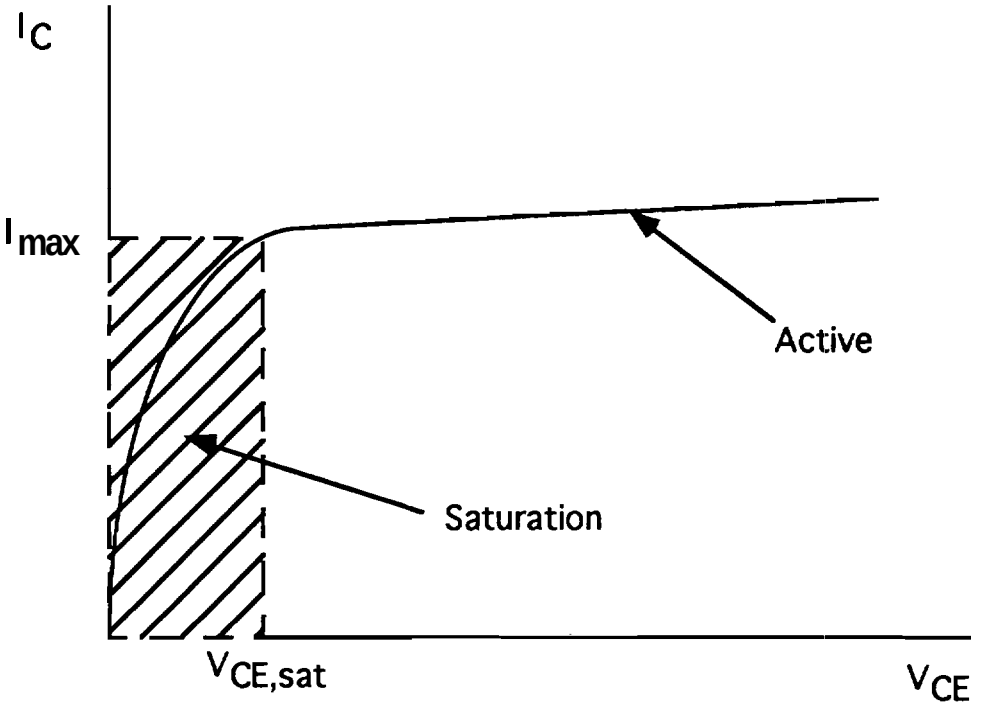

Fig. 2.2. I_C versus V_{CE} with a constant I_B.

load voltage will be within 2 V of the potential of the dc rail to which the transistor is connected. Specifically,

$$'load = V_{dc} - V_{CE,\,sat} \tag{2-1}$$

If the source voltage is large compared to $V_{CE,sat}$, i.e.

$$V_{dc} \gg V_{CE,\,sat} \tag{2-2}$$

then

$$v_{load} \approx V_{dc} \tag{2-3}$$

The previous equations apply only when Q1 is on and the load current is positive. However, if the load current is negative and transistor Q2 is off, the only path for the current is through diode D1. In this case,.

$$'load = V_{dc} + V_{D1} \tag{2-4}$$

Typically, V_{D1} is on the order of 1 V whereupon

$$V_{dc} \gg V_{D1} \tag{2-5}$$

Thus,

$$i_{load} \approx V_{dc} \tag{2-6}$$

It can be seen that the output voltage is approximately equal to V_{dc} when Q1 is on or when Q2 is off and the load current is negative.

If transistor Q2 is on and the load current is negative

$$v_{load} = V_{CE,sat} - V_{dc} \tag{2-7}$$

Hence,

$$v_{load} \approx -V_{dc} \tag{2-8}$$

With Q1 off and the load current positive, the load current must flow through diode D2. In this case,

$$v_{load} = -V_{dc} - V_{D2} \tag{2-9}$$

Therefore,

$$v_{load} \approx -V_{dc} \tag{2-10}$$

Hence, when Q2 is on or when Q1 is off and the load current is positive, the load voltage is approximately equal to $-V_{dc}$.

The hard-switched phase leg has four states: Q1 on and the load current is positive, Q2 off and the load current negative, Q2 on and the load current is negative:, and Q1 off and the load current positive. In each of these states, the load current is flowing through one of the four solid state devices composing the phase leg. With the conduction of current through these physical devices, there is an associated power loss. This conduction power loss can be calculated for each state as the product of the load current and the voltage across the device supplying the current. When Q1 is on and the load current is positive, the conduction power loss is

$$P_{Q1,con} = i_{load} \cdot V_{CE,sat} \tag{2-11}$$

With Q2 off and the load current is negative, the load current flow through diode D1 and introduces a conduction power loss of

$$P_{D1,\,con} = -i_{load} \cdot V_{D1} \tag{2-12}$$

In the third state with Q2 on and a negative load current, the conduction loss is

$$P_{Q2,\,con} = -i_{load} \cdot V_{CE,\,rat} \tag{2-13}$$

When Q1 is off and the load current is positive, the conduction power loss associated with D2 is

$$P_{D2,\,con} = i_{load} \cdot V_{D2} \tag{2-14}$$

2.3 Transistor Turn-on Losses

Two examples of switching losses will be explored in this chapter. Both examples involve the load voltage being switched from the lower dc rail, $-V_{dc}$, to the upper dc rail, $+V_{dc}$. In the first example, the load current, i_{load}, is assumed to be positive. In the second case, the load current is assumed to be negative. In both examples, the load is assumed to be inductive whereby the load current is essentially constant during the switching interval.

It is assumed that, initially, the load is latched to the lower dc rail (transistor Q2 is on and Q1 is off) and the load current is positive. Although Q2 is gated on, the load current flows through the diode D2; whereupon, a small conduction loss, P_{D2}, will be associated with D2. The value of diode conduction power loss is the product of the load current and the forward voltage drop across D1 (approximately 1 V). The conduction energy loss for D2 can be calculated as the integral of the conduction power loss with respect to time, i.e.

$$E_{D2} = \int P_{D2} dt = V_{D2} \int i_{load} dt \tag{2-15}$$

With all of the load current flowing through the diode, the transistor Q2 will not have any conduction losses. Therefore, the only loss initially associated with this state of the phase leg is the-conduction loss in thediode.

When the commutation process begins, transistor Q2 is turned off, and after a brief delay, transistor Q1 is turned on. Since transistor Q2 is switched off under zero current conditions, there is no power loss associated with Q2 in the turn-off process. However,

when Q1 is turned on, the load current does not immediately commute from diode D2 to Q1 because the minority carriers in the base region of Q1 must be supplied before conduction through Q1 can begin. As the base current, I_{B1}, adds minority carriers to the base of Q1, the collector current starts increasing and displacing the current through D2 as the source of the load current. This increase in the collector current can be observed in the simplified plots shown in Fig. 2.3. During this interval, both diode D2 and transistor Q1 are conducting; however, with D2 conducting, the load voltage is still clamped to the lower dc rail. This results in the rail-to-rail voltage being placed across Q1 while current is flowing through Q1; thus, a large amount of power is lost in Q1 during this phase of the commutation. This increase in the collector current, I_{C1}, and the constant V_{CE1} can be observed in Fig. 2.3 [1,2]. The resulting power loss in Q1 during this interval is approximated as a straight line increasing to P_{max} (Fig. 2.3). However, since current is also flowing through diode D2 during this interval, there is an additional loss term associated with the conduction of some of the load current through D2.

The second interval of high loss begins when the collector current of Q1 displaces all of the diode current whereupon the load voltage switches from the lower rail to the upper rail. During this swing, transistor Q1 conducts all of the load current and the load voltage is going from the rail-to-rail voltage to $V_{CE,sat}$ (Fig. 2.3). Hence, the product of the transistor current and the collector-to-emitter voltage is large during this interval and may be approximated as a straight line going from P_{max} to P_{con}.

The energy loss associated with the turning on of transistor Q1 is the integral of the power loss during turn-on. This loss is divided into two parts: the loss in Q1, and the conduction loss in D2 during commutation. The energy loss in Q1 is approximated as the area of the triangle in the power loss diagram (Fig. 2.3) [1].

$$E_{Q1,\,turnon} = \frac{1}{2} P_{max} t_r = \frac{1}{2} (2 V_{dc} i_{load})\, t_r \tag{2-16}$$

The time required to complete the turn-on process is called the rise time, t_r. The current flowing through D2 during the commutation of the load current is

$$I_{D2} = i_{load} - I_{C1} \tag{2-17}$$

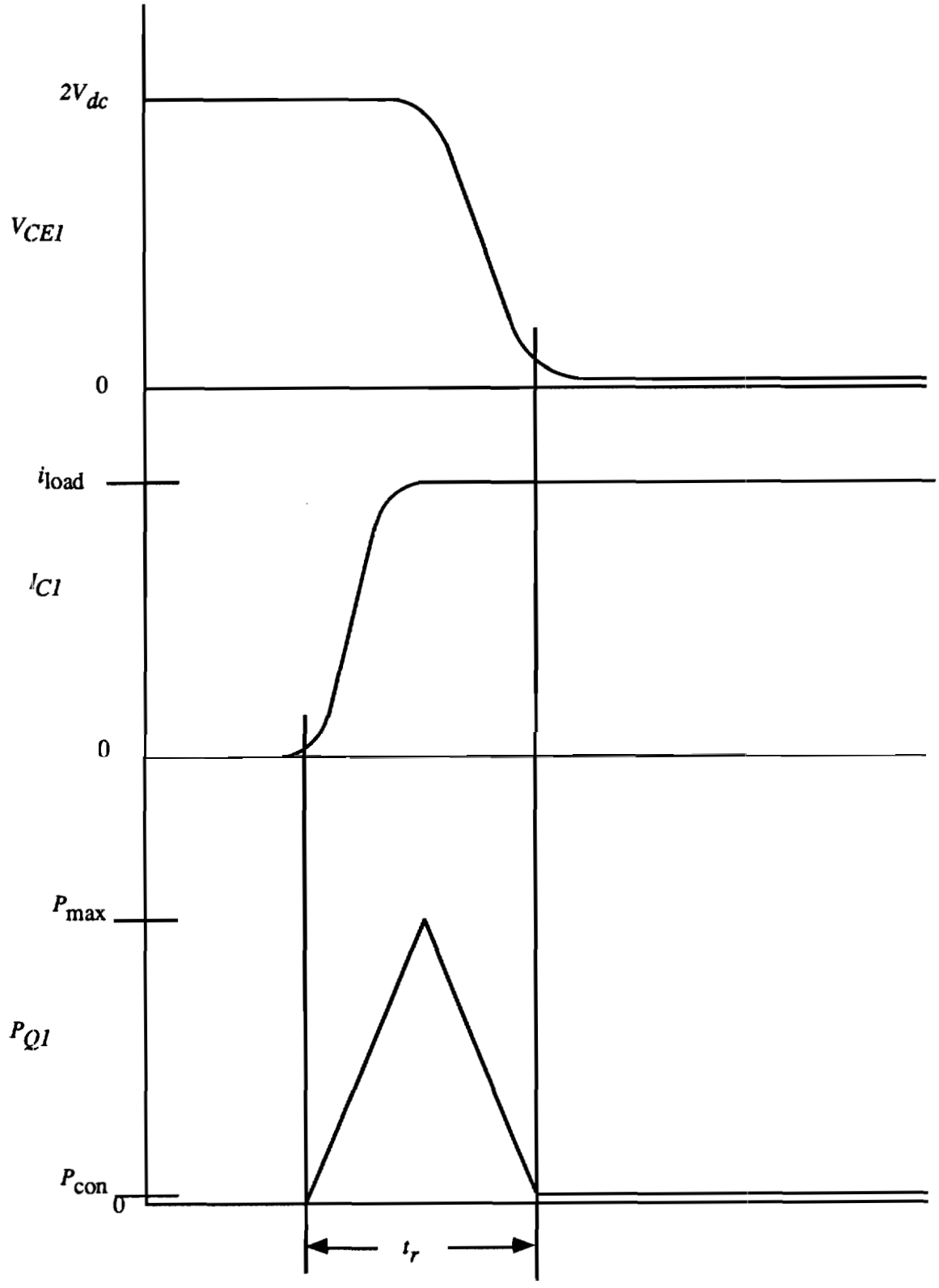

Fig. 2.3. Simplified turn-on switching waveforms for a typical BJT.

The diode current can be approximated as a straight line going from a value of i_{load} to zero in a time of $\frac{1}{2}t_r$. Therefore, the energy loss associated with the conduction of current through D2 during the commutation of the load current can be expressed as

$$E_{D2,\,turnon} = \left(\frac{1}{2}i_{load}\right)V_{D2}\left(\frac{1}{2}t_r\right) \tag{2-18}$$

Thus, the total turn-on energy loss is

$$E_{turnon} = \frac{1}{2}(2V_{dc}i_{load})\,t_r + \left(\frac{1}{2}i_{load}\right)V_{D2}\left(\frac{1}{2}t_r\right) \tag{2-19}$$

When the load voltage reaches the upper rail, the switching sequence is complete. The only loss during this phase is the conduction loss in transistor Q1. This loss is small because the transistor is in the saturation region where the collector-to-emittervoltage is $V_{CE,sat}$. The conduction energy loss for Q1 is

$$E_{Q1,\,con} = \int P_{con}dt \approx V_{CE,\,sat}\int i_{load}dt \tag{2-20}$$

2.4 Transistor Turn-off Losses

In this analysis, it is assumed that the load current is initially negative and the load voltage is to be switched from the lower rail to the upper rail. With a negative load current and the load voltage initially latched to the lower rail, transistor Q2 supplies the load current. Initially, the only loss associated with this phase leg is the conduction loss in transistor Q2. The conduction energy loss for Q2 is

$$E_{Q2,\,con} = \int P_{Q2}dt = -V_{CE,\,sat}\int i_{load}dt \tag{2-21}$$

The energy loss has a negative sign in the third term because the load current is negative in this example and the energy loss is always considered to be positive. The collector current, I_{C2}, the collector-to-emittervoltage, V_{CE2}, and the conduction power loss for Q2 can be observed in Fig. 2.4 [1,2].

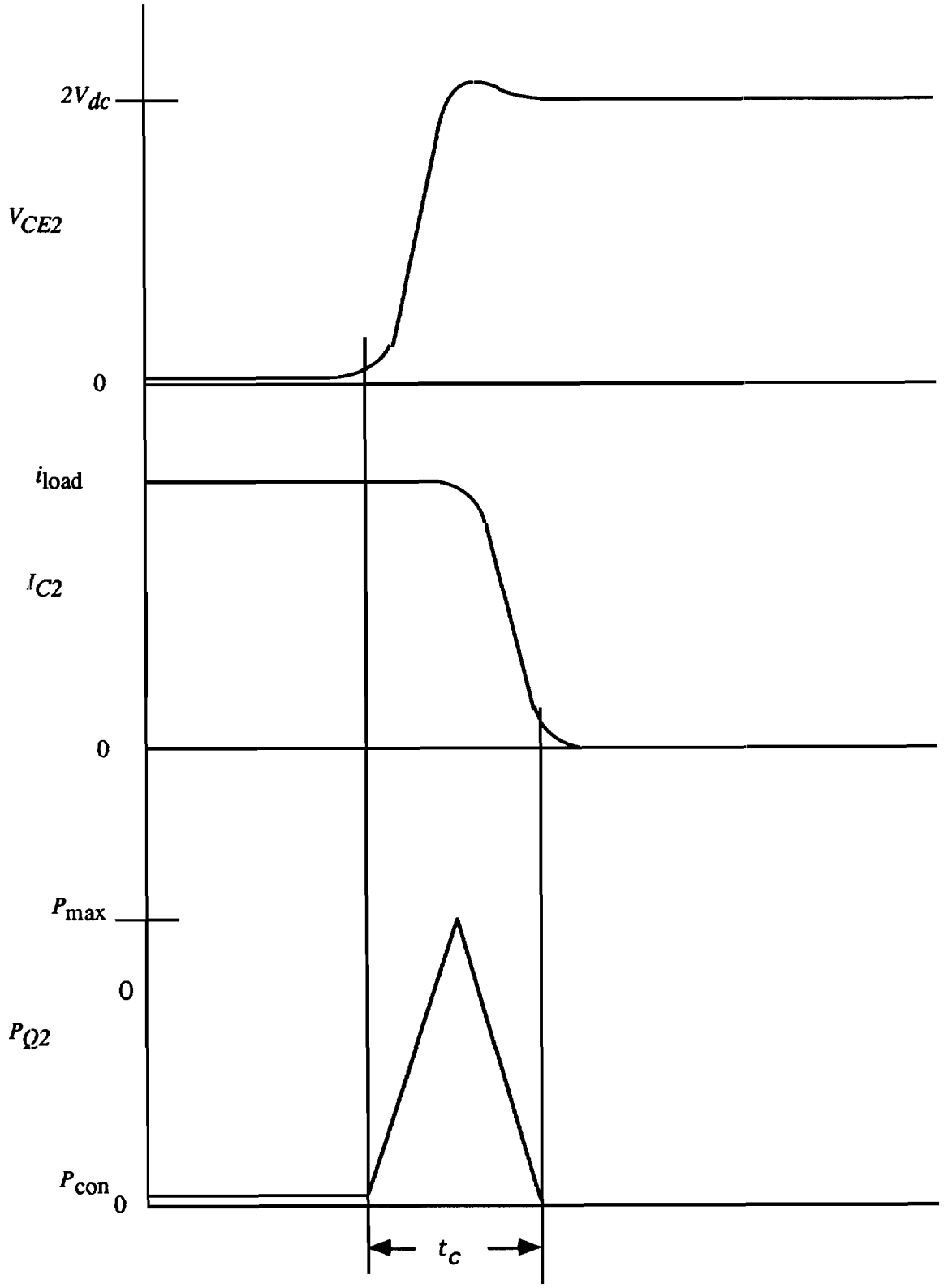

Fig. 2.4. Simplified turn-off switching waveform for a typical BJT.

In order to switch the output voltage, transistor Q2 is switched off and after a brief delay transistor Q1 is gated on. However, due to the fact that minority carriers are still in the base of transistor 42, the collector current remains constant initially. As the minority carriers are collected, the minority carrier concentration in the base will begin to diminish. Consequently, the collector-to-emitter voltage for 42, V_{CE2}, will start to increase. As a result of the inductive nature of the load, the collector current will remain constant until V_{CE2} reaches a value of $2V_{dc}$. Therefore, during this period of the switching, there is significant power being dissipated in transistor Q2 because the load current is flowing through Q2 and the voltage across Q2 is reaching $2V_{dc}$. This increase in V_{CE2} during which I_{C2} is constant can be observed in Fig. 2.3 along with the increasing power loss associated with this interval.

Once V_{CE2} reaches a value of $2V_{dc}$, diode D1 becomes forward bias and begins to assume part of the load current. This commutation of the load current from Q2 to D1 causes I_{C2} to decrease. During this decrease, there is still large amounts of power being dissipated in transistor 42. In addition, there is also a power loss associated with the conduction of current through diode D1.

The energy loss associated with the turn-off process of transistor Q2 is expressed as the sum of the energy loss in Q2 and the conduction energy loss in D1 during the commutation of the load current from Q2 to D1. The energy loss in Q2 can be approximated as the area of the triangle in the power loss diagram for Q2 (2-22) where t_c is called the commutation time [1].

$$E_{Q2,\,\text{turnoff}} = \frac{1}{2}(P_{\max} \cdot t_c) = -\frac{1}{2}(2V_{dc} i_{\text{load}})\, t_c \qquad (2\text{-}22)$$

During the commutation of the load current, the diode current, I_{D1}, can be expressed as

$$I_{D1} = I_{C1} - i_{\text{load}} \qquad (2\text{-}23)$$

With a negative load current and IC1 going from a value of -iload to zero, the diode current can be approximated as a straight line going from zero to iload. Therefore, the conduction energy loss associated with the commutation of the load current can be approximated as the product of the average diode current, the forward diode voltage drop,

and the time of the commutation, $\frac{1}{2}t_c$.

$$E_{D1,\,\text{turnoff}} = \left(-\frac{1}{2}i_{\text{load}}\right)V_{D1}\left(\frac{1}{2}t_c\right) \tag{2-24}$$

The total turn-off energy loss is

$$E_{\text{turnoff}} = -\frac{1}{2}(2V_{dc}i_{\text{load}})t_c + \left(-\frac{1}{2}i_{\text{load}}\right)V_{D1}\left(\frac{1}{2}t_c\right) \tag{2-25}$$

When all the load current is conducting through D1, the commutation of the load current from Q2 to D1 is complete. The only power loss in this final state of the switching sequence is the commutation loss associated with diode D1. The conduction energy loss for D1 is

$$E_{D1,\,\text{con}} = \int P_{D1}dt = -V_{D1}\int i_{load}dt \tag{2-26}$$

3. ANALYSIS OF ARCP PHASE LEG

3.1 Introduction

An analysis of an ARCP phase leg is presented in this Chapter. This analysis begins with a description of the ARCP circuit. The switching of the load voltage from the lower rail to the upper rail is then explored for three seperate cases: commutation from a diode, commutation from a transistor with low load current, and commutation.from a transistor with high load current. The elimation of the switching losses is discussed in each case.

3.2 ARCP Circuit Description

A circuit diagram of the ARCP phase leg is illustrated in Fig. 3.1 [3]. The ARCP contains snubber capacitors C_r between the load and the dc rails. The snu'bber capacitors serve the purpose of holding the voltage across the switches constant during turn-off. This enables the switch being turned-off to have zero voltage across it during turn-off; thus, eliminating switching losses. The ARCP also includes an auxiliary circuit connected between the dc neutral and phase connection. The auxiliary circuit helps enable the load to be swung to the opposite rail to insure zero turn-on voltage. If the auxiliary circuit is not included, then there is a load current constraint to insure zero turn-on voltage.

3.3 Low-to-High-Commutation-From Diode

An example of an ARCP single phase leg commutation will now be examined in the case were the load will be switched from the lower rail to the upper rail with the diode D2 initially conducting. Initially, the load is connected to the lower dc rail and switch S2 is

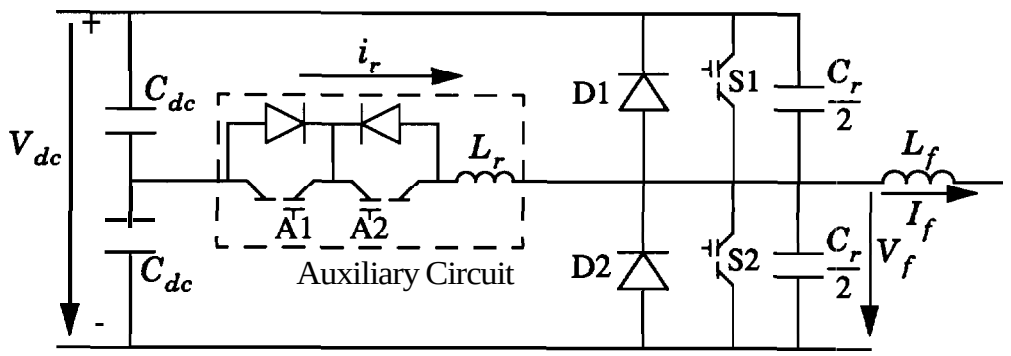

Fig. 3.1. The Auxiliary Resonant Commutated Pole (ARCP).

on as illustrated in Fig. 3.2 (state 1). With the lower switch gated on, the capacitor C_1 has a dc voltage across it. Therefore, the capacitor voltage, V_{C1}, will be constant and the governing differential equation for this state is shown in (3-1). Since the auxiliary circuit is gated off, the auxiliary current, i_r, is zero. The differential equation describing the auxiliary current in state 1 is shown in (3-2).

$$pV_{C1} = 0 \tag{3-1}$$

$$\text{pi,} = 0 \tag{3-2}$$

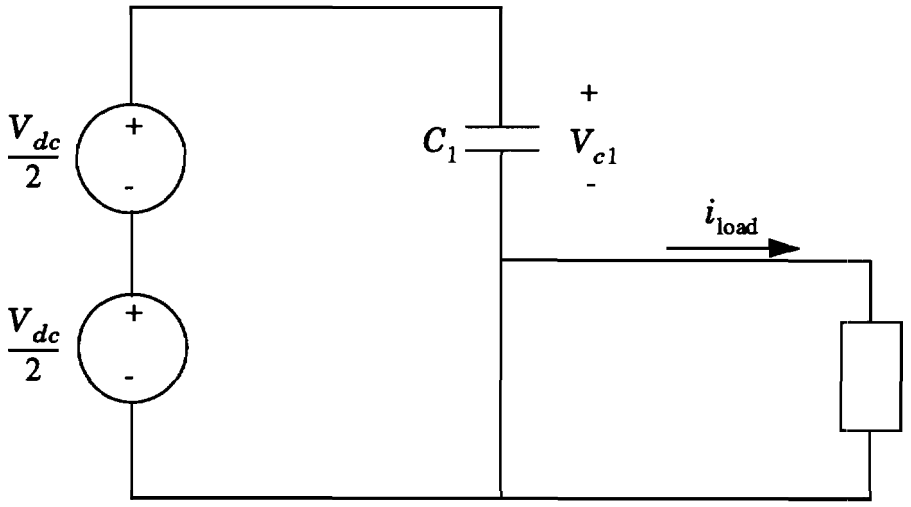

Fig. 3.2. Circuit diagram of ARCP in state 1.

Upon request to switch to the upper rail, the load current is checked. Since the diode is assumed to be conducting in this example, the auxiliary switch A2 is gated on. When A2 is gated on, the auxiliary circuit's inductance does not allow the auxiliary current, i_r, to change instantaneously; hence, the current through A2 remains zero while the gate is being turned on which eliminates losses associated with the turning on of A2. With A2 gated on, the auxiliary circuit is introduced to the circuit as illustrated in Fig. 3.3 (state 2). In state 2, L_r has a dc voltage across it resulting in the auxiliary current ramping up linearly as described by (3-4). The voltage V_{dc} remains across the capacitor C_1 in this state; thus, the governing differential equation for the capacitor voltage is given by (3-3).

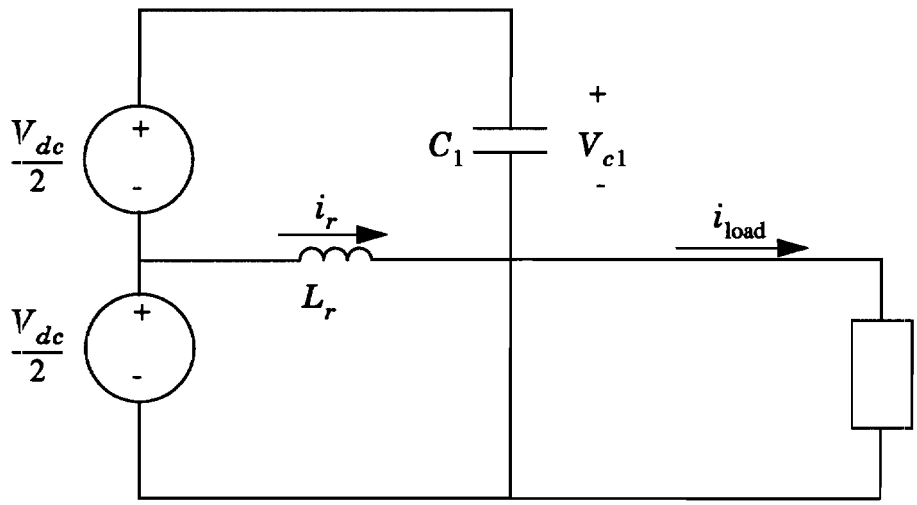

Fig. 3.3. Circuit diagram of ARCP in state 2.

$$pV_{C1} = 0 \tag{3-3}$$

$$pi_r = \frac{V_{dc}}{2L_r} \tag{3-4}$$

This increase in i_r displaces the diode current causing the load current to flow through the auxiliary circuit. When i_r exceeds the load current, the excess current flows through switch S2, $i_r - i_{load}$. When the auxiliary current exceeds the load current plus a boost current, $i_{load} + i_{boost}$, the switch S2 is gated off. The boost current acts to give the auxiliary

circuit additional energy to help insure that the load will swing completely to the upper raiil; thereby, achieving zero voltage turn-on.

Although S2 is gated off, the current through S2 will not immediately go to zero; therefare, if the voltage across S2 is allowed to immediately swing to the upper rail, there will be power loss in the switch because the power loss is the product of the current through the switch and the voltage across the switch. The capacitors are used to eliminate this loss. Since the voltage across a capacitor cannot change instantaneously, the capacitors hold the voltage across S2 at zero until the current in S2 goes to zero; therefore, the product of voltage times current for the switch is zero.

With both switches off and the auxiliary circuit on, the ARCP circuit enters state 3 (Fig. 3.4). Since the load is inductive, the load current is assumed to be constant during a switch; therefore, the excess auxiliary current flows into the snubber capacitors. This places positive charge on the upper plate of the lower capacitor and on the lower plate of the upper capacitor. This charge causes the load voltage to begin to increase. The auxiliary current will continue to increase until the load voltage exceeds the dc neutral voltage then causing the auxiliary current to decrease. When the load voltage reaches the upper rail dc voltage, the diode D1 will become forward biased and switch S1 is gated on; hence, the load is latched to the upper rail.

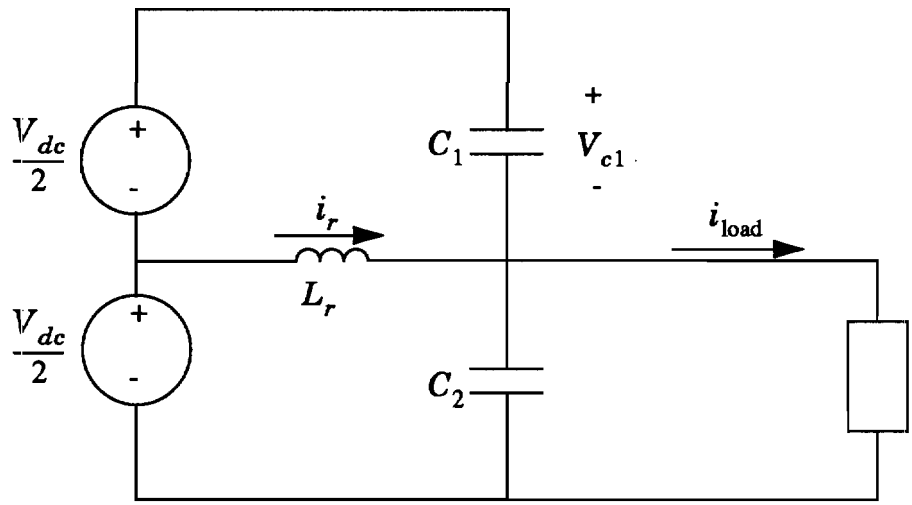

Fig. 3.4. Circuit diagram of ARCP in state 3.

The differential equation for V_{C1} in state 3 can be derived by writing Kirchoff's Current Law (KCL) at the load node (3-5) and Kirchoff's Voltage Law (KVL) around the capacitors and the dc voltage sources (3-6).

$$i_r + C_1(pV_{C1}) - C_2(pV_{C2}) - i_{load} = 0 \tag{3-5}$$

$$V_{C1} + V_{C2} = V_{dc} \tag{3-6}$$

A relationship between pV_{C1} and pV_{C2} can be established (3-7, 3-8) by taking the derivative of both sides of (3-6).

$$p(V_{C1} + V_{C2}) = pV_{dc} = 0 \tag{3-7}$$

$$pV_{C1} = -pV_{C2} \tag{3-8}$$

Substituting (3-8) into (3-5) and simplifying yields the differential equation for V_{C1} shown in (3-10). The differential equation describing i_r in state 3 can be derived by simplifying the KVL equation around the loop including the auxiliary circuit, C_1, and the upper dc voltage source (3-9, 3-11).

$$\frac{V_{dc}}{2} + L_r(pi_r) - V_{C1} = 0 \tag{3-9}$$

$$pV_{C1} = \frac{i_{load} - i_r}{C_1 + C_2} \tag{3-10}$$

$$\text{pi,} = \frac{V_{C1} - \frac{V_{dc}}{2}}{L_r} \tag{3-11}$$

When diode D1 is forward biased and switch S1 is gated on, the snubber capacitors insure that the voltage across S1 remains zero; thereby, eliminating any turn-on loss in switch S1. With the load latched to the upper rail, the auxiliary circuit has a negative voltage across it. Therefore, the auxiliary current will linearly ramp down as described by equation (3-13). With switch S1 gated on, the capacitor voltage V_{C1} is held at zero; thus, the derivative of the capacitor voltage will also be zero (3-12).

$$pV_{C1} = 0 \tag{3-12}$$

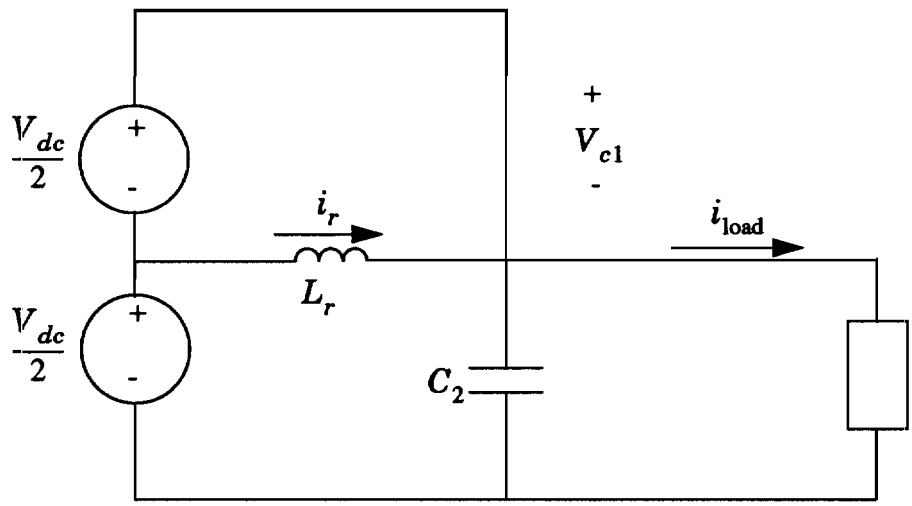

Fig. 3.5. Circuit diagram of ARCP in state 4.

$$pi_r = -\frac{V_{dc}}{2L_r} \tag{3-13}$$

When the auxiliary current reaches zero, switch A2 is gated off. Since the current through A2 is zero when switch A2 is gated off, there is no switching losses associated with A2.

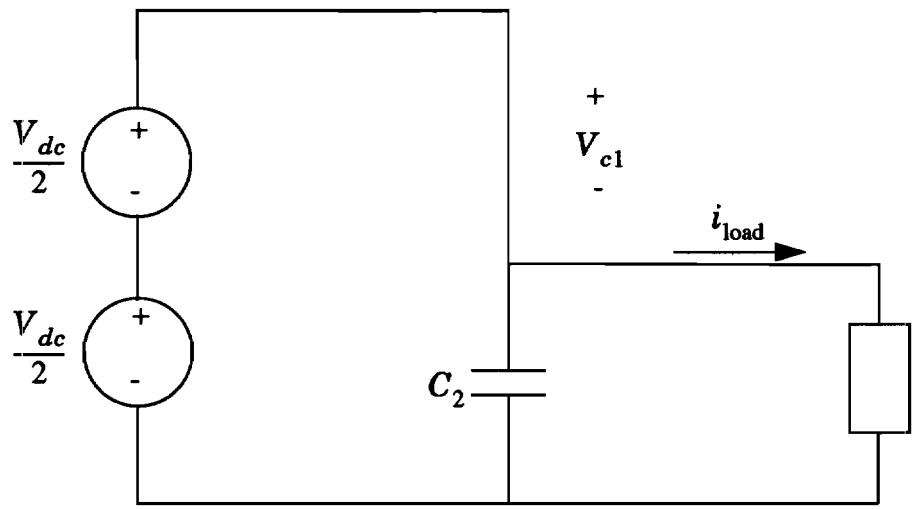

Fig. 3.6. Circuit diagram of ARCP in state 5.

When A2 is gated off, the auxiliary circuit is taken out off the circuit: and the final state is reached with the load being latched to the upper rail. With the auxiliary circuit removed, the auxiliary current is zero; hence, the derivative of the auxiliary current will also be zero (3-15). Since switch S1 is still latched on, the derivative of the capacitor voltage will remain zero (3-14).

$$pV_{C1} = 0 \tag{3-14}$$

$$\text{pi,} = 0 \tag{3-15}$$

A computer simulated plot of the upper capacitor voltage V_{C1} and the auxiliary current i_r is shown in Fig. 3.7 for a switch from low to high with the diode initially conducting. The ARCP parameter values used in the simulation were derived from [3] and are listed in Appendix A. The computer code used in the simulation was written in Advanced Continuous Simulation Language (ACSL) and is shown in Appendix B. Fronn the graph, the individual switching states can be observed along with the transition points between states. Initially, the circuit is latched to the lower rail and the auxiliary circuit is off (state 1). When the auxiliary circuit is gated on, the auxiliary current begins to increase; thus, representing the transition into state 2. When the auxiliary current exceeds the sum of the load current and the boost current, state 3 is entered. In state 3, the load voltage, $V_{dc} - V_{C1}$, is swung from the lower rail to the upper rail. Upon the load voltage reaching the upper rail ($V_{C1} = 0$), the circuit passes into state 4. In state 4,,the auxiliary current decreases linearly. When the auxiliary current equals zero, state 5 is reached. The capacitor voltage, V_{C1}, is not constant during states 2 and 4 as discussed earlier because in the simulation the diodes and switches were not modeled as ideal; thus, a small deviation was introduced.

3.4 Low-to-High Commutation From Switch, Low Current

In the second example of an ARCP single leg commutation, it is assumed that the load voltage is to be switched from the lower to upper rail with switch S2 initially conducting a

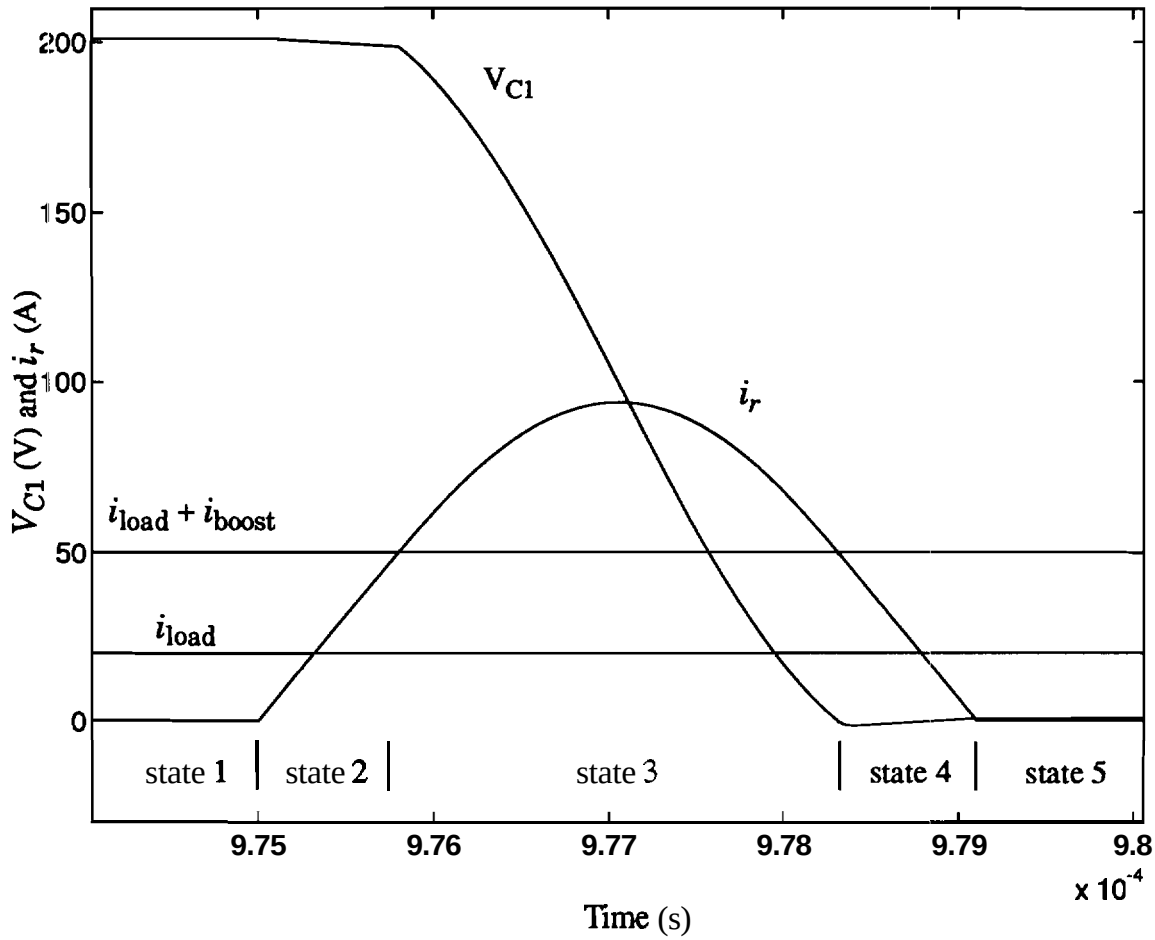

Fig. 3.7. **ARCP** commutation **low-to-high** from **diode.**

small current. The governing differential equations describing each state are the same as in the previous example.

Initially, the load is latched to the lower rail (state 1). When the **ARCP** phase leg is **commanded** to switch to the upper rail, the load current is checked. Since the load current is assumed to be flowing through the switch, the magnitude of the **current** is compared with a threshold value. In this case, it is assumed that the current is less than the threshold **value;** therefore, the load does not contain enough energy to overcome **losses** to drive the load to the opposite rail without the introduction of the auxiliary circuit. Thus, the auxiliary circuit is turned on by gating switch **A2** on.

With the auxiliary circuit gated on, the circuit is in state 2. The auxiliary current will ramp up due to the dc voltage placed across it. When the auxiliary current reaches the value of the boost current plus the load current, the auxiliary circuit has substantial energy to drive the load to the opposite rail. Therefore, the lower switch, S2, is gated off. The snubber capacitors prevent switching losses in S2 because the capacitors hold the voltage across the switch to zero while the switch current diminishes.

State 3 is entered after turning off switch S2. The load current and the auxiliary current will charge the snubber capacitors; hence, driving the load voltage to the upper rail. When the load voltage reaches the upper rail, the diode D1 will become forward biased and will stop further charging of the capacitors by conducting the excess current. When the diode becomes forward biased, the switch S1 is gated on with zero volts across the switch; thereby, preventing any turn-on losses in S1.

When the load voltage is equal to the upper rail, state 4 is obtained. The auxiliary circuit has a negative voltage across it. Therefore, the auxiliary current will ramp down. When the auxiliary current reaches zero, switch A2 is gated off to disconnect the auxiliary circuit. With zero current through A2 during turn-off, switching losses iissociated with A2 are avoided. The load is now latched to the upper rail and the auxiliary circuit is removed; therefore, the commutation is completed and the final state, state 5, is reached.

The upper capacitor voltage, V_{C1}, and the auxiliary circuit, i_r, are plotted in Fig. 3.8 for commutation from the switch in the low-current case. Commutation from the switch at low current levels is similar to commutation from the diode except that:the auxiliary current does not have to become as large in the switch example. This is because the load current aids the commutation process when the switch is initially conducting and hinders commutation when the diode is initially conducting.

3.5 Low-to-High Commutation From Switch, High Current

The final case to be explored involves switching of the load from the lower to upper rail with the switch initially conducting a current larger than the threshold current. Initially, the load is latched to the lower rail and the circuit is in state 1 (Fig. 3.2). For a switch

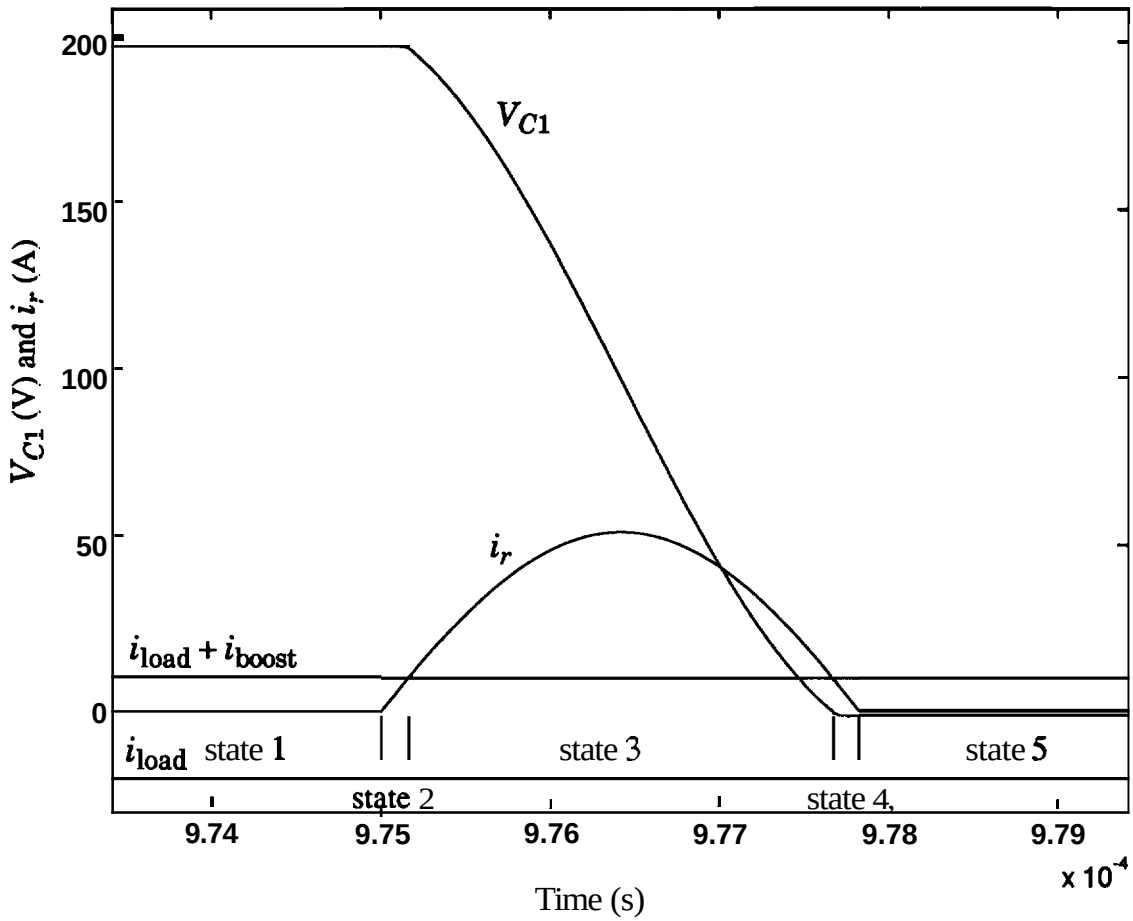

Fig. 3.8. **ARCP** commutation low-to-high from switch (low current).

from the lower rail to the upper rail when switch S2 is conducting a current larger than the threshold value, the auxiliary circuit does not need to be included in the switching sequence. This is a result of the load inductor have sufficient energy to overcome any switching losses and drive the load voltage to the opposite rail. In this case, the **ARCP** acts exactly like a snubber circuit, because switch S2 is gated off without introducing the auxiliary circuit.

Once S2 is gated off, state 6 is entered. In state 6, the load current charges the snubber capacitors and drives the load to the upper rail. When the load voltage reaches the upper rail, diode D1 is forward biased and switch S1 is gated on under zero voltage conditions.

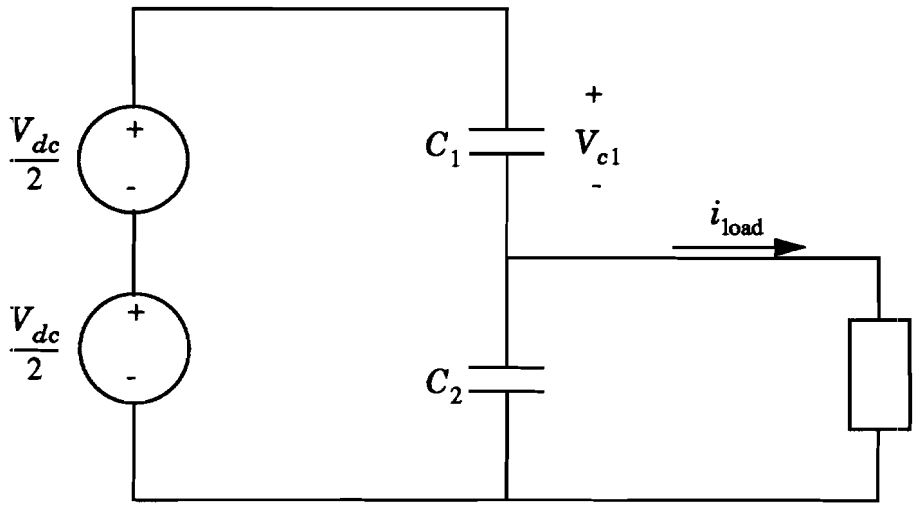

Fig. 3.9. Circuit diagram of ARCP in state 6.

The differential equation characterizing V_{C1} in state 6 can be derived exactly as in state 3 with the auxiliary current neglected (3-16). Since the auxiliary circuit is not gated on in state 6, the derivative of the auxiliary current is zero (3-17).

$$pV_{C1} = \frac{i_{load}}{C_1 + C_2} \tag{3-16}$$

$$\text{pi,} = 0 \tag{3-17}$$

With the load gated to the upper rail, the switching transition is completed. and the circuit is in state 5 (Fig. 3.6).

A plot of the capacitor voltage, V_{C1}, is displayed in Fig. 3.10. Since the load is assumed to be inductive, the load current is assumed to be constant over a switching cycle. Tlherefore, during state 6 the capacitor voltage decrease linearly until the diode D1 is forward bias and conducts the load current.

3.6 Simulation of ARCP Phase Leg

The equations describing the ARCP phase leg have been implemented digitally using the Advanced Continuous Simulation Language (ACSL). The ACSL source code is given in. Appendix B. The ARCP phase leg switch command is given by the ACSL variable `SW1`. When `SW1 = 5`, the output voltage is connected to the upper rail (state 5) or is

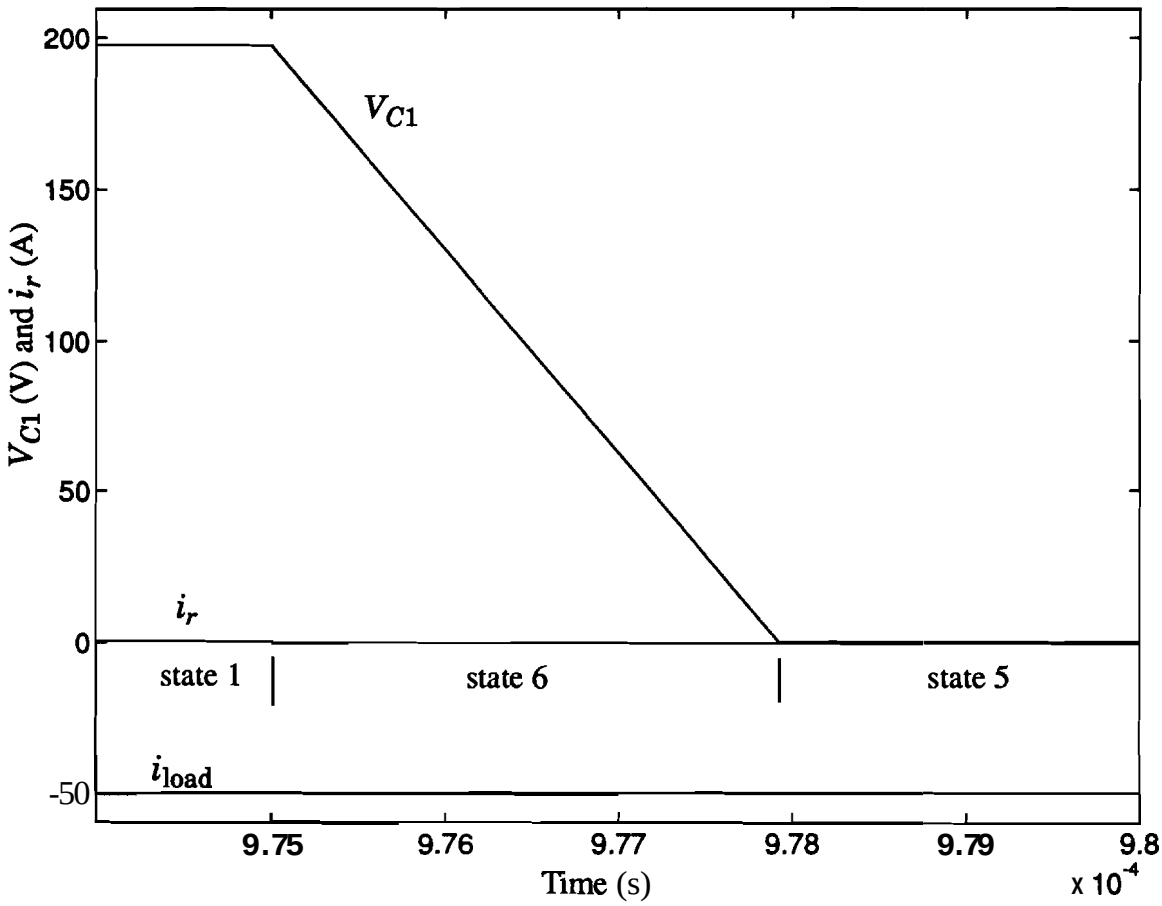

Fig. 3.10. **ARCP** commutation low-to-high from switch (high current).

switching to the upper rail. Likewise, when `SW1 = 1`, the output voltage is connected to the lower rail (state 1) or is switching to the lower rail. The derivatives of the state variables are dependent upon the present state of the phase leg. The present state is given by the variables `state1`. Logic is used to detect a change from one state into the next state, at which a flag is set. This flag calls a discrete block which changes `state1` to its new vidue, calls a data file to log the present value of all the prepare variable, and resets the vidue of the flag. Discrete blocks were used for changes in state because this allowed the state equations to be changed at discrete instances in time. With a switching frequency of 20 kilohertz, 1.36 seconds of central processor time on a Sun Sparcstation 5 were required to run the computer simulation for 5 milliseconds. Computer studies involving the **ARCP** phase leg are described in subsequent chapters.

4. ANALYSIS OF ARCP H-BRIDGE

4.1 Introduction

A comparison of losses is made between an H-bridge circuit using conventional hard-switched phase legs and an H-bridge circuit using ARCP phase legs. Prior to discussing the losses, an H-bridge circuit is discribed along with the pulse-width-modulation control used in this study. Analysis of the ARCP H-bridge is also presented herein.

4.2 Circuit Description and Pulse-Width Modulation

An H-bridge circuit is a load connected between two phase legs. An example of an H-bridge using ARCP phase legs is shown in Fig. 4.1. The load voltage, v_{load}, in an H-bridge can be swung from $+V_{dc}$ to $-V_{dc}$. A positive load voltage can be achieved by having the first phase leg latched to the upper rail and the second phase leg latched to the lower phase leg. A negative load voltage can be obtained by having the first phase leg latched to the lower rail and the second phase leg latched to the upper rail.

Many control strategies may be used to control the load voltage or load current. In this chapter, pulse-width modulation (PWM) will be uses to control the load voltage. In PWM, a controlled sinusoidal waveform which oscillates at the fundamental frequency of the load, f1 (1 kHz), is compared with a triangle wave whose frequency is on the order of ten times larger than f1 to determine whether the load voltage is high or low. If the controlled waveform is larger than the mangle wave, the load voltage is switched positive. If the controlled waveform becomes smaller than the triangle wave, the load voltage is switched negative. Plots showing the controlled waveform, the mangle waveform, and the load voltage are shown in Fig. 4.2 [4].

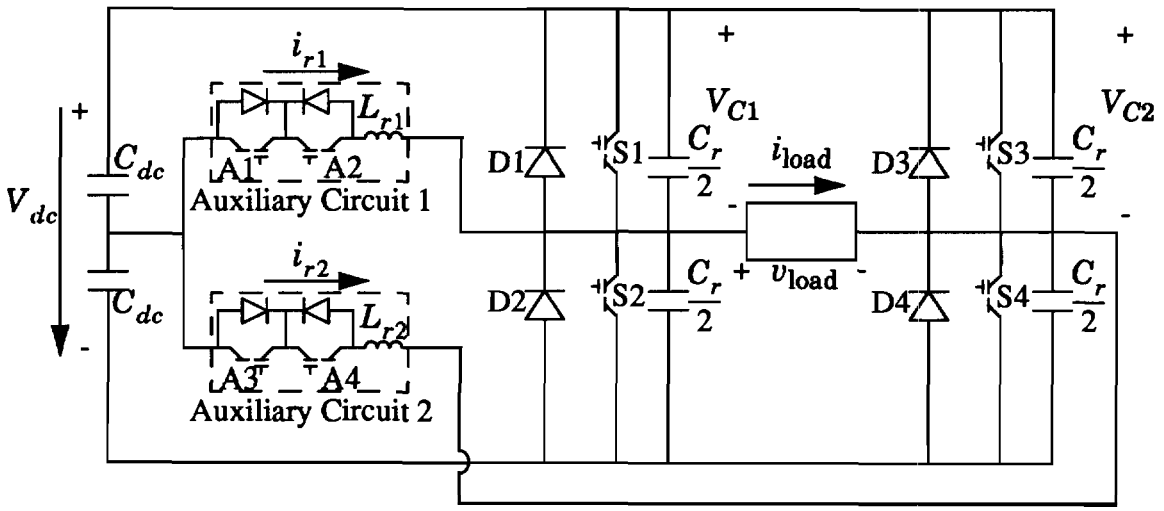

Fig. 4.1. H-bridge using ARCP phase legs.

4.3 H-Bridge Loss Analysis

In this section, a comparison is made between the losses of a hard-switched H-bridge and an H-bridge using ARCP phase legs. In the standard hard-switched converter, the losses will be conduction losses of the transistors and diodes and the switching losses in the transistors. However, in the ARCP converter, the switching losses in the transistors are eliminated at the cost of introducing conduction losses from the auxiliary circuits. The energy loss in the hard-switched converter is explained in detailed in Clhapter 2 with the equations describing the losses shown in (4-1) through (4-4).

$$E_D = \int P_D dt = V_D \int i_{\text{load}} dt \tag{4-1}$$

$$E_{Q,\text{con}} = \int P_{\text{con}} dt = V_{CE,\text{sat}} \int i_{\text{load}} dt \tag{4-2}$$

$$E_{\text{turnon}} = \frac{1}{2}(2V_{dc} i_{\text{load}})\, t_r + \left(\frac{1}{2} i_{\text{load}}\right) V_{D2}\left(\frac{1}{2} t_r\right) \tag{4-3}$$

$$E_{\text{turnoff}} = -\frac{1}{2}(2V_{dc} i_{\text{load}})\, t_c + \left(-\frac{1}{2} i_{\text{load}}\right) V_{D1}\left(\frac{1}{2} t_c\right) \tag{4-4}$$

In the ARCP converter, the conduction losses will be the same; however, the switching

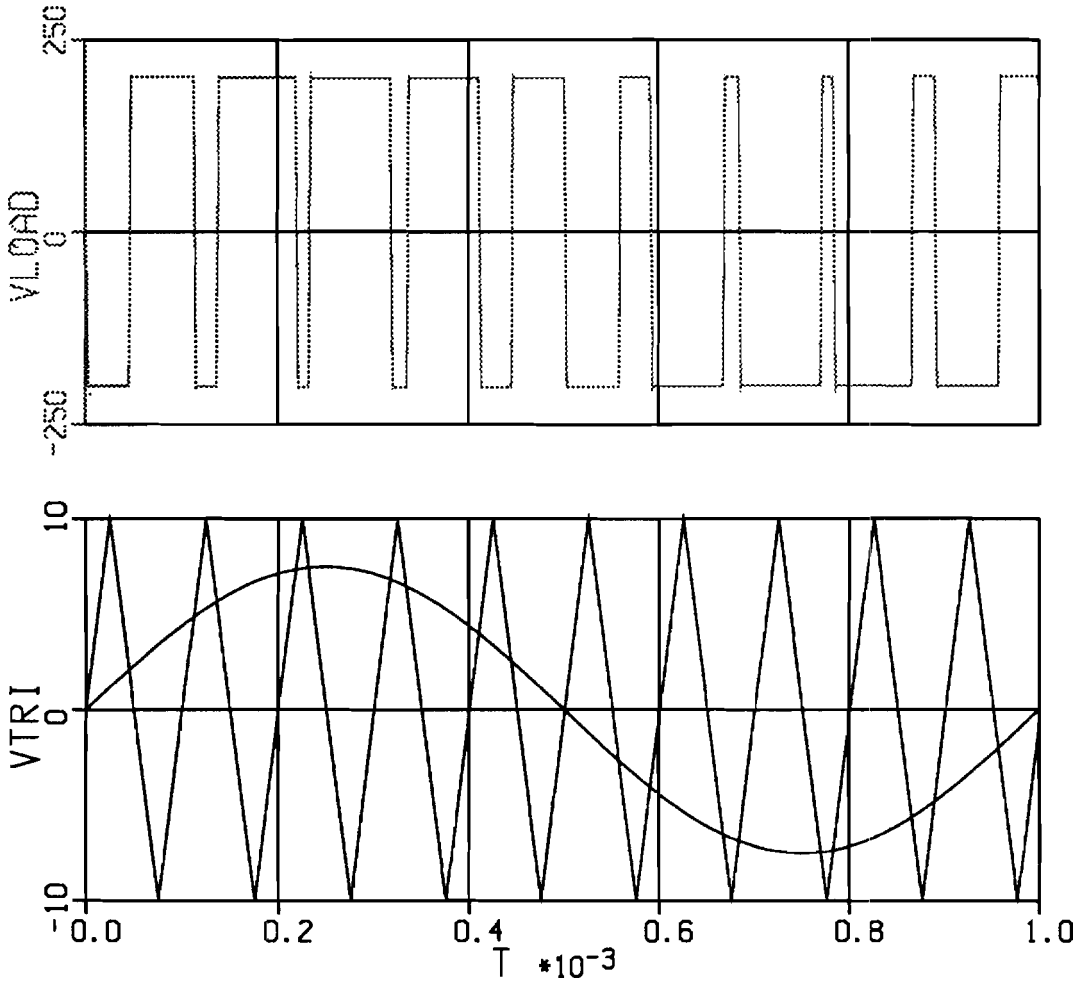

Fig. 4.2. v_{load} versus time and PWM waveforms.

losses shown in (4-3) and (4-4) are replaced by the auxiliary circuit conduction loss (4-5).

$$E_{aux,con} = \int P_{aux,con} dt = V_{CE,sat} \int i_r dt \qquad (4\text{-}5)$$

Plots of the energy loss during one cycle using PWM and an H-bridge with a resistive and inductive-load for both the hard-switched example, `losshs`, and the ARCP example, `lossarcp`, are shown in Fig. 4.3. In this example, the turn-on commutation interval, t_c, and the turn-off rise time interval, t_r, were both set equal to 5 μs which is a typical value for high-power transistors. From the plot, it is shown that through one PWM cycle the

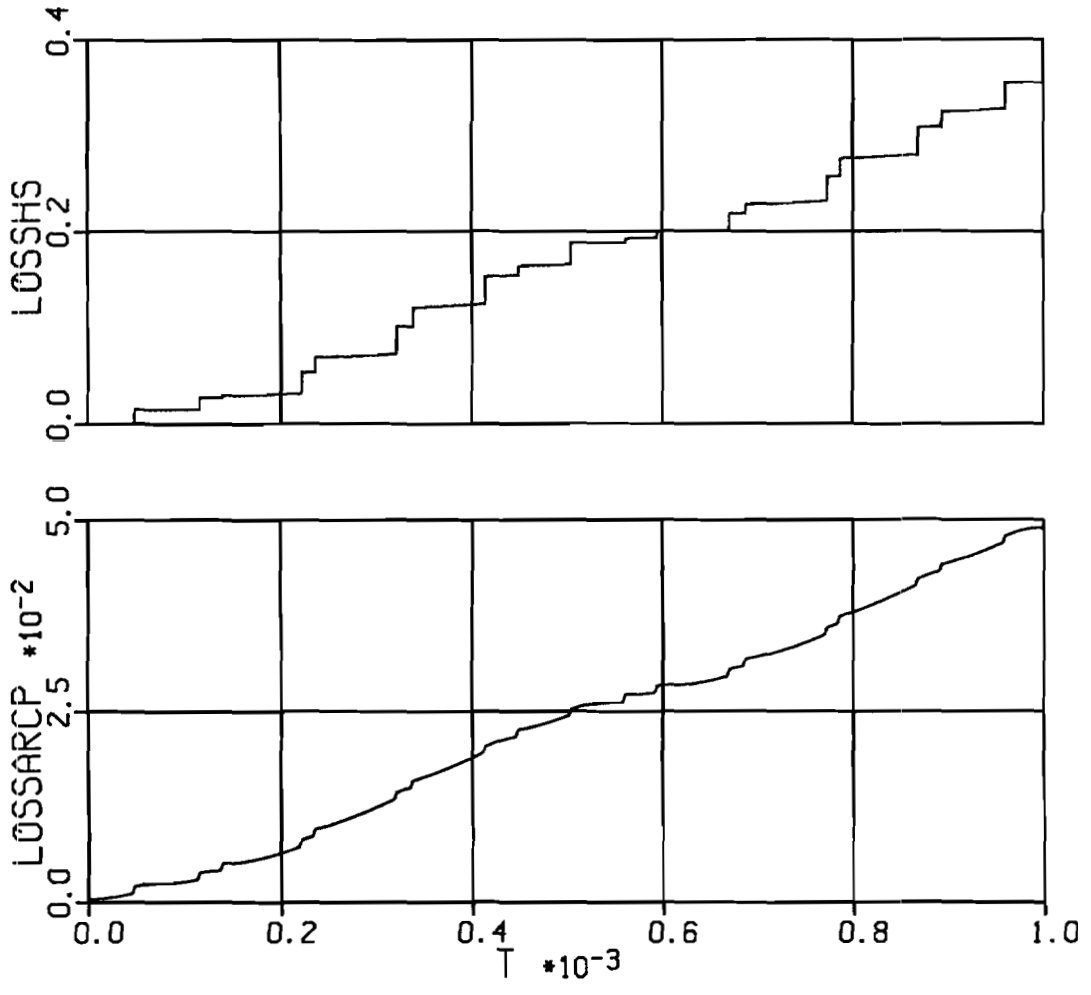

Fig. 4.3. Energy losses for hard-switched and **ARCP** converters.

ARCP H-bridge dissipated about one-nineth the amount of energy of the hard-switched **example** used. This drastic savings in energy, not only allows the application to be more efficient, but also allows the switching circuitry to be reduced is size because of the **elimination** of heat sinks. This reduction in size makes the **ARCP** technology extremely useful in applications were size constraints are the major driving factors.

Plots of the capacitor voltage, V_{C1}, and the auxiliary circuit current, i_{r1}, are shown in Fig. 4.4. The capacitor voltage and auxiliary current for the second **phase** leg is shown in Fig. 4.5. The plots show that the auxiliary circuits are only on during a capacitor voltage

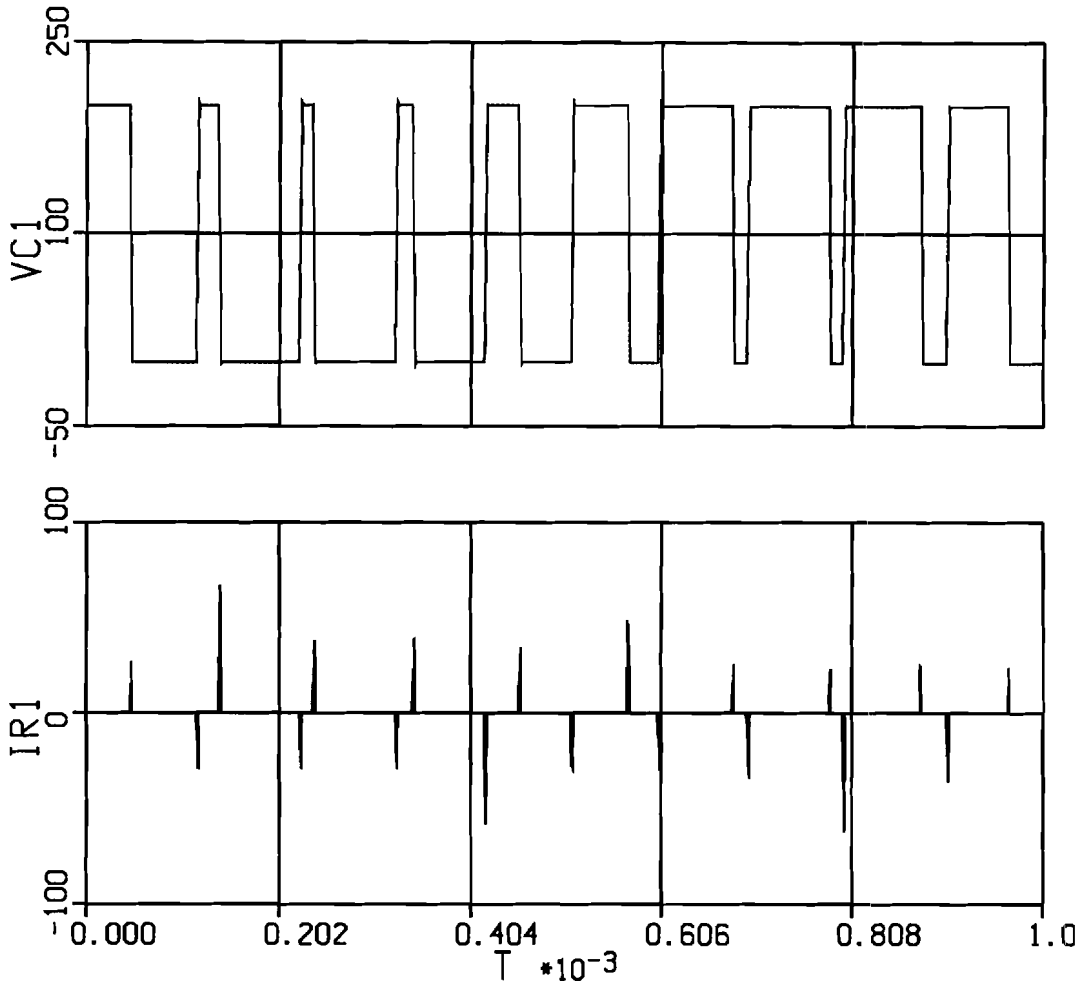

Fig.4.4. ARCP H-bridge example, V_{C1} and i_{r1} versus time.

swing. Therefore, the only time the additional circuitry introduces conduction losses is during the switching interval. Since the auxiliary circuits are turned on during every switching interval, the high current switching case of the ARCP, which allows the voltage to swing from one rail to the opposite rail without the introduction of the auxiliary circuit, is not entered.

Plots of the load current, i_{load}, and the load voltage, v_{load}, for the RL-load are shown in Fig. 4.6. From the plot of the load current, the fundamental frequency of the load is shown to be 1 kHz. This is the same frequency of the control sinusoidal wave used in the PWM control.

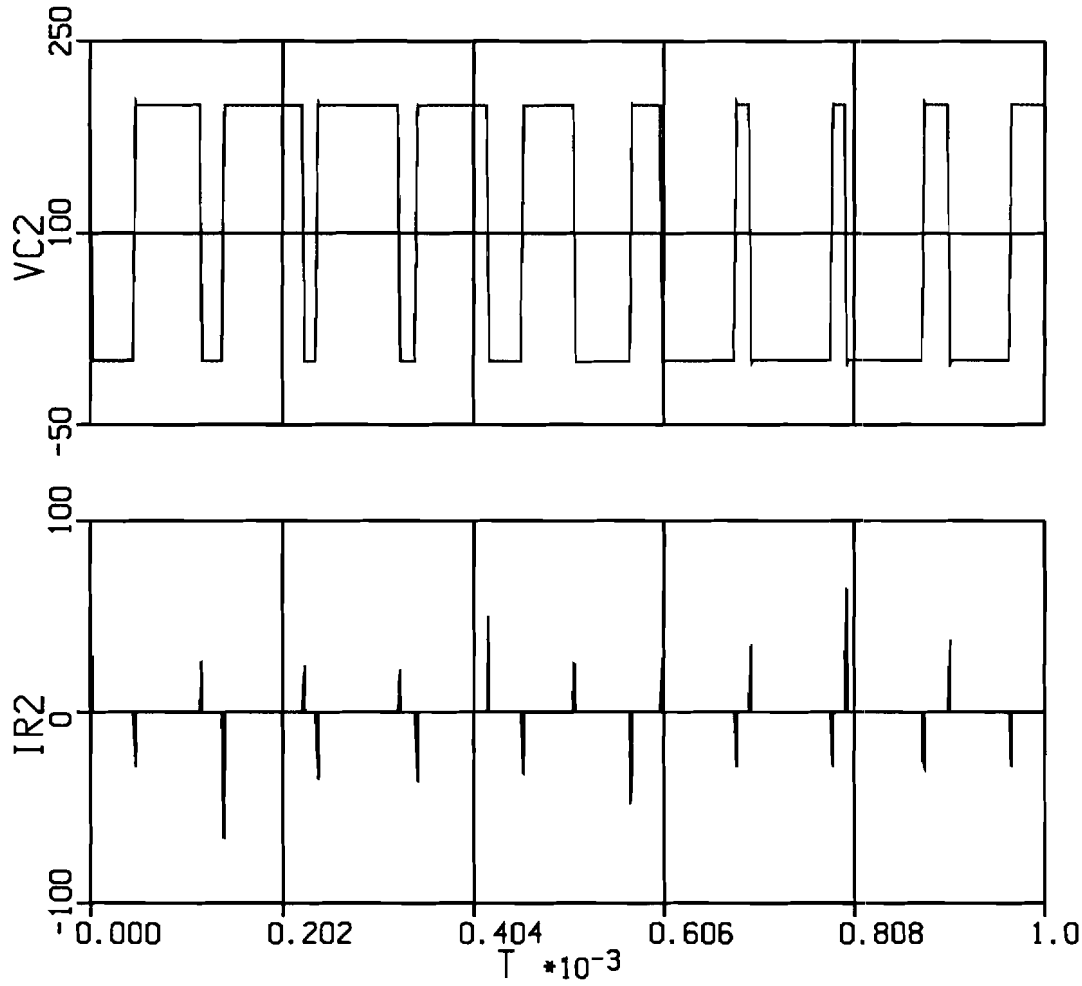

Fig. 4.5. ARCP H-bridge converter, V_{C2} and i_{r2} versus time.

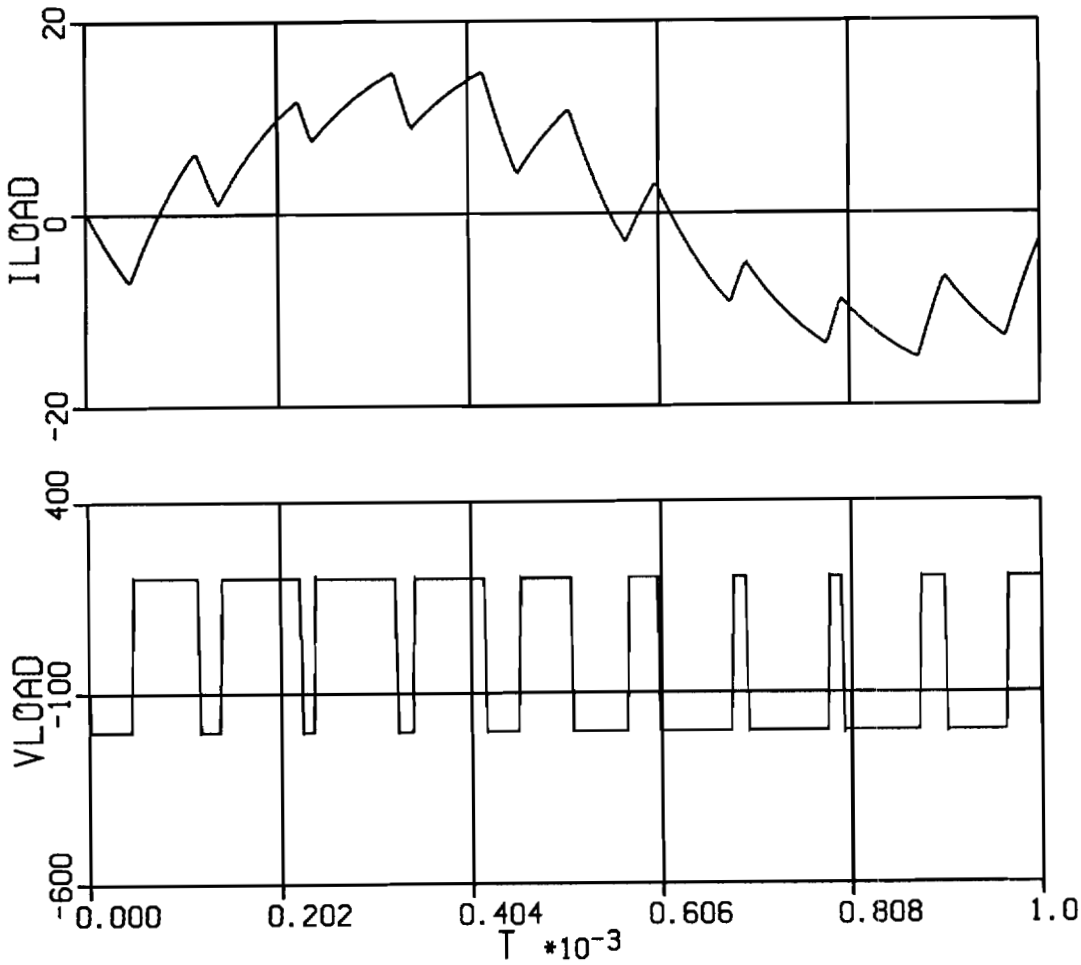

Fig. 4.6. ARCP H-bridge converter, i_{load} and v_{load} versus time.

5. ANALYSIS OF ARCP THREE-PHASE

5.1 Introduction

In this chapter, a variable-speed drive system which includes a three-phase ARCP inverter, a current controller, and an induction motor, is described. A computer simulation of this system has been implemented using ACSL. Results of a computer study using the variable-speed drive system are presented herein.

5.2 Description of ARCP Three-Phase Circuit

A block diagram of the system configuration studied is shown in Fig. 5.1. The current controller is depicted in Fig. 5.2. Therein, $i_{qs}^{e\,*}$ and $i_{ds}^{e\,*}$ are the commanded currents in the synchronously rotating reference frame. The speed of the synchronous reference frame is given by ω_e. The synchronous reference frame variables are transformed into the stationary reference frame by

$$\begin{bmatrix} i_{as}^{*} \\ i_{bs}^{*} \\ i_{cs}^{*} \end{bmatrix} = {}^{e}K_{s}^{s} \begin{bmatrix} i_{qs}^{e\,*} \\ i_{ds}^{e\,*} \end{bmatrix} = \begin{bmatrix} \cos\Theta_e & \sin\Theta_e \\ \cos\left(\Theta_e - \frac{2\pi}{3}\right) & \sin\left(\Theta_e - \frac{2\pi}{3}\right) \\ \cos\left(\Theta_e + \frac{2\pi}{3}\right) & \sin\left(\Theta_e + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} i_{qs}^{e\,*} \\ i_{ds}^{e\,*} \end{bmatrix} \tag{5-1}$$

The actual as, bs, and cs currents (i_{as}, i_{bs}, and i_{cs}) are then subtracted from the commanded as, bs, and cs currents (i_{as}^{*}, i_{bs}^{*}, and i_{cs}^{*}) to produce an enror value i_{ε} for each phase [4]. If the error value is larger than a hysteresis value, the switch signal for thiit phase (SW_a, SW_b, or SW_c) will command that phase leg to switch to the upper rail in

order to increase the current of that phase and to reduce the error value. If the error value becomes more negative than a negative hysteresis value, the switch signal for that phase will command the phase leg to switch to the lower rail; thus, the phase current will decrease and the error value will become smaller in magnitude.

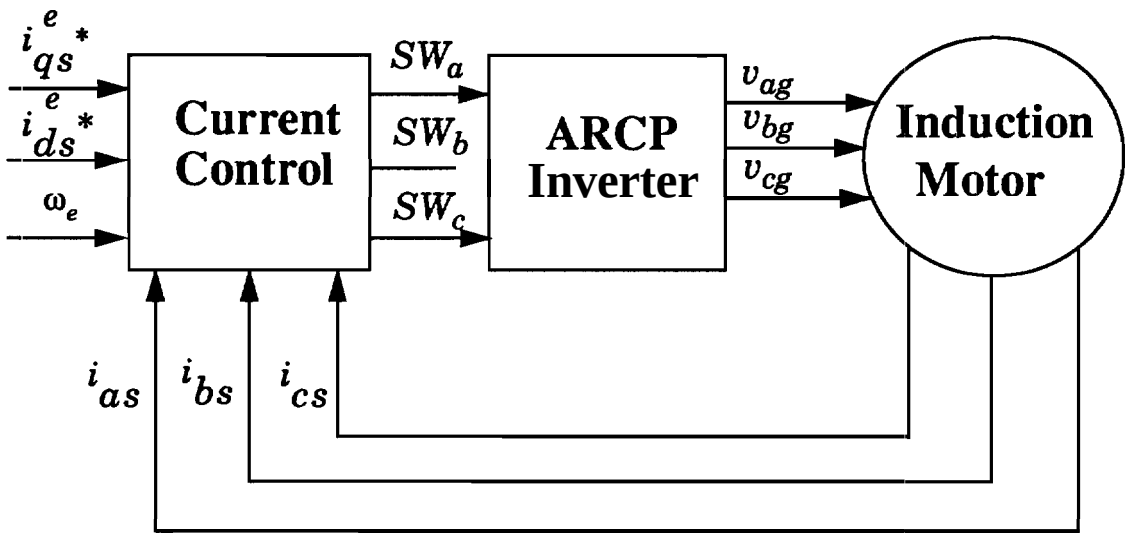

Fig. 5.1. Three-phase example using ARCP inverter:

The switch signals SW_a, SW_b, and SW_c are used to control the a, b, and c phase legs of the inverter, respectively. A circuit diagram of the inverter using ARCP phase legs is shown in Fig. 5.3. The inverter is identical to a conventional inverter except for the auxiliary circuit and the snubber capacitors associated with each phase. The output voltages of the phase legs is used as the three-phase input voltage for the induction motor. These voltages are the voltages between the output phase leg and the lower rail of the inverter. Since the neutral of the induction motor is internal to the motor, the neutral voltage v_n is not equal to the lower rail voltage v_g of the inverter. Therefore, to obtain v„ v_{bs}, and v_{cs} for theinduction-motor-the-followingalgebra must.be applied [5].

$$v_{ng} = v_n - v_g = \frac{1}{3}(v_{ag} + v_{bg} + v_{cg}) \tag{5-2}$$

$$v_{as} = v_{ag} - v_{ng} \tag{5-3}$$

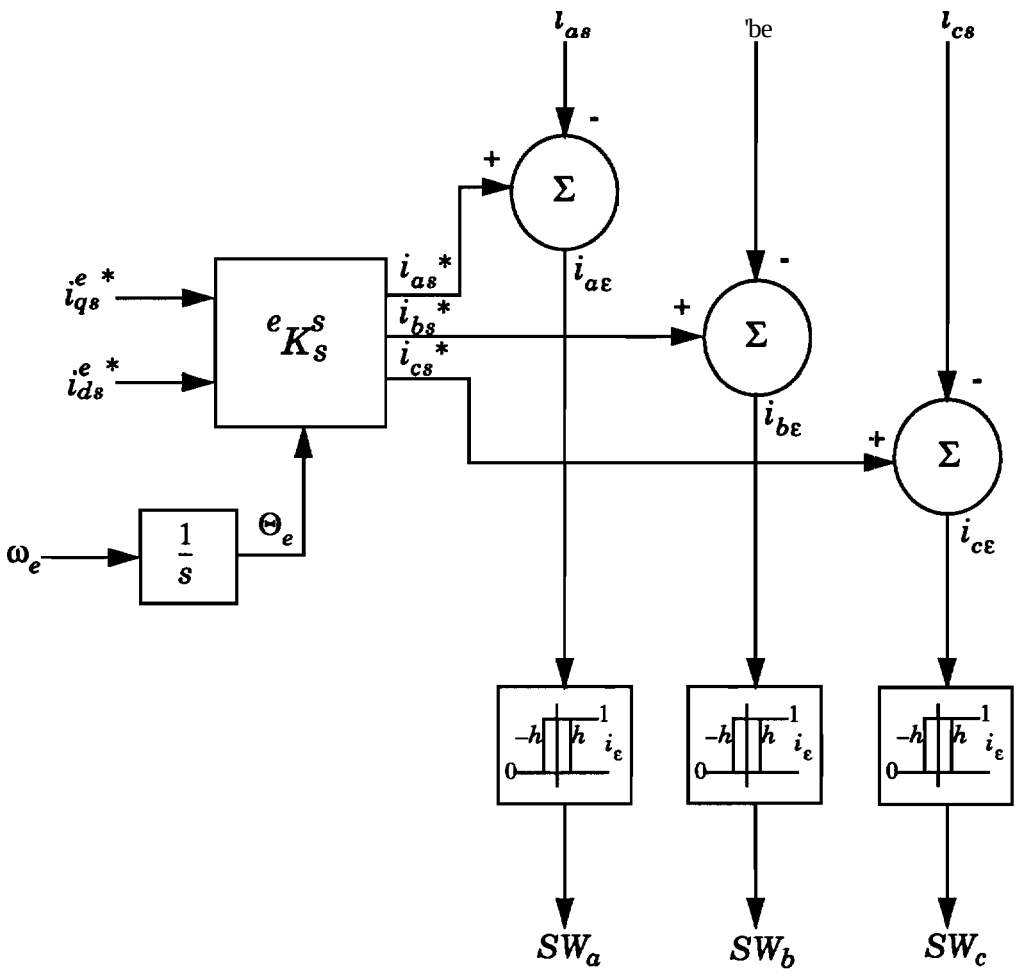

Fig. 5.2. Current control block diagram.

$$v_{bs} = v_{bg} - v_{ng} \tag{5-4}$$

$$v_{cs} = v_{cg} - v_{ng} \tag{5-5}$$

With v_{as}, v_{bs}, and v_{cs} as inputs to the induction motor the phase currents (i_{as}, i_{bs}, and i_{cs}) can be calculated [5]. These phase currents serve as inputs to the current controller.

5.3 Computer Study

In this study, the steady-state characteristics of the three-phase system shown in Fig. 5.1 are established by computer simulation. The parameters of an ARCP phase leg are

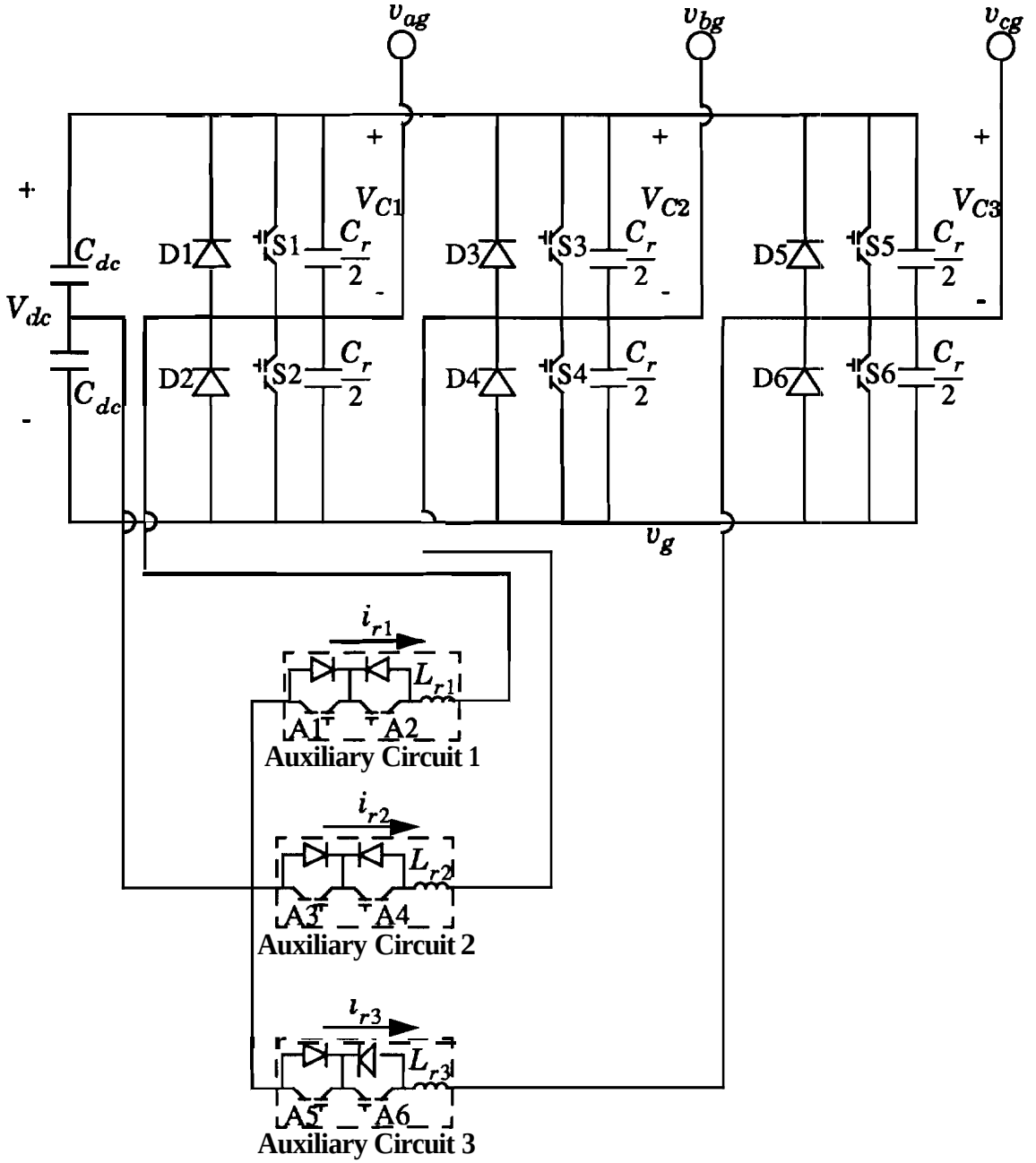

Fig. 5.3. Inverter using ARCP phase legs.

given in Appendix A with the parameters of the induction motor listed in Appendix C [5]. It is assumed that the induction machine is operating at half of rated or base frequency (188.5 radian per second (rad/s)); therefore, the required line-to-neutral voltage is approximately 133 V rms to produce rated torque. The rated slip is 0.05278. Hence, the rotor speed for this study is set to a constant value of 178.6 rad/s.

Plots of the simulated current i_{as} and the commanded current i_{as}^* are shown in Fig. 5.4. These plots were made with a hysteresis value of 7.5 amperes (A) or a tolerance-band of 15 A [4]. The smaller the tolerance-band, the more closely the actual currents will track the commanded currents. However, with this smaller tolerance-biind, the switching frequency of the phase legs will increase because of the increased restrictions on the controls.

The upper capacitor voltage and the auxiliary circuit current for the tz-phase leg is shown in Fig. 5.5. Each spike in the auxiliary current corresponds to commutation from a diode or commutation from a switch in the low-current switch in the a-]phaseleg. Although the capacitor voltage waveform appears to be a square-wave with instantaneous switching, this is a result of the time scale being too large to observe the soft-switching transitions of the capacitor voltages as discussed in Chapter 3. From the: plot of the capacitor voltage, it can be observed that the switching frequency of the phase leg does not remain constant. This is result of the switching frequency depending on how fast the current changes from one side of the tolerance-band to the other, which is not constant due to the: dependence of the current changes on V_{dc}, the back-electromotive force, and the load of the induction motor [4].

Comparing i_{as} from Fig. 5.4 with the auxiliary circuit current for the a-phase in Fig. 5.5, a dependence of phase current on the auxiliary current can be examined. When the phase current is smaller than the threshold value for the ARCP (60 A), every switch is in the low-current case.- In this case the auxiliary current-spikes oscillate from positive to negative since one of the commutations is from a diode and the other from a switch. In the other case, were the phase current is positive and larger than the threshold value, every auxiliary current spike is positive. This is a result of the commutation from the switch

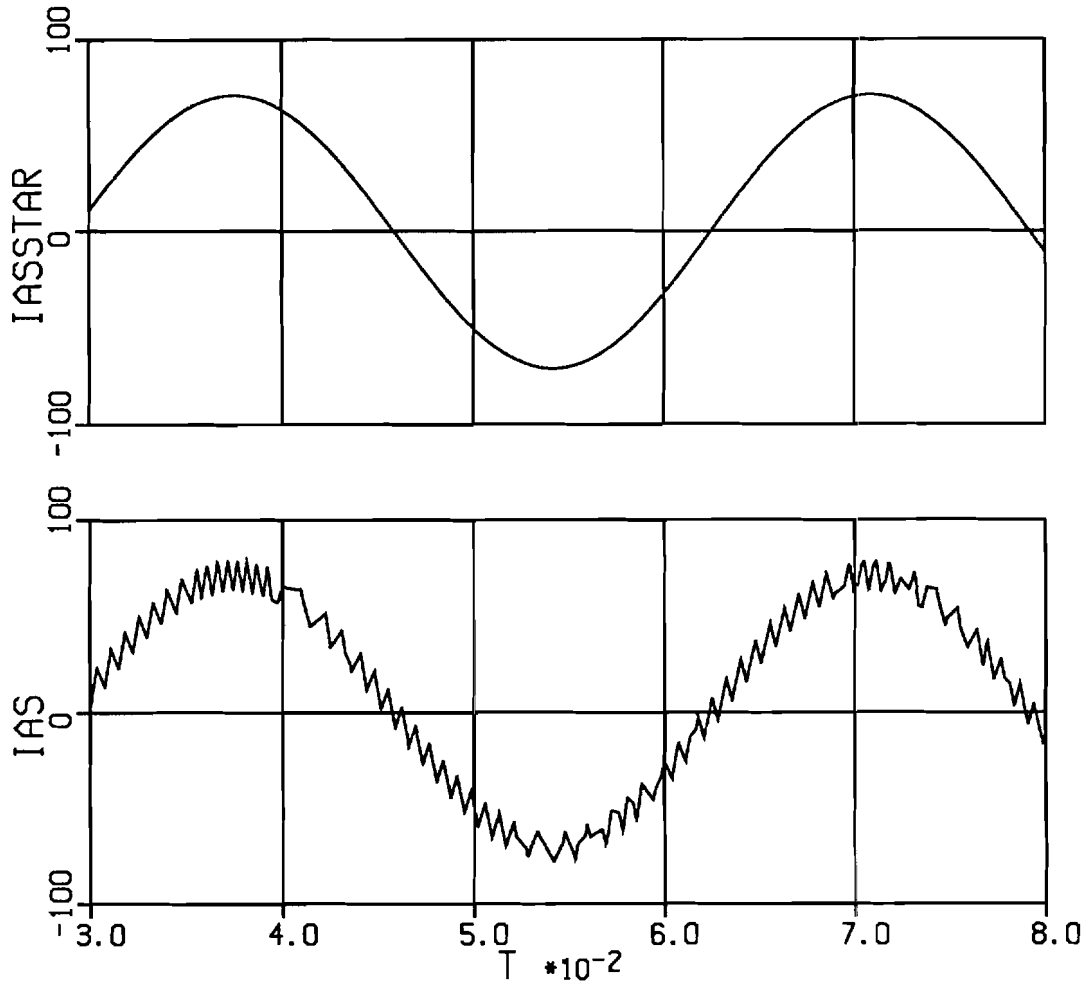

Fig. 5.4. Plots of i_{as} and i_{as}^{*} versus time.

(upper-to-lower transition) not requiring the auxiliary circuit to be turned-on. Therefore, the spikes are all results of lower-to-upper transitions when the current is commutating from the lower diode. When the phase current is negative and larger in magnitude than the threshold voltage, all of the auxiliary current spikes are negative. This is for the same reason as in the previous case except that commutation is from the upper diode in this case.

Plots of the stator voltages (v_{as}, v_{bs}, and v_{cs}) for the induction motor are shown in Fig.

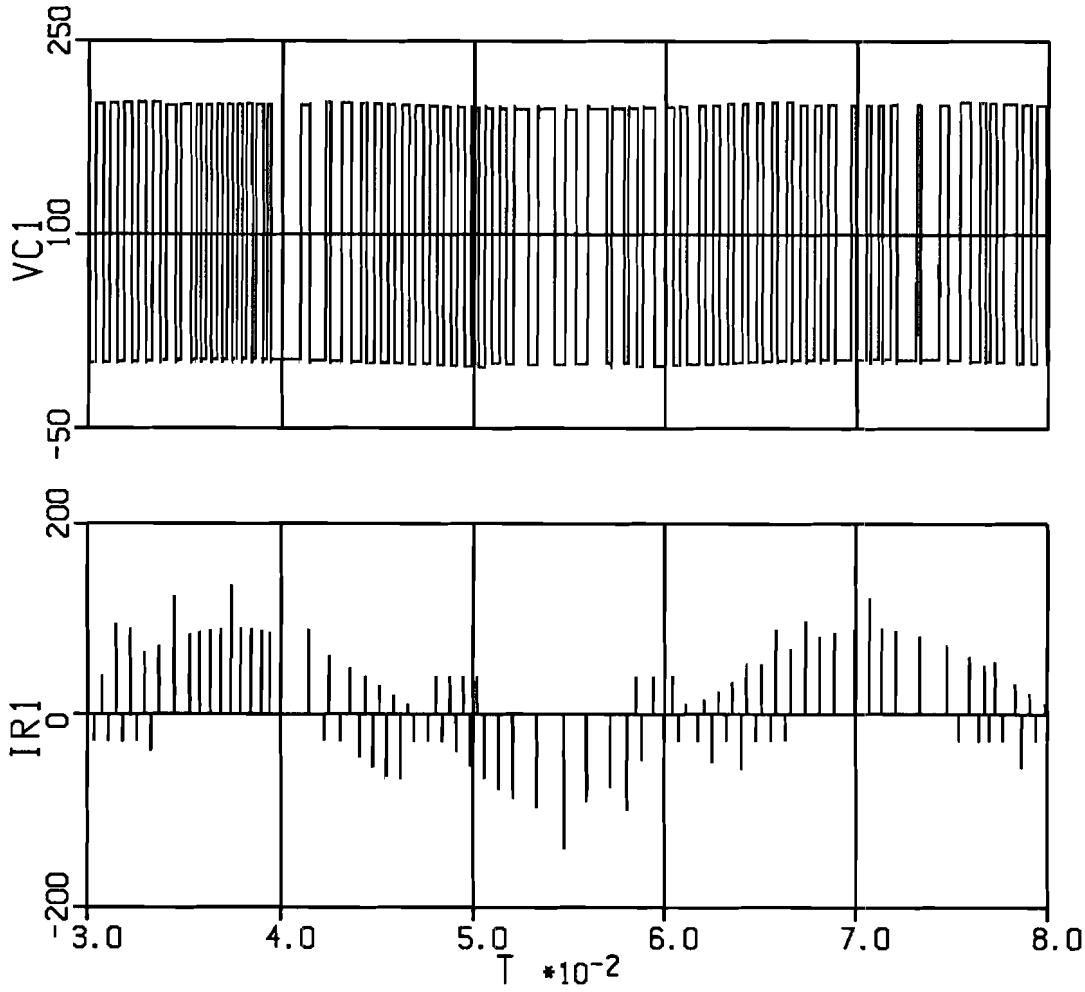

Fig. 5.5. Auxiliary circuit current, i_{r1}, and capacitor voltage, V_{C1}, for the a-phase.

5.6. The peak value of the stator voltages is 133 V, two-thirds of the rail-to-rail voltage of the ARCP. This value is comparable to the rms voltage for the induction motor at half speed.

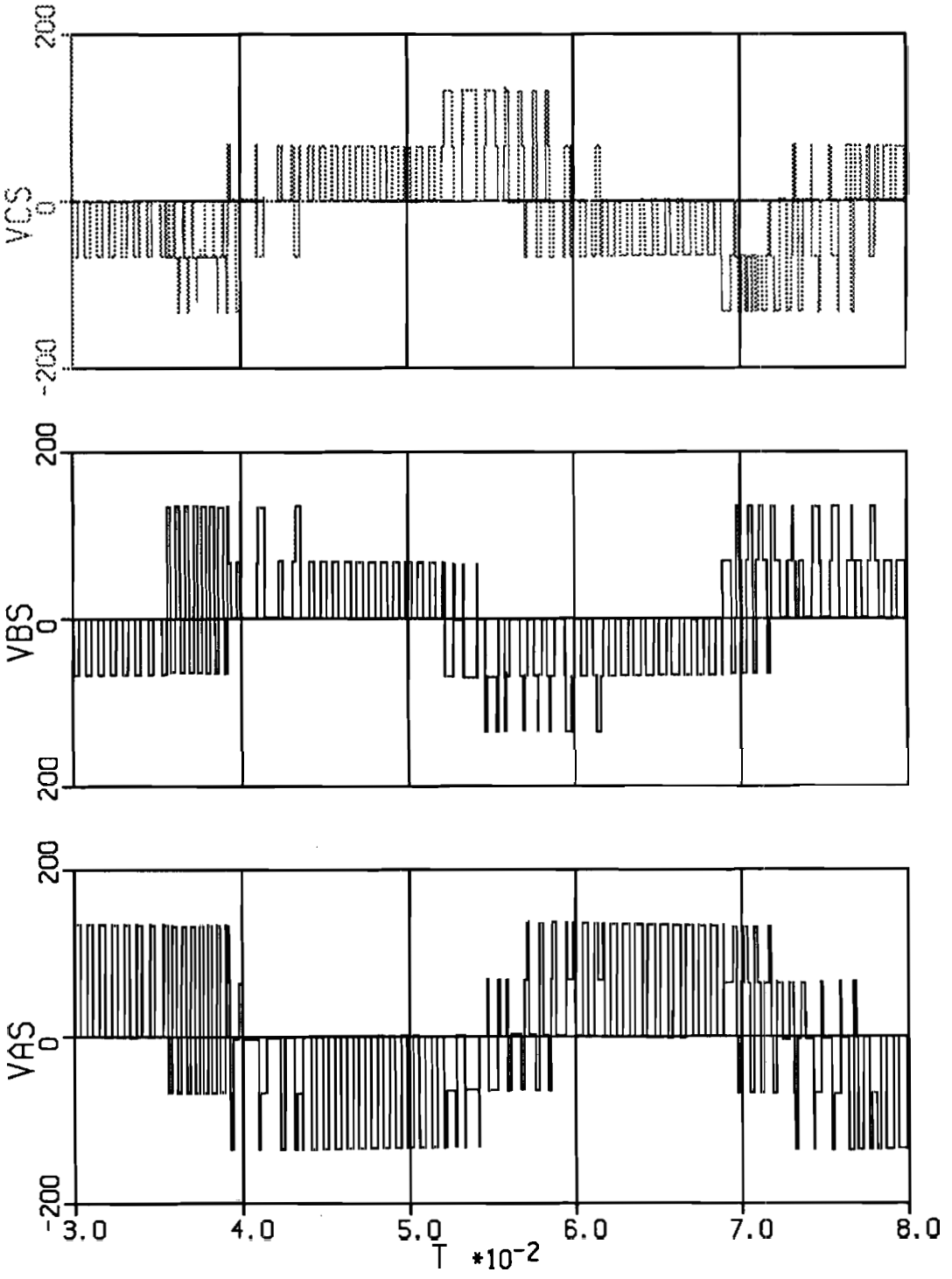

Fig. 5.6. Stator voltages for the induction motor.

6. SUMMARY

In this thesis, the **ARCP** phase leg was described and analyzed. For purposes of comparison, the switching and conduction losses of a conventional hard-switched phase leg were also described. Losses associated with hard-switching include conduction loss and sviitching loss associated with transistor turn-on and turn-off. In an ARCP phase leg, all switching losses are eliminated by turning transistors on and off under either zero current or zero voltage conditions. This is accomplished with the introduction of an auxiliary circuit which aids the commutation process. With the switching losses eliminated, the only losses in an **ARCP** phase leg involve the conduction losses in the phase leg and in the auxiliary circuit.

The switching sequence of the **ARCP** and the corresponding state equations are described in detail in this thesis. Based upon these state equations, computer models of the **ARCP** and hard-switched phase legs were developed and implemented using **ACSL.**

A computer study was performed to compare the losses of **ARCP** and hard-switched switching strategies. In the study, an H-bridge using conventional PWM was analyzed using both types of phase legs and a comparison was made between the energy loss in both cases. It was shown that the **ARCP,** by eliminating switching losses, used approximately one-ninth the energy per **PWM** cycle of the hard-switched converter.

Finally, a variable-speed induction motor drive system using a three,-phase**ARCP** inverter was simulated. The dependence of an **ARCP** phase leg's auxiliary current on the phase current was presented along with a discussion on the relationship between current control parameters and switching frequency.

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[4] N. Mohan, T. M. Undeland, and W. P. Robbins, ***Power Electronics: Converters, Applications, and Design.*** New York: John Wiley & Sons, Inc., 1989, pp. 104-121, 146-148.

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APPENDIX A

ARCP Parameters

Table A.1. ARCP parameters used in simulation.

ARCP Parameter	Value used in simulation
Upper Capacitor, C_1	0.159 μF
Lower Capacitor, C_2	0.159 μF
Resonant Inductor, L_r	0.159 μH
Threshold Current, i_{th}	60 A
Boost Current, i_{boost}	30 A
Rail-To-Rail Voltage, V_{dc}	200 V

APPENDIX B

Advanced Continuous Simulation Language Code For ARCP Phase Leg

```
! Program:  ARCP phase leg
!
! Purpose:  To simulate an ARCP phase leg.
!
! Programmer: Eric Walters
!
! Date: January 17, 1995
!
!-----------------------------------------------
include 'MACROS/leg.mac'
include 'MACROS/per2.mac'
include'MACROS/err3.mac'
include 'MACROS/stchange1.mac'
PROGRAM arcp

   INITIAL
     CONSTANT iload=0.0   ! load current

!---Load parameters and DC voltage parameters----
     CONSTANT Vdc = 200.0    ! DC voltage
!-----------------------------------------------

!---Switch variables-----------------------------
     INTEGER SW1
     SW1 = 1
!-----------------------------------------------
```

```
    CONSTANT maxmaxt = 1.0e-5
    CONSTANT minmaxt = 1.0e-8
  END ! of initial

  DYNAMIC
    MAXTERVAL maxt = 1.0e-5
    MINTERVAL mint = 1.0e-9
    CONSTANT tstop = 1.0e-3
    TERMT (t.ge.tstop)
    ALGORITHM ialg = 3
    CINTERVAL cint = 1.0e-3

    DERIVATIVE main
      SCHEDULE statechangel .XP. intxzerol

      Vload = Vdc - Vcl

      err3(1,xzerol)

      per(SW1)

      leg(1,iload,SW1)

    END ! of derivative

! --- Discrete block to change state and to change maxt --

    DISCRETE statechangel
      stchange(1,xzerol,intxzerol,state1,SW1,nextstatel)
```

```
      END  ! of discrete

!-------------------------------------------------------------

   END ! of dynamic

END ! of program



! --- MACRO for an ARCP leg ----------------------
I
! PROGRAMMER:  Eric Walters
!
! DATE: January 17, 1995

include'MACROS/buffer.mac'

MACRO LEG(z,iload,SW)

   INITIAL
     INTEGER nextstate&z, state&z
     nextstate&z = 1
     state&z = 5
     xzero&z = -1.0
     !flag = -1
     CONSTANT C1&z = 0.159e-6   ! capacitor 1 voltage
     CONSTANT C2&z = 0.159e-6   ! capacitor 2 voltage
     CONSTANT Lr&z = 0.159e-6  ! resonant inductor
     CONSTANT ith&z = 60.0        ! threshold current level
```

```
      CONSTANT iboost&z = 30.0       ! boost current level
      CONSTANT Rswitch&z = 0.05    ! switch resistance in near
volt. case

      CONSTANT Vc&z&ic = 0.0
      CONSTANT iric&z = 0.0

   END ! of initial


   SCHEDULE statechange&z .XP. xzero&z ! calls discrete
block with
                                    ! zero crossing of xzero

   Vc&z = INTEG(pVc&z,Vc&z&ic)     ! Capacitor voltage inte-
gration
   ir&z = INTEG(pir&z,iric&z)      ! Resonant current integra-
tion

   buffer(z,Vc&z,ir&z)


!   err(z,xzero&z)
!--- Procedural to produce zero crossings for sclhedule calls
---

   PROCEDURAL(xzero&z,nextstate&z=...
     iload,Vc&z,state&z,ir&z,SW,ith&z,iboost&z,pVc&z,Vdc)

       xzero&z = -1.0
       nextstate&z = 1
```

```
        IF (state&z .NE. SW) THEN
         GO TO (N&z&1,N&z&2,N&z&3,N&z&4,N&z&5,N&z&6), state&z
N&z&1..      IF (iload .GT. -ith&z) THEN
               nextstate&z = 2
               xzero&z = 1.0
             ELSE
               nextstate&z = 6
               xzero&z = 1.0
             END IF
             GO TO loopend&z

N&z&2..      IF ((ir&z.GT.(iboost&z+iload)) .AND. (SW.EQ.5))
THEN
               nextstate&z = 3
               xzero&z = 1.0
             END IF

             IF ((ir&z .GE. 0.0) .AND. (SW .EQ. 1)) THEN
               nextstate&z = 1
               xzero&z = 1.0
             END IF
             GO TO loopend&z


N&z&3..      IF ((Vc&z .LE. 0.0) .AND. (SW .EQ. 5)) THEN
               nextstate&z = 4
               xzero&z = 1.0
             END IF
```

```
                IF ((pVc&z .GE. 0.0) .AND. (SW .EQ. 5)) THEN
                  nextstate&z = 4
                  xzero&z = 1.0
                END IF

                IF ((Vc&z .GE. Vdc) .AND. (SW .EQ. 1)) THEN
                  nextstate&z = 2
                  xzero&z = 1.0
                END IF

                IF ((pVc&z .LE. 0.0) .AND. (SW .EQ. 1)) THEN
                  nextstate&z = 2
                  xzero&z = 1.0
                END IF
                GO TO loopend&z

N&z&4..         IF ((ir&z .LE. 0.0) .AND. (SW .EQ. 5)) THEN
                  nextstate&z = 5
                  xzero&z = 1.0
                END IF

                IF ((ir&z .LT. -iboost&z) .AND. (SW .EQ. 1)) THEN
                  nextstate&z = 3
                  xzero&z = 1.0
                END IF
                GO TO loopend&z

N&z&5..         IF (iload .LT. ith&z) THEN
                  nextstate&z = 4
                  xzero&z = 1.0
```

```
              ELSE
                nextstate&z = 6
                xzero&z = 1.0
              END IF
              GO TO loopend&z

N&z&6..       IF ((Vc&z .GE. Vdc) .AND. (SW .EQ. 1)) THEN
                nextstate&z = 1
                xzero&z = 1.0
              END IF

              IF ((Vc&z .LE. 0.0) .AND. (SW .EQ. 5)) THEN
                nextstate&z = 5
                xzero&z = 1.0
              END IF
loopend&z..CONTINUE
         END IF

   END ! of procedural
!-------------------------------------------------------------
-----------

!---Procedural to set the derivatives of ir and Vc based on
the state-

   PROCEDURAL(pVc&z,pir&z=...
      state&z,iload,ir&z,Vc&z,Vdc,Rswitch&z,C1&z,C2&z,Lr&z)

       GO TO (M&z&1,M&z&2,M&z&3,M&z&4,M&z&5,M&z&6), state&z
M&z&1..  pVc&z=0.0
```

```
          pir&z=0.0
         ! ir&z=0
         ! Vc&z = 200
          GO TO psetend&z

M&z&2..  pVc&z=((iload-ir&z)+((Vdc-Vc&z)/Rswitch&z))/
(C1&z+C2&z)
          pir&z=(Vc&z-Vdc/2)/Lr&z
          GO TO psetend&z

M&z&3..  pVc&z=(iload-ir&z)/(C1&z+C2&z)
          pir&z=(Vc&z-Vdc/2)/Lr&z
          GO TO psetend&z

M&z&4..  pVc&z=((iload-ir&z)-(Vc&z/Rswitch&z))/(C1&z+C2&z)
          pir&z=(Vc&z-Vdc/2)/Lr&z
          GO TO psetend&z

M&z&5..  pVc&z=0.0
          pir&z=0.0
         ! ir&z=0
         ! Vc&z=0
          GO TO psetend&z

M&z&6..  pVc&z = iload/(C1&z+C2&z)
          pir&z=0.0

psetend&z..CONTINUE
     END ! of procedural
```

```
!-------------------------------------------------------------
-----

MACRO END



MACRO PER(SW)

   INITIAL
     CONSTANT freq = 20.0e3
   END

   PROCEDURAL(SW=freq,t)
     period=1/freq
     remain=mod(t,period)
     IF (remain .LE. period/2) THEN
       SW=1
     ELSE
       SW=5
     END IF
     IF (t .LE. le-6) THEN
       SW=1
     END IF
   END ! of procedural
MACRO END



MACRO BUFFER(z,Vc,ir)
```

```
   INITIAL

        INTEGER i&z
        i&z=3     ! buffer counter
        bufferflag&z = .false.
        delta&z = 0.5
        DIMENSION bufferir&z(2000) ! resonant current leg 1
        DIMENSION buffertime&z(2000) ! time
        DIMENSION bufferVc&z(2000) ! Capacitor volt. leg 1
        bufferVc&z(1) = 0
        bufferVc&z(2) = 0
        bufferir&z(1) = 0
        bufferir&z(2) = 0

   END ! of initial

 !--STORAGE for resonant currents and capacitor voltages -
   PROCEDURAL(i&z,bufferir&z,bufferVc&z, ...
              buffertime&z,bufferflag&z=Vc,ir,t,delta&z)

        IF (i&z .GT. 2000) i&z = 3

        bufferflag&z = .false.

        IF (abs(bufferir&z(i&z-2)-ir) .GT. delta&z) buffer-
flag&z = .true.
        IF (abs(bufferVc&z(i&z-2)-Vc) .GT. delta&z) buffer-
flag&z = .true.

        IF (bufferflag&z .eq. .true.) THEN
```

```
        bufferir&z(i&z) = ir
        bufferVc&z(i&z) = Vc
        buffertime&z(i&z) = t
        i&z = i&z + 1
      ELSE
        buffertime&z(i&z-1)=t
      END IF

  END ! of procedural
!-------------------------------------------------------------
MACRO END



MACRO ERR3(z,xzero)

  INITIAL
    constant k&z=1.0e7
    CONSTANT intxzero&z&ic=-1.0
  END ! of initial

  pintxzero&z = k&z*(xzero-intxzero&z)
  intxzero&z = INTEG(pintxzero&z,intxzero&z&ic)

MACRO END



MACRO STCHANGE(z,xzero,intxzero,state1,SW,nextstate)
```

```
        state&z = nextstate
        xzero = -1
        intxzero = -1
        IF ((state&z.eq.1).OR. (state&z.eq.5)) THEN
          ir&z = 0
          CALL LOGD(.TRUE.)
        END IF

        IF ((state1 .EQ. 2) .OR. (state1 .EQ. 4)) CALL
LOGD(.TRUE.)

        IF (state1 .NE. SW) THEN
          maxt(1)=minmaxt
          CALL RSTART(main,minmaxt)
        ELSE
          maxt(1)=maxmaxt
          CALL RSTART(main,maxmaxt)
        END IF


MACRO END
```

APPENDIX C

Induction Motor Parameters

The following parameters come from [5] on page 190.

Table A.2. Induction motor parameters.

Induction Motor Parameter	Parameter value
r_s	0.087 ohms
X_{ls}	0.302 ohms
X_M	13.08 ohms
X_{lr}'	0.302 ohms
r_r'	0.228 ohms
J	1.662 kilogram square: meters
Rated line-to-line voltage	460 V
Rated slip	0.05278