7-1-2008

Dimensionality in metal-oxide-semiconductor field-effect transistors: A comparison of one-dimensional and two-dimensional ballistic transistors

Raseong Kim
Purdue University

Neophytos C. Neophytou
Purdue University - Main Campus, neophyto@purdue.edu

Abhijeet Paul
Purdue University, abhijeetpaul@purdue.edu

Gerhard Klimeck
Birck Nanotechnology Center, Purdue University, gekco@purdue.edu

Mark S. Lundstrom
School of Electrical and Computer Engineering, Birck Nanotechnology Center, Purdue University, lundstro@purdue.edu

Dimensionality in metal-oxide-semiconductor field-effect transistors: A comparison of one-dimensional and two-dimensional ballistic transistors

Raseong Kim,[a] Neophytos Neophytou, Abhijeet Paul,
Gerhard Klimeck, and Mark S. Lundstrom
Network for Computational Nanotechnology, Purdue University, West Lafayette, Indiana 47907

(Received 29 October 2007; accepted 17 March 2008; published 15 August 2008)

One-dimensional (1D) and two-dimensional (2D) metal-oxide-semiconductor field-effect transistors are compared using an approach based on the top-of-the-barrier ballistic transport model. The results for model devices show that 1D and 2D transistors behave quite similarly if the electrostatics is assumed to be perfect. Distinctive features of 1D transport are difficult to observe at room temperature. The effects of band structure on *I-V* and *C-V* characteristics of Si and InAs nanowire transistors are also examined using the $sp^3d^5s^*$ tight-binding model. It is found that band structure effects in 1D transistors are most distinctively reflected in the drain current versus gate bias or transconductance versus gate bias for low drain bias at low temperatures. Some effects may also be observed in nanowire *C-V* characteristics. © *2008 American Vacuum Society.*
[DOI: 10.1116/1.2908442]

I. INTRODUCTION

Semiconductor nanowires (NWs) are drawing attention due to their potential as next generation metal-oxide-semiconductor field-effect transistors (MOSFETs) and for applications such as transparent/flexible electronic circuits and nanowire sensors.[1–5] In one-dimensional (1D) devices such as NW MOSFETs, novel effects may appear due to quantum confinement. In this article, we address three questions: (i) How is a 1D MOSFET different from a planar MOSFET? (ii) How is the NW band structure reflected in the current-voltage (*I-V*) characteristics? (iii) How is the NW band structure reflected in the capacitance-voltage (*C-V*) characteristics? The 1D and 2D device characteristics are compared using the ballistic top-of-the-barrier model with the effective mass approximation.[6] The effects of band structure on *I-V* and *C-V* characteristics of NW MOSFETs are studied using the ballistic top-of-the-barrier model and the $sp^3d^5s^*$ tight-binding model.[7]

II. PHYSICS OF TRANSISTORS

As a result of continuous scaling, the on current (I_{on}) of present-day silicon technology is quite close to the ballistic limit.[8] A recent study of the SiGe core/shell nanowire FETs also suggests that those devices operate close to the ballistic limit.[9] Therefore, the ballistic current is a useful benchmark to compare device performance.

Accordingly, we use a simple ballistic model for 1D and 2D MOSFETs based on the top-of-the-barrier approach.[6] The potential at the top of the barrier (Ψ_{top}) is determined as

$$\Psi_{top} = \frac{C_G}{C_\Sigma}(-qV_G) + \frac{C_D}{C_\Sigma}(-qV_D) + \frac{C_S}{C_\Sigma}(-qV_S) + \frac{q^2 n}{C_\Sigma}, \quad (1)$$

where C_G, C_D, and C_S refer to the gate, drain, and source capacitances, and $C_\Sigma = C_G + C_D + C_S$.[10] Then, the electron density at the top of the barrier, n, can be calculated from Ψ_{top} and the *E-k* relations. The *E-k* relations of 1D and 2D devices are obtained either from the effective mass approximation or from the tight-binding calculation. After obtaining the self-consistent solutions for Ψ_{top} and n, the ballistic drain current (I_{DS}) can be calculated as described by Rahman *et al.*.[6] Although this simple model does not capture tunneling current or dimension-dependent scattering,[11] it handles essential physics of transistors such as the quantum capacitance effect. Therefore, we believe that this model is a good starting point to answer this: Is there any inherent difference between the 1D and 2D MOSFET characteristics that can be observed in experiments?

The on current is a widely used metric to assess transistor performance, but quoting the on current may not be meaningful unless the power supply voltage (V_{DD}) and the off current (I_{off}) are also specified. Comparing I_{on} becomes more ambiguous for 1D and 2D transistors because the currents are given in amperes and amperes per width, respectively. In the next section, we describe an approach to compare transistors with different dimensionalities.

III. DIMENSIONALITY AND MOSFETS

In this section, we compare *I-V* characteristics, device delay, and internal quantities of 1D and 2D transistors using the top-of-the-barrier ballistic transport model with the effective mass approximation.[6] There is, of course, a clear difference between 1D and 2D transistors in terms of electrostatics. However, we assume perfect gate electrostatics, $C_\Sigma = C_G$, for both 1D and 2D transistors because we would like to address if there is any factor other than the electrostatics that makes 1D transistors inherently different from 2D transistors. As a 1D model device, we take a gate-all-around (GAA) SiNW *n*-MOSFET with 3 nm diameter. As a 2D model device, we take a Si double-gate ultra-thin-body (DG UTB)*n*-MOSFET. The transport direction is [100] for both cases, and only one subband is considered. The valley degeneracies (g_v) for the

[a]Electronic mail: kim369@purdue.edu

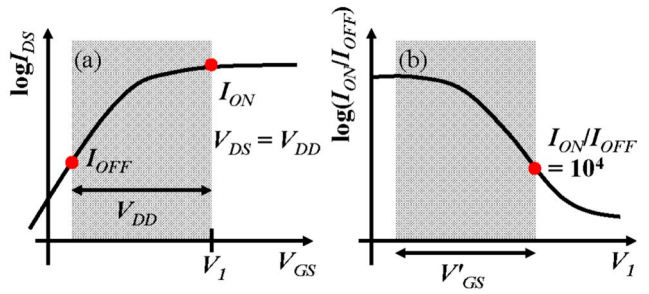

FIG. 1. Approach to compare the performance of 1D and 2D transistors. (a) For a given V_{DD}, the V_{DD} window is swept in I_{DS} vs V_{GS}. The right end of the V_{DD} window is denoted as V_1. (b) For a desired I_{on}/I_{off}, we choose a new gate bias range, V'_{GS}. Then, 1D and 2D transistors are compared in the gate bias ranges that give us the same I_{on}/I_{off}.

1D and 2D devices are 4 and 2, and the effective mass is the transverse effective mass ($m^*=m_t$). The SiO_2 oxide thickness (t_{ox}) is taken as 1 nm, and $V_{DD}=0.6$ V.

To compare the performance of 1D and 2D devices, we select V_{DD} windows to achieve $I_{on}/I_{off}=10^4$ for both cases, as summarized in Fig. 1. We then examine the 1D and 2D device characteristics in the gate bias ranges that give us the same on-off ratio. As a result, devices are compared over gate voltage ranges that give a suitable I_{on}/I_{off} in each case.

Figure 2 shows the I_{DS} versus drain bias (V_{DS}) of 1D and 2D ballistic MOSFETs at $T=77$ K and $T=300$ K. At $T=77$ K, the conductance of the 1D MOSFET is independent of the gate bias (V_{GS}) for low V_{DS}, which is a characteristic feature of 1D transport.[10] However, the 1D and 2D MOSFET characteristics look similar at room temperature.

The ratio of the quantum capacitance (C_Q) to the oxide capacitance (C_{ox}) and the injection velocity (v_{inj}) at $T=77$ K and $T=300$ K are plotted in Figs. 3(a) and 3(b). The ratio, C_Q/C_{ox}, determines how V_{GS} modulates Ψ_{top}. If C_Q/C_{ox} is small, then Ψ_{top} varies a lot with V_{GS}, and higher

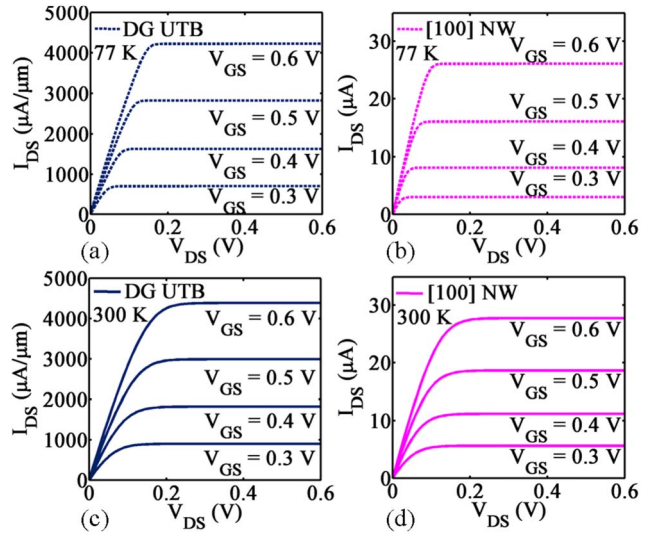

FIG. 2. Simulation results of I_{DS} vs V_{DS} of 1D and 2D silicon n-MOSFETs at $T=77$ K and $T=300$ K. In (c) and (d), the 1D and 2D transistor characteristics look similar at room temperature.

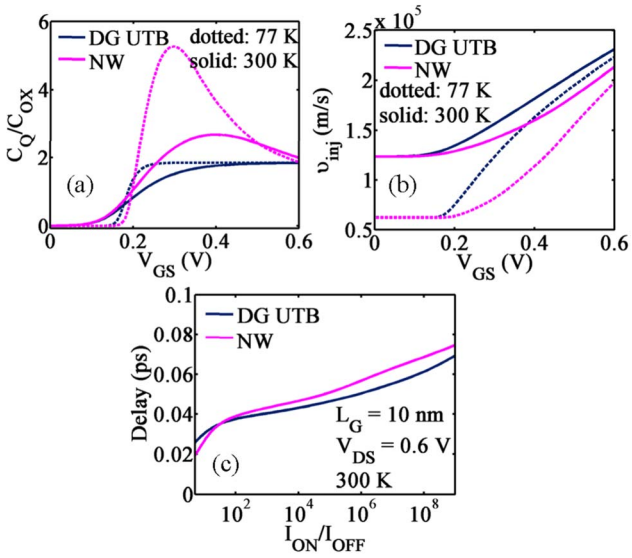

FIG. 3. Simulation results of (a) C_Q/C_{ox} vs V_{GS} at $T=77$ K and $T=300$ K, (b) v_{inj} vs V_{GS} at $T=77$ K and $T=300$ K, and (c) the intrinsic device delay vs I_{on}/I_{off} at $T=300$ K. Device dimension itself makes little difference to the device performance.

energy states can be occupied. Therefore, v_{inj} of the 2D device is observed to be a little higher due to the smaller C_Q/C_{ox}. Due to the van Hove singularity, C_Q/C_{ox} is high for the 1D transistor near turn on, but the ratio is very similar for 1D and 2D MOSFETs at the on state.

The intrinsic device delay (τ) versus I_{on}/I_{off} at $T=300$ K is shown in Fig. 3(c) for both the 1D and 2D MOSFETs. The intrinsic device delay is defined as $\tau=(Q_{on}-Q_{off})/(I_{on}-I_{off})$, where Q_{on} and Q_{off} represent the amounts of charge at the on and off states. The gate length (L_G) is assumed to be 10 nm in both cases. This plot shows that dimensionality itself make little difference to the performance of a MOSFET. Dimensionality does, however, influence the band structure, so we turn to an examination of band structure effects next.

IV. BAND STRUCTURE AND *I-V*

In this section, we examine the band structure effects on *I-V* characteristics of NW MOSFETs using the top-of-the-barrier ballistic transport model. Band structures of [100] Si, [110] Si, and [100] InAs cylindrical NWs calculated from the $sp^3d^5s^*$ tight-binding model[7] are shown in Fig. 4. The diameters are all 3 nm. Figure 4 also shows the m^* and g_v of the lowest subband.

The ballistic *I-V* characteristics of the three GAA n-MOSFETs with $t_{ox}=1.1$ nm are shown in Fig. 5. Figure 5(a) shows I_{DS} vs V_{DS} at $T=300$ K. The threshold voltage of each device was adjusted to have the same I_{off}. The [100] and [110] Si NW results are similar while the InAs NW gives a higher I_{on} and a smaller conductance. For high V_{DS}, the 1D MOSFET current increases with $\eta_F=(E_F-\Psi_{top})/k_BT$, and the current is independent of m^* for a given η_F because the m^* dependencies in the density of states and v_{inj} cancel out.[10] Therefore, a smaller m^* helps obtain a higher current because it leads to a smaller C_Q (larger η_F) for the same V_{GS}.

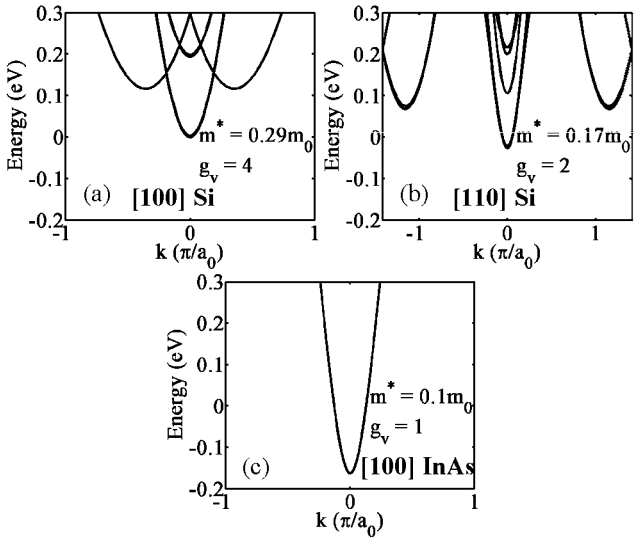

FIG. 4. Band structures of (a) [100] Si, (b) [110] Si, and (c) [100] InAs cylindrical NWs calculated from the $sp^3d^5s^*$ tight-binding model. The diameters are all 3 nm.

The effect of g_v, however, is subtle because a higher g_v gives a higher C_Q while the current is proportional to g_v for a given η_F. The InAs NW gives us a higher I_{on} as a combinational result of the small m^* and g_v. The small channel conductance for the InAs NW comes from the small g_v.

For 1D MOSFETs, I_{DS} increases stepwise with V_{GS} for low V_{DS} at low temperatures. The I_{DS} step heights are proportional to g_v and independent of m^*. To observe these steps, qV_{DS} should be smaller than the subband spacing (ΔE), and ΔE should be larger than k_BT.[12]

Figures 5(b) and 5(c) present the simulation results for I_{DS} vs V_{GS} and transconductance (g_m) vs V_{GS} for V_{DS}=1 mV at

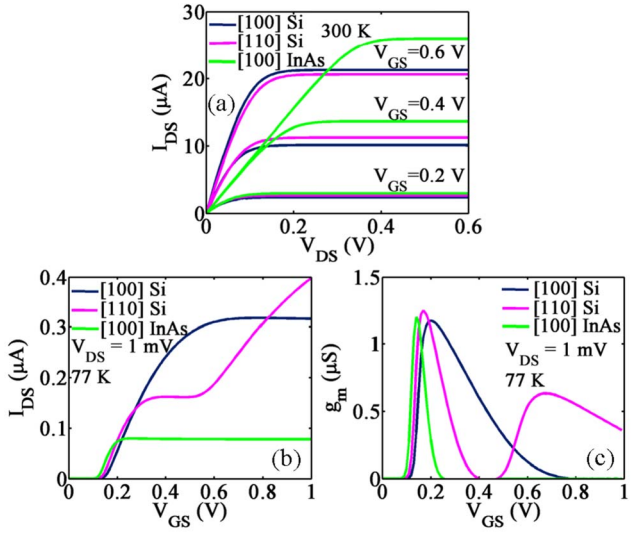

FIG. 5. (a) Simulation results of I_{DS} vs V_{DS} of [100] Si, [110] Si, and [100] InAs NWs at T=300 K. The [100] and [110] Si NW results are similar while the InAs NW gives a higher I_{on} and a lower conductance. Distinctive 1D features are observed in (b) I_{DS} vs V_{GS} and (c) g_m vs V_{GS} for V_{DS}=1 mV at T=77 K. Two subbands are occupied for the [110] Si NW.

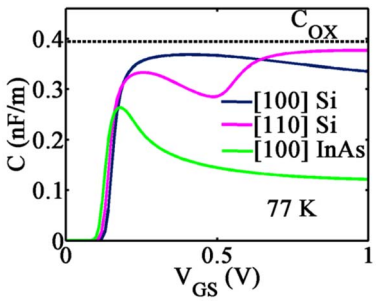

FIG. 6. C-V simulation results of [100] Si, [110] Si, and [100] InAs NWs at T=77 K. A dip is observed in the [110] Si C-V due to the second subband occupation.

T=77 K. Unlike in Fig. 5(a), there is a significant difference between the [100] and [110] Si NWs. For the [110] Si NW, two steps in I_{DS} vs V_{GS} and two spikes in g_m vs V_{GS} are observed, while for the [100] Si NW, only one is seen. This arises because one and two subbands are occupied in the [100] and [110] Si NWs, respectively. The second subband of the [110] Si NW can be occupied because of the smaller g_v, lighter m^*, and smaller ΔE. For the InAs NW, however, only one subband is occupied because of the very large ΔE. In Fig. 5(b), the relative heights of the first I_{DS} steps of [100] InAs, [110] Si, and [100] Si NWs are 1, 2, and 4, which corresponds to the fact that g_v=1, 2, and 4 for each case.

Recent experiments for NW MOSFETs report similar stepwise behaviors in I_{DS} vs V_{GS} for low V_{DS} at low temperatures.[3] As shown by the above simulations, band structure differences of 1D MOSFETs are clearly reflected in I_{DS} vs V_{GS} or g_m vs V_{GS} for low V_{DS} at low temperature. Therefore, measuring these characteristics may be a possible tool for subband spectroscopy.[13]

V. BAND STRUCTURE AND *C-V*

In a recently reported experiment, the capacitance of a single carbon nanotube device was directly measured, and the results reflected 1D band structure effects.[14] Similar 1D effects might be observed in C-V curves for NW transistors. Figure 6 shows the C-V simulation results at T=77 K for the Si and InAs NW MOSFETs considered in Sec. IV. The band structure was computed non-self-consistently, that is, it was computed under flatband conditions and then assumed to be independent of bias. In reality, bias-dependent effects are expected to occur.[15] A dip in the [110] Si C-V is observed, which corresponds to the occupation of the second subband. In practice, parasitic capacitance and surface states may cloud these measurements, and the effects might be more observable in the I_{DS}-V_{GS} characteristics for low V_{DS}.

VI. CONCLUSION

In this work, a simple physical model was employed to determine whether there are any inherent differences between the 1D and 2D ballistic MOSFETs. Electrostatic differences are well understood and not examined in this article.

Simulation results show that 1D and 2D ballistic MOSFETs similarly behave especially at room temperature. The band structure differences arising from the device dimensionality, orientations, and materials are reflected on the *I*-*V* and *C*-*V* characteristics of NW MOSFETs at low temperatures. To better understand the performance trade-offs between 1D and 2D transistors, the role of quantum transport and dimension-dependent scattering should be examined. Although based on a semiclassical ballistic model, the results presented here provide some guidance for observing 1D transport in NW transistors.

ACKNOWLEDGMENTS

This work was supported by the National Science Foundation under Grant No. 0609282. Three of the authors N. Neophytou, A. Paul, and G. Klimeck were supported by the Semiconductor Research Corporation.

[1]C. P. Auth and J. D. Plummer, IEEE Electron Device Lett. **18**, 74 (1997).
[2]N. Singh *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2006**, 547.
[3]K. H. Cho *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2006**, 543.
[4]S. Ju *et al.*, Nat. Nanotechnol. **2**, 378 (2007).
[5]P. R. Nair and M. A. Alam, Appl. Phys. Lett. **88**, 233120 (2006).
[6]A. Rahman, J. Guo, S. Datta, and M. S. Lundstrom, IEEE Trans. Electron Devices **50**, 1853 (2003).
[7]G. Klimeck, F. Oyafuso, T. B. Boykin, R. C. Bowen, and P. Allmen, Comput. Model. Eng. Sci. **3**, 601 (2002).
[8]S. Tyagi *et al.*, Tech. Dig. - Int. Electron Devices Meet. **2005**, 245.
[9]G. Liang, J. Xiang, N. Kharche, G. Klimeck, C. M. Lieber, and M. Lundstrom, Nano Lett. **7**, 642 (2007).
[10]M. Lundstrom and J. Guo, *Nanoscale Transistors: Device Physics, Modeling and Simulation* (Springer, New York, 2005).
[11]S. O. Koswatta, S. Hasan, M. S. Lundstrom, M. P. Anantram, and D. E. Nikonov, IEEE Trans. Electron Devices **54**, 2339 (2007).
[12]J. P. Colinge, W. Xiong, C. R. Cleavetin, T. Schulz, K. Schrüfer, K. Matthews, and P. Patruno, IEEE Electron Device Lett. **27**, 120 (2006).
[13]R. Kim and M. S. Lundstrom, IEEE Trans. Nanotechnol. (to be published).
[14]S. Ilani, L. A. K. Donev, M. Kindermann, and P. L. McEuen, Nat. Phys. **2**, 687 (2006).
[15]N. Neophytou, A. Paul, M. S. Lundstrom, and G. Klimeck, SISPAD, Vienna, Austria, 2007 (unpublished), pp. 217–220.