2002

Metal–insulator–semiconductor electrostatics of carbon nanotubes

Jing Guo
Purdue University

Sebastien Goasguen
Purdue University

Mark S. Lundstrom
Purdue University, lundstro@purdue.edu

Supriyo Datta
Birck Nanotechnology Center and Purdue University, datta@purdue.edu

Metal–insulator–semiconductor electrostatics of carbon nanotubes

Jing Guo,[a] Sebastien Goasguen, Mark Lundstrom, and Supriyo Datta
1285 Electrical Engineering Building, Purdue University, West Lafayette, Indiana 47907

(Received 14 January 2002; accepted for publication 28 June 2002)

Carbon nanotube metal–insulator–semiconductor capacitors are examined theoretically. For the densely packed array of nanotubes on a planar insulator, the capacitance per tube is reduced due to the screening of the charge on the gate plane by the neighboring nanotubes. In contrast to the silicon metal–oxide–semiconductor capacitors, the calculated $C-V$ curves reflect the local peaks of the one-dimensional density-of-states in the nanotube. This effect provides the possibility to use $C-V$ measurements to diagnose the electronic structures of nanotubes. Results of the electrostatic calculations can also be applied to estimate the upper-limit on-current of carbon nanotube field-effect transistors. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1502188]

The carbon nanotube field-effect transistor (CNTFET)[1–3] is a promising candidate for future electron devices. Rapid progress in the field has recently made it possible to fabricate digital and analogue CNTFET-bases circuits, such as logic gates, static memory cells, and ring oscillators.[4,5] To explore the role of CNTFETs in future integrated circuits, it is important to evaluate their performance as compared to the metal–oxide–semiconductor field-effect transistor (MOSFET).[3] A transistor's on-current, an important performance metric, is the product of the charge induced by the gate and the average carrier velocity,[6] so the first step is to understand the gate-controlled electrostatics of a carbon nanotube metal–insulator–semiconductor (MIS) capacitor.

Theoretical studies of carbon nanotube electrostatics have focused on two-terminal devices and the electrostatics along the nanotube direction.[7,8] The planar gate-controlled electrostatics has been treated approximately in experimental studies in order to qualitatively explain or fit measured data.[5,9] In this letter, the MIS electrostatics of carbon nanotube capacitors in three different geometries is analyzed by solving the two-dimensional Poisson equation self-consistently with carrier statistics of nanotubes. The results show that for the densely packed array of nanotubes on a planar insulator, the capacitance per tube is reduced due to the screening of the charge on the gate plane by the neighboring nanotubes. In contrast to silicon, planar MOS capacitors, the capacitance is strongly influenced by the nanotube's one-dimensional density-of-states. The results also show that careful electrostatic design will be critical for the performance of CNTFETs.

The three nanotube capacitors examined in this study, each with a semiconducting nanotube having a diameter of $D=1$ nm, are shown in Fig. 1. In the third dimension (out of the page) the nanotube is assumed to be connected to ground, which supplies the carriers to balance the charge on the gate. For comparison to a silicon MOS capacitor, we assume a silicon doping of $N_A=10^{18}$ cm^{-3}, insulator thickness $t_{\mathrm{ins}}=1$ nm and a dielectric constant of $\kappa_{\mathrm{ins}}=4$. It is important that results be compared at the same gate overdrive, (V_G-V_T), so the gate work functions were selected to produce the same threshold voltage V_T for the CNT and MOS capacitors.

The nanotube capacitance versus gate voltage is computed as follows. For an assumed potential of the nanotube, the charge density, Q_L, was obtained from

$$Q_L=(-e)\cdot\int_{-\infty}^{+\infty}dE\cdot\mathrm{sgn}(E)D(E)f(\mathrm{sgn}(E)[E-\tilde{E}_F]), \tag{1}$$

where e is the electron charge, sgn(E) is the sign function, $D(E)$ is the density-of-states (DOS) of the nanotube[10] and $\tilde{E}_F=eV_{\mathrm{CNT}}$ is the position of Fermi level relative to the middle of the energy gap (we assume an intrinsic nanotube), and V_{CNT} is the average potential of the nanotube. We adopt a semiclassical approach in which the effect of gate voltage is to move the subbands of the nanotube rigidly up and down without changing the $D(E)$, the nanotube DOS. This assumption is valid for the coaxial geometry because the cylindrical symmetry produces the same potential for each carbon atom. But for a planar geometry, potential drops across the nanotube can perturb its band structure.[11] As long as the potential variation across a ~1 nm diameter nanotube is below 0.8 V, the effect is small,[11] so our use of a 0.4 V power supply, as required for high-density digital systems,[12] suggests that band structure perturbations will be small in this case.

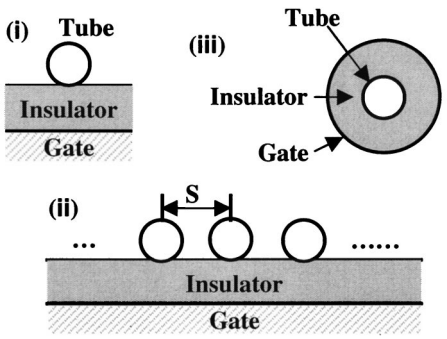

FIG. 1. Three geometries of nanotube MIS capacitors: (i) the single nanotube planar capacitor, (ii) a periodic array of nanotubes, and (iii) the coaxially gated capacitor. Nanotube diameter $D=1$ nm, insulator thickness $t_{\mathrm{ins}}=1$ nm, and a dielectric constant $\kappa_{\mathrm{ins}}=4$ are the same for all capacitors.

[a]Electronic mail: guoj@purdue.edu

Having computed the charge in the nanotube for an assumed nanotube potential, the corresponding gate voltage is

$$V_G' \equiv V_G - V_{\rm fb} = V_{\rm CNT} - Q_L / C_{\rm ins}, \quad (2)$$

where $C_{\rm ins}$ is the gate to nanotube insulator capacitance (a constant independent of gate voltage), V_G is the gate voltage, and $V_{\rm fb}$ the flatband voltage as determined by the gate metal to nanotube work function difference and any insulator–nanotube surface states. Because $V_{\rm fb}$ depends on specifics of experimental conditions, all results will be plotted as a function of V_G' except otherwise specified. By solving Eqs. (1) and (2) self-consistently, the $Q_L(V_G)$ relation is obtained and the gate capacitance is $C_G = -dQ_L/dV_G$. This procedure is analogous to the one commonly used to compute MOS C_G versus V_G characteristics.[6]

Before the C_G versus V_G characteristic can be evaluated, the insulator capacitance must be specified. There is a simple, analytical expression for the coaxial geometry,[13] but planar capacitors require a numerical solution of two-dimensional Poisson equation because two different dielectric constants above the metal plate (the insulator and air) invalidate the simple, analytical expression. The numerical solution was first evaluated for a classical conducting cylinder on the top of an infinite conducting plane with a uniform dielectric material between them, and the result agreed well with the exact analytical solutions.[13] The single nanotube planar geometry, which has two dielectric materials [case (i) in Fig. 1] was then simulated. Two limits were considered: (1) a classical distribution of charge in the nanotube, which assumes the charge redistribute itself to establish an equal potential over the nanotube like a classical metal and (2) a single subband quantum distribution, which assumes that the charge distributes symmetrically around the nanotube. In the classical limit, we find $C_{\rm ins} = 0.61$ pF/cm and in the quantum limit, $C_{\rm ins} = 0.53$ pF/cm.

The significant difference between the classical and quantum limits occurs because the quantum charge distribution (the center of the nanotube) is located further from the metal gate than is the classical charge centroid, and the nanotube diameter is comparable to $t_{\rm ins}$. Note that in most of the experimental planar nanotube capacitors explored to date[1,3] the difference between the classical and quantum limits will be small because the nanotube diameter (typically $\sim$1 nm) is much smaller than insulator thickness (typically $\sim$100 nm). The difference may become important, however, for the very thin insulators that will be used near the scaling limit.

Figure 2 shows the insulator capacitance of an array of parallel nanotubes [case (ii) in Fig. 1] versus the nanotube density, $\rho = 1/S$, where S is the spacing between neighboring nanotubes. For small packing densities, the capacitance per unit area is proportional to the packing density. The largest capacitance per unit area (still 20%–50% below $C_{\rm ins}$ of the planar silicon MOS capacitor) is achieved when the tubes are close packed, but increasing the normalized packing density above 0.5, does not result in the proportional increase of capacitance because each nanotube images to a narrower width and, therefore, a smaller fraction of the charge on the gate. When the nanotubes are closely packed, the capacitance per tube decreases due to the screening of the gate charge by neighboring nanotubes.[14]

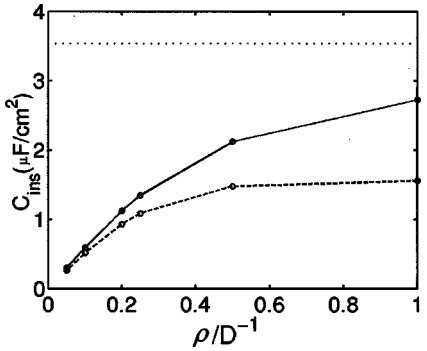

FIG. 2. The insulator capacitance $C_{\rm ins}$ versus the tube density ρ (normalized to $\rho_{\rm max} = 1/D$, the close-packed case) for an array of parallel nanotubes, compared to $C_{\rm ins} = \kappa_{\rm ins}\varepsilon_0 / t_{\rm ins}$ of the MOS capacitor (dotted line). The solid line assumes classical charge distribution, and dash line one subband quantum limit.

Figure 3(a) shows the one-dimensional (1D) charge density Q_L as a function of the effective gate voltage V_G' for the coaxial nanotube capacitor, which provides the optimum geometry for gate control in a MISFET.[15] The charge density is approximately linear with gate voltage above the threshold voltage and can, therefore be expressed as $Q_L \approx C_G(V_G - V_T)$. The effective gate capacitance per unit length, $C_G \approx 1.65$ pF/cm, is only 80% of the insulator capacitance, $C_{\rm ins} = 2.03$ pF/cm, because the gate capacitance is the series combination of the insulator and nanotube capacitance. For very large gate voltages (where our semiclassical treatment needs to be critically examined), electrons occupy the second

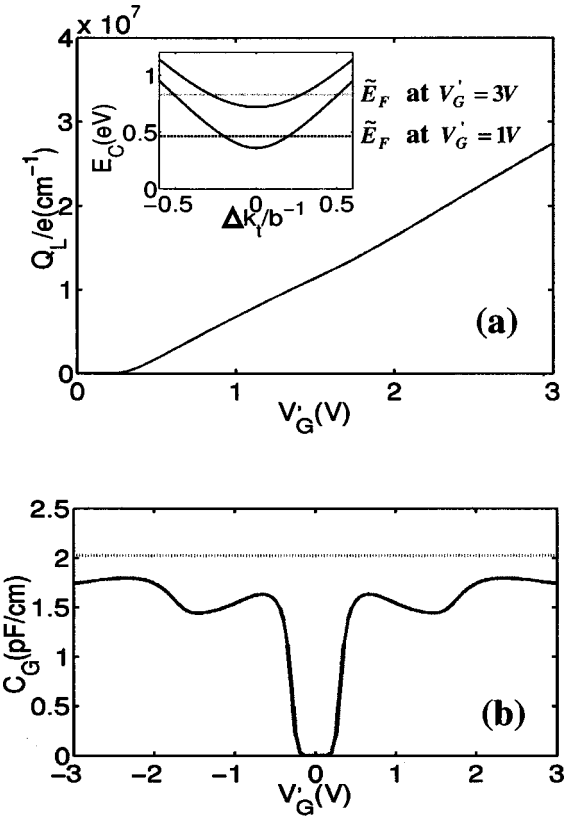

FIG. 3. Charge vs. gate voltage for the coaxial capacitor, (a) charge density Q_L and (b) the gate capacitance C_G versus the effective gate voltage V_G'. The inset in (a) shows location of the Fermi level in the first and second subbands at $V_G' = 1$ V, and 3 V. The dotted line in (b) indicates the insulator capacitance $C_{\rm ins}$.

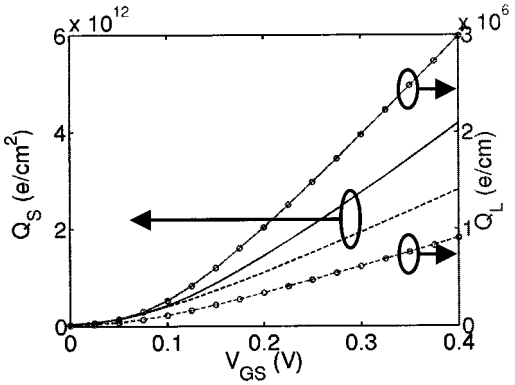

FIG. 4. Charge density vs. gate voltage V_G. On the left axis, the close-packed array of nanotubes (dashed line) is compared to the silicon MOS capacitor (solid line). On the right axis, the coaxially gated capacitor (solid line with circles) is compared to the single nanotube planar geometry (dashed with circles). To make a fair comparison, the gate workfunction of each capacitor is adjusted to produce a common threshold voltage, $V_T \approx 0.1$ V.

conduction band as shown in the inset of Fig. 3(a). The subband spacing decreases with increasing nanotube diameter, but for typical diameters of about 1 nm and operating voltages of <0.5 V, only a single subband will be occupied. The one-subband approximation, therefore, can be used in the calculation.

Figure 3(b) shows the computed C_G versus V_G characteristic of the coaxial nanotube capacitor. The striking difference from that for a MOS capacitor on an intrinsic substrate is due to the 1D DOS of the nanotube. The origin of local maxima is apparent when the nanotube capacitance is calculated at zero temperature $C_{\mathrm{CNT}}\ (V_{\mathrm{CNT}}) = -dQ_L/dV_{\mathrm{CNT}} = e^2 D(eV_{\mathrm{CNT}})$, where $D(E)$ is the DOS of the nanotube. Although the peaks in the 1D DOS are smoothed out by temperature, and the insulator capacitor in series, they still display local maximums on the $C-V$ curve at room temperature. Experimental measurement of $C-V$ curves, especially at low temperature using liquid-ion gating[9] which provides a high insulator capacitance, could generate useful diagnostic information on the DOS of the nanotube.

Figure 4 is an attempt to compare silicon MOS capacitors with carbon nanotube MIS capacitors. The MOS C_G versus V_G characteristic was computed by a self-consistent Schrödinger–Poisson solver so that quantum confinement effects were included.[16] The same threshold voltage V_T, and the power supply voltage V_{DD}, were assumed for all capacitors. On the left axis, we show that the effective gate capacitance of the nanotube array (the slope of the curve above threshold) is 66% of that of the silicon MOS capacitor because geometrical effects and quantum charge distribution reduce the insulator capacitance, as discussed earlier. (For thicker gate insulator, a planar nanotube capacitor can outperform the corresponding silicon MOS capacitor because the capacitance decreases more slowly with the insulator thickness in the nanotube case.[3]) The performance of planar nanotube capacitors may be improved by embedding nanotubes inside the gate insulator,[14] which results in comparable performance to the silicon, planar MOS capacitor. On the right axis, we compare the charge for a single tube in a planar geometry, case (i) in Fig. 1, to that in a coaxial geometry. The results show a clear advantage for the coaxial geometry and suggest that careful electrostatic design should be important for CNTFETs.

In summary, we have presented numerical studies of the MIS electrostatics of carbon nanotube capacitors and have shown that the capacitance versus voltage characteristics are quite different from those of standard, planar, silicon MOS capacitors. The difference arises from the 1D density of states in the nanotube, which leads to local maxima in the C_G versus V_G characteristic. We show that the planar nanotube capacitors offer comparable performance to the silicon MOS capacitors, but the coaxial gate geometry promises significantly higher performance. These results support a recent study based on a drift-diffusion analysis, which suggests that CNTFETs can be competitive with MOSFETs.[3] The electrostatic calculations also allow us to estimate the upper-limit on-current of CNTFETs based on a simple 1D model.[17,18]

This material is based upon work supported by the National Science Foundation under Grant No. 0085516. Helpful discussions with M. P. Anantram of NASA Ames Research Center and P. McEuen, Cornell, through the MARCO /DARPA Focus Center on Materials, Structures, and Devices are also acknowledged.

[1] R. Martel, T. Schimidt, H. R. Shea, T. Hertel, and Ph. Avouris, Appl. Phys. Lett. **73**, 2447 (1998).
[2] W. Choi, J. Chu, K. Jeong, E. Bae, and J. Lee, Appl. Phys. Lett. **79**, 3696 (2001).
[3] R. Martel, H.-S. P. Wong, K. Chan, and P. Avouris, Tech. Dig. Int. Electron Devices Meet. **2001**, 159 (2001).
[4] V. Derycke, R. Martel, J. Appenzeller, and Ph. Avouris, Nano Lett. **9**, 453 (2001).
[5] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, Science **294**, 1317 (2001).
[6] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices* (Cambridge University Press, Cambridge, UK, 1998).
[7] F. Leonard and J. Tersoff, Phys. Rev. Lett. **83**, 5174 (1999).
[8] A. Odintsov, Phys. Rev. Lett. **85**, 150 (2000).
[9] M. Kruger, M. Buitelaar, T. Nussbaumer, and C. Schonenberger, Appl. Phys. Lett. **78**, 1291 (2001).
[10] J. W. Mintmire and C. T. White, Phys. Rev. Lett. **81**, 2506 (1998).
[11] Y. H. Kim and K. J. Chang, Phys. Rev. B **64**, 153404 (2001).
[12] *International Technology Roadmap for Semiconductors*, (SEMATECH, Austin, TX, 2001), available at http://public.itrs.net.
[13] S. Ramo, J. R. Whinnery, and T. V. Duzer, *Field and Waves in Communication Electronics* (Wiley, New York, 1994).
[14] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and Ph. Avouris, Appl. Phys. Lett. **80**, 3817 (2002).
[15] C. Auth and J. Plummer, IEEE Electron Device Lett. **18**, 74 (1997).
[16] D. Vesileska, D. K. Schroder, and D. K. Ferry, IEEE Trans. Electron Devices **44**, 584 (1997).
[17] K. Natori, J. Appl. Phys. **76**, 4879 (1994).
[18] J. Guo, M. Lundstrom, and S. Datta, Appl. Phys. Lett. **80**, 3192 (2002).

Metal–insulator–semiconductor electrostatics of carbon nanotubes

Jing Guo, Sebastien Goasguen, Mark Lundstrom, and Supriyo Datta

Citation: **81**, (2002); doi: 10.1063/1.1502188
View online: http://dx.doi.org/10.1063/1.1502188
View Table of Contents: http://aip.scitation.org/toc/apl/81/8
Published by the American Institute of Physics