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Theoretical investigation of surface roughness scattering in silicon nanowire transistors

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Using a full three-dimensional (3D), quantum transport simulator, we theoretically investigate the effects of surface roughness scattering (SRS) on the device characteristics of Si nanowire transistors (SNWTs). The microscopic structure of the Si/SiO₂ interface roughness is directly treated by using a 3D finite element technique. The results show that (1) SRS reduces the electron density of states in the channel, which increases the SNWT threshold voltage, and (2) the SRS in SNWTs becomes less effective when fewer propagating modes are occupied, which implies that SRS is less important in small-diameter SNWTs with few modes conducting than in planar metal-oxide-semiconductor field-effect-transistors with many transverse modes occupied. © 2005 American Institute of Physics.

The silicon nanowire transistor (SNWT) is attracting broad attention as a promising structure for future electronics.1,2 Therefore, understanding carrier transport in Si nanowires becomes increasingly important. Careful studies are needed to experimentally explore transport in SNWTs, but it is also clear that a theoretical understanding is similarly important. In this letter, we present a theoretical exploration of the Si/SiO₂ interface roughness scattering, or surface roughness scattering (SRS),3–5 in SNWTs.

It is well-known that scattering due to Si/SiO₂ interface roughness is important in planar silicon metal-oxide-semiconductor field-effect transistors (MOSFETs), and it is expected to be even more important in ultrathin-body silicon-on-insulator (UTBSOI) MOSFETs.3 For bulk MOSFETs, electrons are confined at the Si/SiO₂ interface by an electrostatic potential well. Under high gate bias, the potential well is thin, electrons are confined very near the interface, SRS increases, and the effective mobility decreases. For UTBSOI MOSFETs, the confining potential is determined by the film thickness, and SRS can be enhanced by the roughness at the two interfaces.3 In a SNWT, the channel is surrounded by the Si/SiO₂ interfaces, so one might expect SRS to dominate transport. We will show, however, that SRS may be less important in SNWTs than in planar devices because of the one-dimensional (1D) nature of the SNWT channel.

In Ref. 6, we developed a full three-dimensional (3D), quantum transport simulator of SNWTs based on the effective-mass approximation. In this work, to investigate the effects of SRS on small-diameter (~3 nm) SNWTs with physically rough Si/SiO₂ interfaces, we make use of this previously developed simulator. The simulated structure is a gate-all-around SNWT with a rectangular cross section and a [100] oriented channel (see Fig. 1). Following previous work on SRS,3–5 we assume an abrupt, randomly varying interface between the Si and SiO₂, parametrized by a root mean square (rms) amplitude and an autocovariance function.7,8 The statistical nature of the roughness will depend on the nanowire fabrication methods and may differ considerably from that arising during the high temperature oxidation of a planar Si surface. Nevertheless, since our objective is to discuss general insights into the physics of SRS in SNWTs, we will employ the roughness parameters for a planar (100) Si/SiO₂ interface obtained from Ref. 7. Our use of a continuum level description may be questioned, but we believe that it is a

[FIG. 1. (a) Schematic diagram of the simulated gate-all-round SNWT. The source/drain doping concentration is \(2 \times 10^{20} \text{cm}^{-3}\) and the channel is undoped. There is no source/drain overlap with the channel and the gate length is \(L=10 \text{nm}\). \(V_s\), \(V_d\), and \(V_g\) are the applied voltage biases on the source, drain, and gate, respectively; (b) cross section of the SNWT with a specific interface roughness pattern for the slice at \(X=9.0 \text{nm}\). For the device with smooth Si/SiO₂ interfaces, the Si body thickness is \(T_{Si}=3 \text{nm}\), the wire width is \(W_{Si}=3 \text{nm}\), and the oxide thickness is 1 nm; (c) confined wave functions for the slices at \(X=7.8 \text{nm}, X=8.0 \text{nm}, \) and \(X=8.2 \text{nm}\), respectively.]

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useful first step that gives insight into how the magnitude and spatial coherence of potential fluctuations influence carrier transport. In contrast to previous work, which made use of perturbation theory to compute the surface roughness scattering rate, we treat the physically rough structure directly.

The microscopic structure of the Si/SiO$_2$ interface roughness is implemented into the 3D simulator according to the following procedure. We first discretize the simulation domain with a 3D finite element mesh; each element is a triangular prism with a $2\ \text{Å}$ height and edge length, comparable to the size of roughness at the (100) Si/SiO$_2$ interface.

Next, we generate a two-dimensional (2D) random distribution across the whole Si/SiO$_2$ interface (unfolding the four interfacial planes into a sheet) according to an exponential autocovariance function:

$$C(x) = \Delta_m^2 e^{-x^2/L_m^2},$$ (1)

where $L_m$ is the correlation length, $\Delta_m$ is the rms fluctuation of the roughness, and $x$ is the distance between two sampling points at the interface. Based on the 2D random distribution, the types of the elements at the Si/SiO$_2$ interfaces may be changed from Si to SiO$_2$ or reversely, to mimic the rough interfaces [see Fig. 1(b)].

After the roughness is implemented, electron transport through the rough SNWT is simulated by using the nonequilibrium Green’s function approach. With a coupled mode space (CMS) representation, the wave function deformation due to the roughness is treated. (The simulation methodology has been described in detail in Refs. 6 and 10.) To emphasize the role of SRS on electron transport, we do not include any other scattering mechanisms, so coherent transport is assumed inside the device. (Oscillations in the current due to quantum interference might be expected, but the averaging over a thermal distribution of wavelengths that occurs is sufficient to suppress them.) The length of the channel (10 nm) is long enough to ensure that sufficient averaging takes place so that sample specific effects are not observed. The simulated results for the rough SNWT are then compared with those for a device with the same geometric parameters (e.g., nominal oxide thickness and Si body thickness) but smooth Si/SiO$_2$ interfaces. By doing this, the effects of SRS on SNWT device characteristics can be clearly identified.

Figure 2 plots the electron subband profile (left column) at the ON-state ($V_{GS}$=0.4 V) in the simulated SNWT with rough and smooth Si/SiO$_2$ interfaces. The corresponding transmission coefficients (right column) for both the rough and smooth SNWTs are also shown. Note that the modes are coupled in the simulation; we show them separately for illustrative purposes only. It is clearly seen in the energy versus $X$ plot that the presence of the roughness introduces significant fluctuations in the electron subbands, which lead to fluctuating elements in the diagonal terms of the device Hamiltonian [for details, see Eq. (7) in Ref. 6] and act as a scattering potential. At the same time, the shape of the confined wave function also varies from slice to slice along the wire in the rough SNWT [see Fig. 1(c) for an example], which produces deformation and coupling elements in both diagonal and off-diagonal terms of the device Hamiltonian [for details, see Eqs. (7), (8b), and (8c) in Ref. 6], and consequently lowers the transmission. (This effect has been named “wavefunction deformation scattering.”) To examine the significance of wave function deformation scattering, we plot an energy versus transmission curve (dotted-dashed) for the rough SNWT calculated by the uncoupled mode space (UMS) approach, in which only the variations in the electron subbands are included while the deformation and coupling terms are discarded. The fact that the UMS approach significantly overestimates the transmission for the rough device infers that wave function deformation scattering dominates the transport. This is an important finding because common perturbation theory treatments of SRS scattering typically treat the subband energy fluctuations but not the wave function deformation scattering.

From the energy versus transmission plot, we find that the difference between the transmission curve for the rough SNWT and that for the smooth device becomes more and more noticeable as energy increases. This occurs because as energy increases, more subbands (modes) become conductive and the coupling between different modes efficiently re-
rescribed earlier, enhances SRS in the SNWTs. Increasing gate overdrive. This occurs because more modes conduct. As a result, the effective height of the Coulomb blockade is reduced, enhancing SRS in the SNWTs. To do this, we compute a current ratio β vs gate overdrive. Figure 4 shows the β vs gate overdrive curves for the simulated SNWTs with different wire widths (WW) and roughness parameters (Lm and rms). At all the cases, the Si body thickness is fixed to be TSi=3 nm and the drain bias is VDS=0.4 V.

Fig. 4. Current ratio β vs gate overdrive curves for the simulated SNWTs with different wire widths (WW) and roughness parameters (Lm and rms). At all the cases, the Si body thickness is fixed to be TSi=3 nm and the drain bias is VDS=0.4 V.

vides the transmission in the rough SNWT. In other words, SRS becomes less serious when fewer propagating modes conduct, implying that SRS is more serious in a planar MOSFET than in a small-diameter SNWT. This effect is important in small-diameter nanowires as it is in conventional, planar MOSFETs.

In summary, we theoretically investigated SRS in SNWTs by using a full 3D, self-consistent, quantum mechanical simulator. The microscopic structure of the Si/SiO2 interface roughness was implemented into the simulator using the 3D finite element method. We found that (1) SRS reduces the electron density of states in the channel, which increases the SNWT threshold voltage, and (2) SRS in SNWTs becomes less serious when fewer propagating modes conduct, implying that SRS will be less important in small-diameter SNWTs than in planar MOSFETs with many transverse modes occupied. This work provides important insights into the nature of SRS in SNWTs and suggests that SRS may not be as important in small-diameter nanowires as it is in conventional, planar MOSFETs.

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