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Abstract: ***This paper describes a test method which relies on the actual observation of supply current*** *(I„)* ***waveforms. The method can be used to supplement the standard*** I_{DDQ} ***test method because it can be easily applied to dynamic logic circuits. The method allows us to detect faults which may not be detected by*** I_{DDQ} *methods,* ***and is sensitive enough to detect potential faults, which do not manifest themselves as functional errors. A simple built-in current sensor, which prove to be adequate in verifying the feasibility of using the*** I_{DD} ***waveforms analysis to try to detect faults in CMOS circuits, is proposed to safely observe the current waveforms without significantly changing the waveforms.***

I. Introduction

Testing of static CMOS circuits by observing the quiescent power supply current (I_{DDQ}) has been a very popular technique for detecting a large number of physical defects. CMOS ICs showing abnormal quiescent power supply current (I„) may contain defects. However, the recent trend in low power design by scaling down the power supply voltage (V_{DD}) and decreasing the threshold voltage (V_T), has caused an increase in the I_{DDQ} current, which reduces the effectiveness of I_{DDQ} testing. Another shortcoming of I_{DDQ} testing is that it cannot be applied to dynamic logic circuits. Hence, to help overcome these shortcomings, we propose a novel test method which relies on the actual observation of the supply current (I„) waveforms. The method can be used to supplement the I_{DDQ} testing method in trying to detect defects in CMOS circuits.

Defects which cause electrical shorts and opens that cause floating CMOS inputs are detectable by observing the quiescent current I_{DDQ}. Our objective is not to target such faults which can be detected by I_{DDQ} testing, but to be able to detect weak opens (high resistance shorts), or individual weak transistors. In fact, such faults may not even show any logic functionality error in the circuit, but can cause delay faults, and can affect reliability issues with marginal circuit performance at certain process corners. Such defects show up as a change in the waveforms of the supply current.

The rest of the paper is organized as follows. In section II, we describe a method to analyze the waveforms of the supply current. In section III, we verify that the defects which we try to detect indeed cause errors in the waveforms for static CMOS, and pre-charged domino circuits. A built-in current sensor which shows the feasibility of actually observing the IDD waveforms is evaluated in section IV. In section V, a complete 8-bit adder circuit is used to verify that the method is applicable to a group of gates. We summarize with a list of key results and directions for future work in section VI.

II. Supply Current (I_{DD}) Waveforms Analysis Method

First, we temporarily neglect the issue of whether it is physically possible to accurately observe the supply current waveforms, without significantly altering the waveforms. We assume that there is a current sensor which is able to safely observe the waveforms. In section IV, we consider the design of a current sensor to accurately observe the supply current waveform. With the above assumption, we can represent our CMOS circuit as the system shown in figure 1. v(t) is the input voltage waveform from the previous stage, h(t) is the transfer function of the CMOS circuit, and i(t) is the supply current.

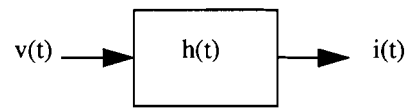


FIGURE 1. Model of a CMOS circuit

There are two factors which can alter the supply current waveform i(t):

- A change in the input voltage waveform v(t). This change can happen because of a fault in the previous stage.
- A change in the transfer function of the CMOS circuit h(t). If the entire stage becomes stronger or weaker, h(t) is proportionally scaled by a constant factor.

The current I_{DS} which flows through the drain and source of a group of serially connected, saturated mode PMOS

transistors is proportional to

$$K_P(V_{DD} - V_T)^2$$

where K_P is the process transconductance parameter of the transistor, V_{DD} and V_T are the power supply voltage and the threshold voltage, respectively. Hence, we can approximately model the charging or discharging of the output capacitances by a stack of PMOS transistors as

$$C\frac{dV}{dt} = I_{DS} = \alpha K'(V_{DD} - V_T)^2$$

where C is the capacitance being charged or discharged, a is the proportionality constant, K' the equivalent K_P of the transistor stack, V_{DD} and V_T are the supply voltage and the threshold voltage of the MOS dlevices, respectively. A weak transistor only changes K' in the above model. Although simple analysis indicates that the waveform does not change, actual simulations show that the waveform does get modified. The actual defects, which are more likely to be shorts or opens, have V/I characteristics that are linear (resistive) or exponential (diode). Hence, the supply current i(t) equation is very different. We model the weak opens as being ohmic.

To compare a faulty circuit with a good circuit, we analyze the Fourier components of the supply current. The relative magnitudes of the Fourier components correspond to the relative supply current waveforms. The relative magnitudes of the Fourier components are expressed as

$$F_r = \frac{F_i - F_1}{F_1}$$

where F_r, F_1, F_i are the normalized Fourier component, the fundamental component, and the i^{th} component, respectively.

The frequency components of the output current i(f), which is equal to h(f)*v(f), are then measured. In actual operation, any error in v(f) or h(f) will cause a change in i(f). The advantage of using the normalized Fourier components in the analysis is to make the method tolerant to process and temperature variations, since the normalized Fourier components depend only on the supply current waveforms.

III. I_{DD} Waveforms Analysis for FCMOS and Pre-charged Domino Circuits

We verify that the I, waveforms analysis does indeed work for CMOS circuits. For the purpose of verification, the HSPICE simulations for circuits were carried out using a $0.6\mu m$, HP CMOS process. Figure 2 shows the simulation model.

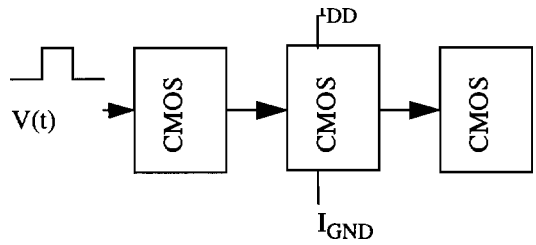


FIGURE 2. SPICE model

In our SPICE model, we observe the supply and ground currents of a single isolated gate. Furthermore, in order to provide realistic operating conditions for the gate, we drive the input of the isolated gate with an identical gate and load the output with a similar gate. The loading effects by other gates on the power and ground lines are also included before we simulate the circuit.

a. Fully Complementary CMOS (FCMOS) Circuits

An inverter and a two input NAND gate are used to verify the I, waveform analysis for FCMOS circuits. The circuit used in the simulation is shown in figure 3.

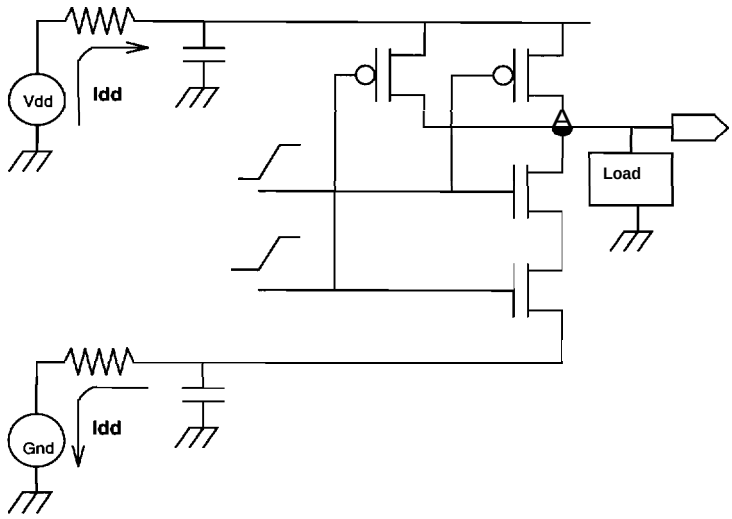
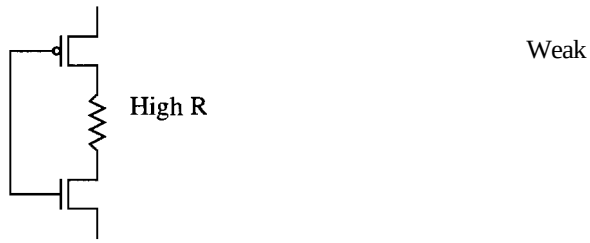


FIGURE 3. SPICE Model for FCMOS Circuits

In order to detect the weak opens (high resistance shorts) and the weak transistors faults., the following fault effects are simulated for the inverters and NAND gates:

- High resistance shorts, modeled by adding a resistance from the drain of a MOSFET
- Weak MOSFETS, modeled by decreasing the width of a MOSFET.



We then simulate the circuit and obtain the input-output waveforms, the supply current I, and the ground current I, waveforms with their corresponding Fourier components for both the inverter and NAND gates. Figures 4 and 5 show the waveforms obtained from the inverter, and figures 6 through 9 show the various waveforms obtained from the NAND gates.

For the inverter, the waveforms obtained from the simulations with the weak transistor fault:; are shown in figure 4, and the waveforms from the simulations with the resistive shorts are shown in figure 5. In figure 4, the input-output waveforms are shown in the bottom left corner, and the supply current I_{DD} and the ground current I_{GND} waveforms are shown in the top left comer. The top right comer of figure 4 shows the normalized Fourier components of the supply current I, and the bottom right corner shows the Fourier components of the ground current I, The family of waveforms in figure 4 are obtained by changing the width of the PMOS device of the inverter with a ratio of 0.5, 1.0 and 2.0. The figure shows that by observing the first three of the Fourier components, it is possible to differentiate each case of the circuits.

In figure 5, the input-output waveforms are shown in the top half and the normalized Fourier components for the supply current I, are shown in the bottom half. The resistive shorts are simulated by adding a resistance at the drains of the transistors. The range of the resistance values used is from $10k\Omega$ to $100k\Omega$. The modeled resistor values have been selected such that the correct functionality of the inverter is maintained. This implies that the fault is not easily detected by conventional testing method, such as I_{DDQ}. The normalized Fourier components are markedly different from the one in figure 4. It is slightly easier to detect the resistive shorts compared to the weak transistor faults.

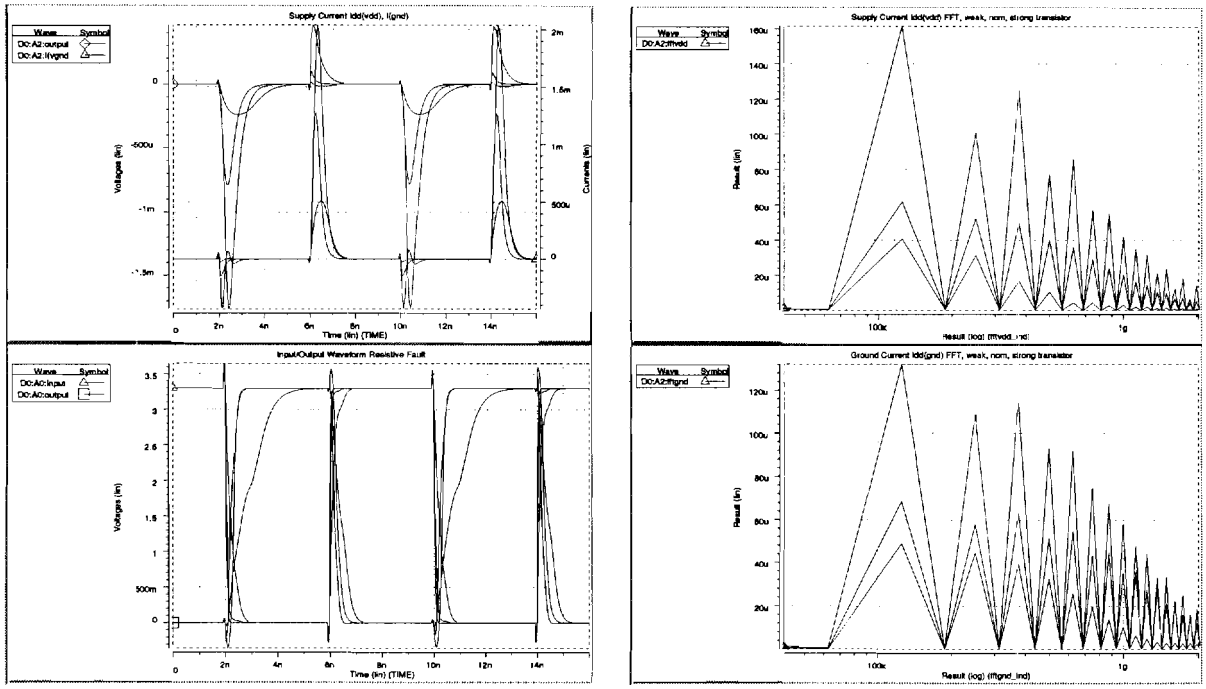


FIGURE 4. Simulations for weak transistor faults in an inverter.

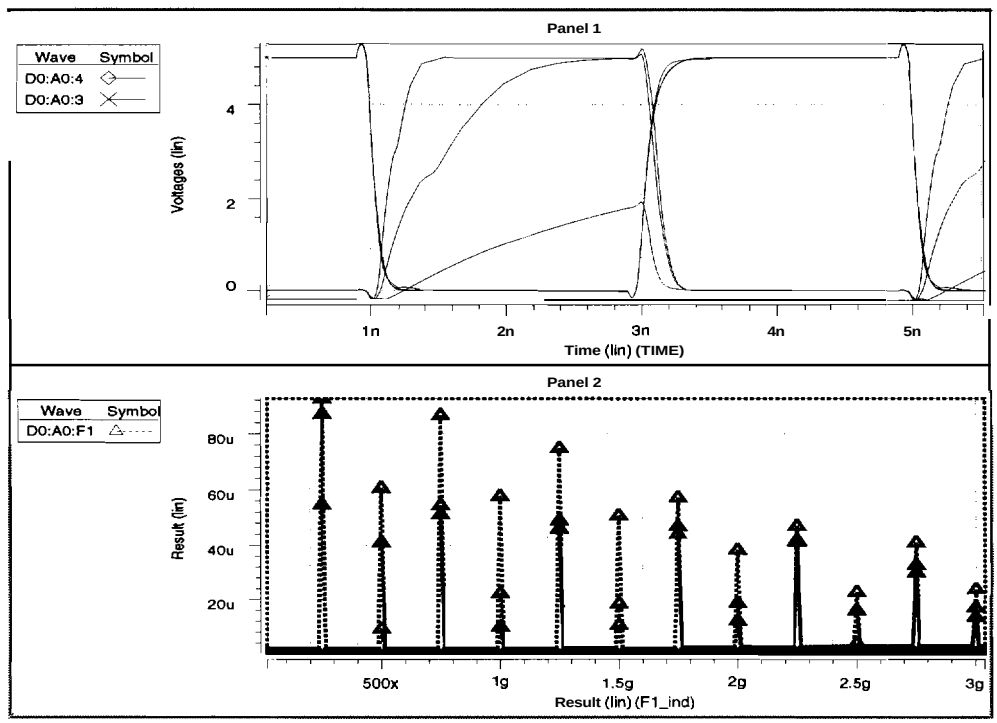


FIGURE 5. Simulations for a resistive short at the drain of the PMOS of an inverter gate

For NAND gates, the waveforms obtained from the simulations with the weak transistor faults are shown in figure 6 and 7, and the waveforms obtained from the simulations with the resistive shorts are shown in figure 8 and 9. In figure 6, the supply current I_{DD} and the ground current I_{GND} waveforms are shown in the top half, and the input-output waveforms are shown in the bottom half. The normalized Fourier components of the supply current I_{DD} are shown in the top half of figure 7, and the bottom half shows the Fourier components of the ground current I_{GND} waveforms. Again, the first three components of the Fourier components are sufficient to differentiate between the good circuit and the circuit with the weak transistor faults.

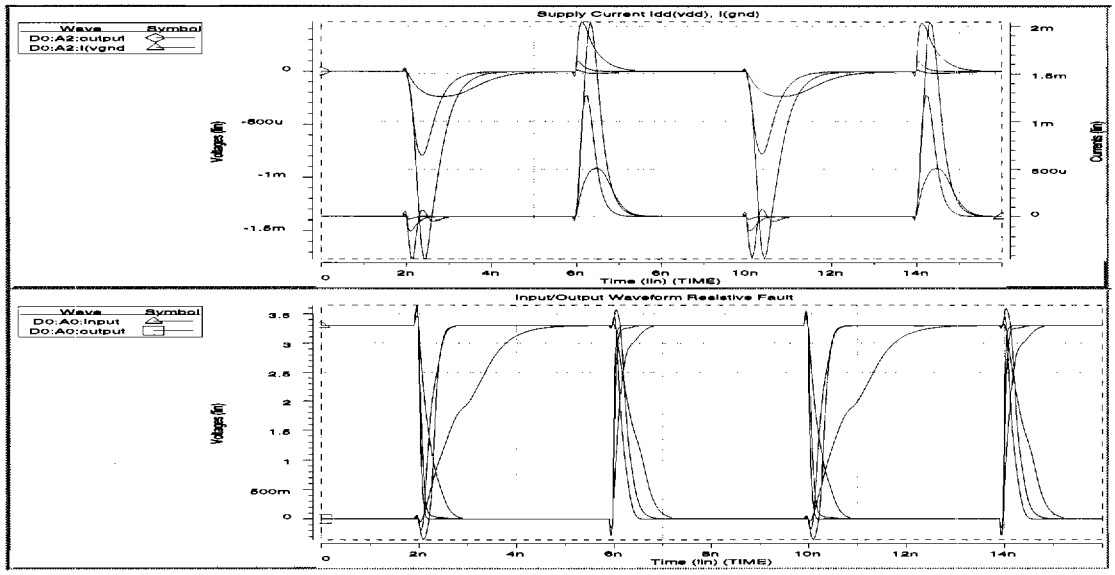


FIGURE 6. Supply current, ground current and input-output waveforms for a NAND gate

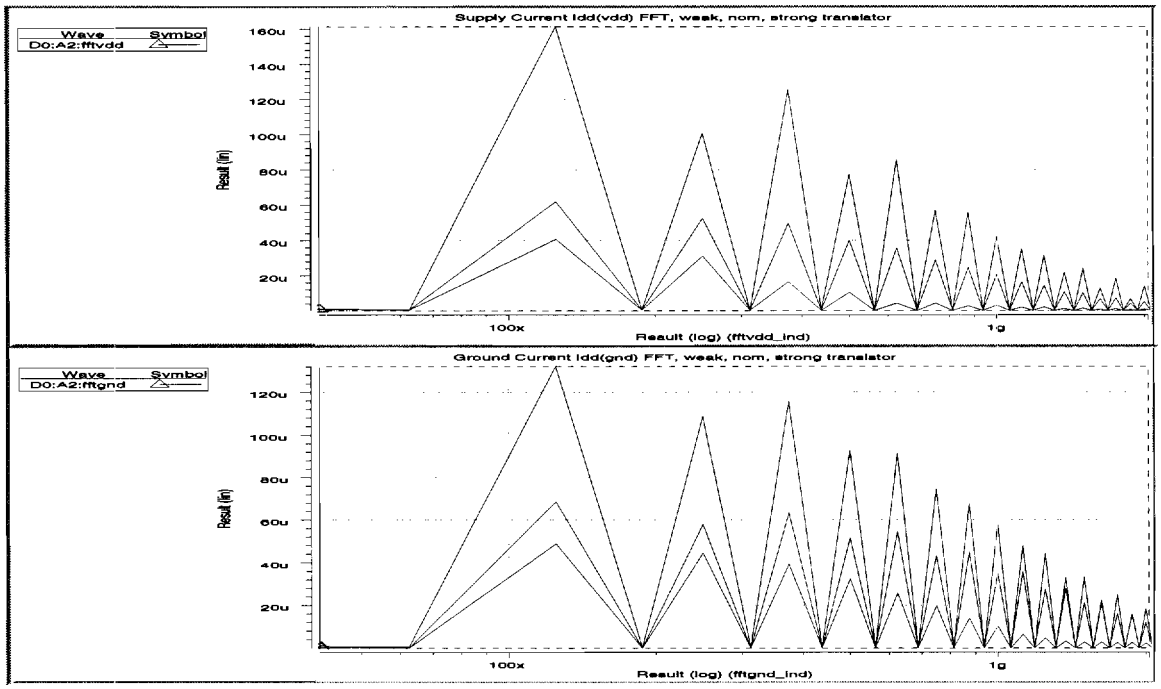


FIGURE 7. Normalized Fourier transform of the supply and ground currents

The input-output waveforms obtained from simulating the NAND gates in the presence of resistive shorts are shown in the middle third of figure 8. The supply current I_{DD} and the ground current I_{GND} waveforms are shown in the top third and bottom third of figure 8, respectively. The normalized Fourier components for the supply current I_{DD} and the ground current I_{GND} waveforms are shown in the top half and bottom half of figure 9 respectively. Figure 9 also shows the effect of different loading on the Fourier components, and the effect of a fault in one gate in the presence of 100 similar gates. The number of gates which load the power supply is referred to as the partition size and will be described further in section IV. Presently, it is sufficient to note that the Fourier components show insignificant variations with increasing partition sizes, while the magnitude of the current waveforms in figure 8 shows large variations.

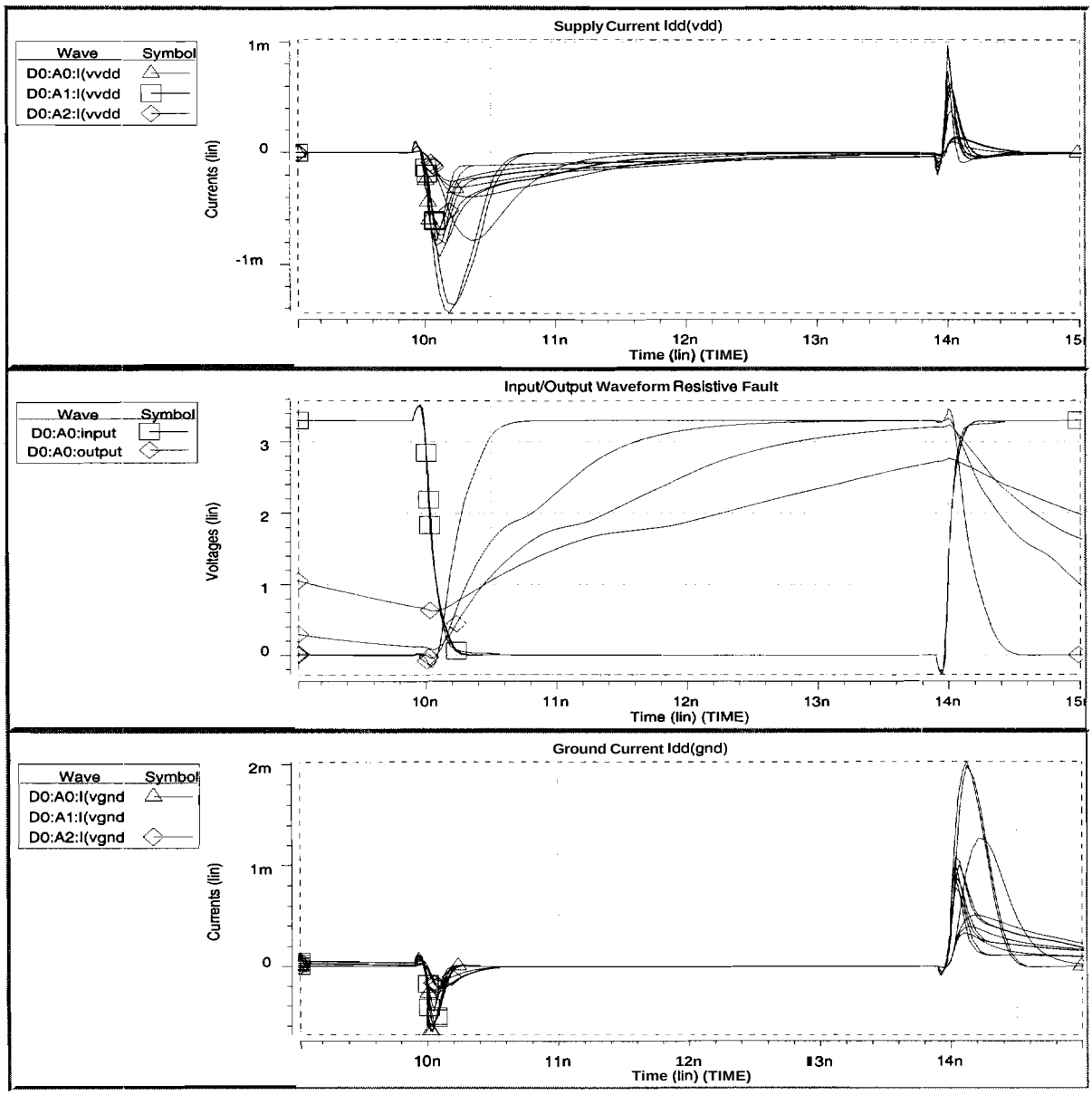


FIGURE 8. Supply current, ground current, input-output waveforms for a NAND gate resistive shorts

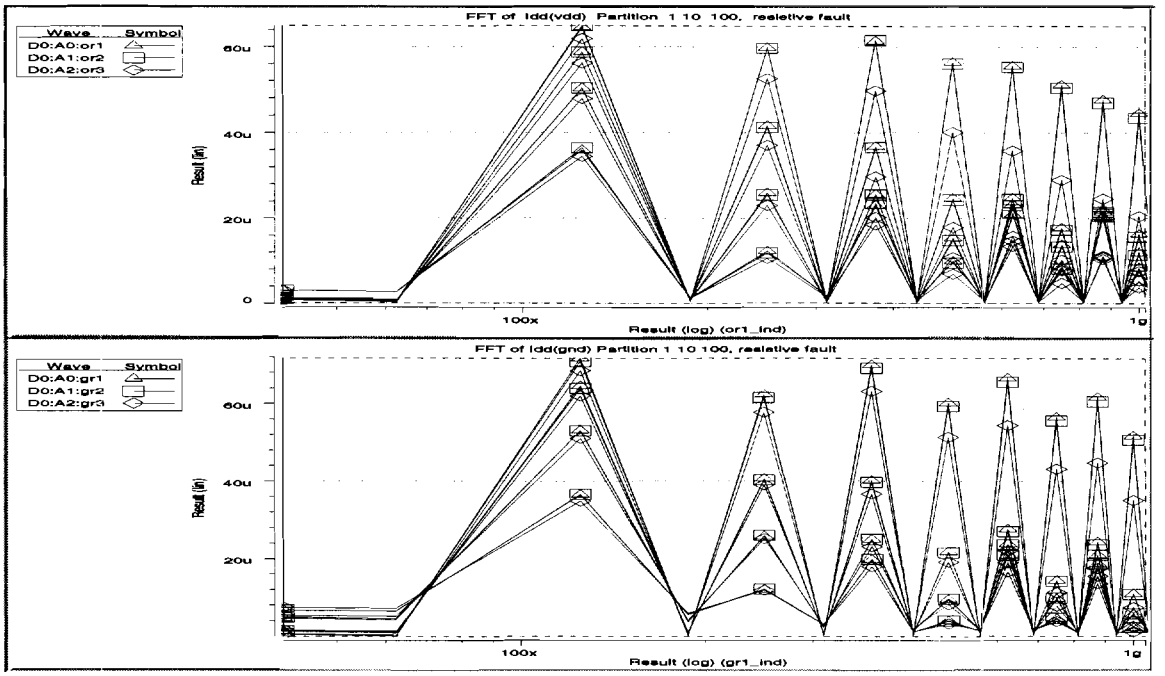


FIGURE 9. Fourier components of current and ground currents for a NAND gate with resistive shorts

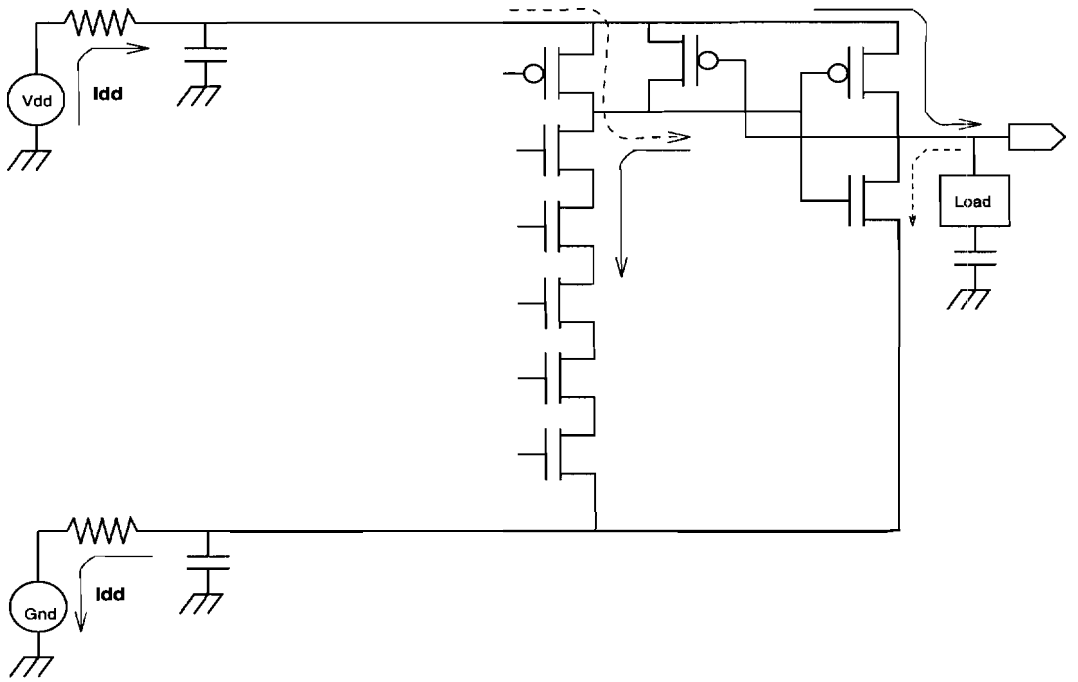


FIGURE 10. Simulation setup to obtain I_{DD} waveforms for domino logic

b. Pre-charged Domino Logic Circuits

A 4-input NAND gate, coupled with a static inverter, are used to verify the I_{DD} waveforms analysis for pre-charged domino logic circuits. The circuit used in the simulations is shown in Figure 10 . The following defects are simulated for the 4-input pre-charged domino logic NAND gates: weak transistors and high resistive shorts. During the pre-charge phase, by observing the power supply current (I_{DD}) and the ground current (I_{GND}), we can detect the weak transistor fault in the PMOS of the NAND gate and the NMOS of the static CMOS inverter simultaneously (illustrated by the dashed arrow in figure 10). During the evaluation phase, by observing the power supply current (I_{DD}) and the ground current (I_{GND}), the faults in the NMOS stack in the Pull Down Network of the NAND gate and the fault in the PMOS of the static CMOS inverter can be detected simultaneously (illustrated by the solid arrow in figure 10).

Figure 11 through 14 show various waveforms obtained from simulating the pre-charged domino logic circuits in the presence of weak transistor faults and high resistive shorts. Figure 11 and 12 show the waveforms corresponding to the presence of weak transistor faults, and figure 13 and 14 show the waveforms corresponding to the presence of resistive shorts. The effect of weak transistor faults is modeled by changing the width of the NMOS device in the Pull Down Network stack of the NAND gate.

The top and second quarters of figure 11 show the power supply current, I_{DD} and the ground current, I_{GND}, for good circuit and circuit with weak transistor faults, respectively. The third and last quarters of figure 11 show the input-output waveforms for good circuit and circuit with weak transistor faults, respectively.

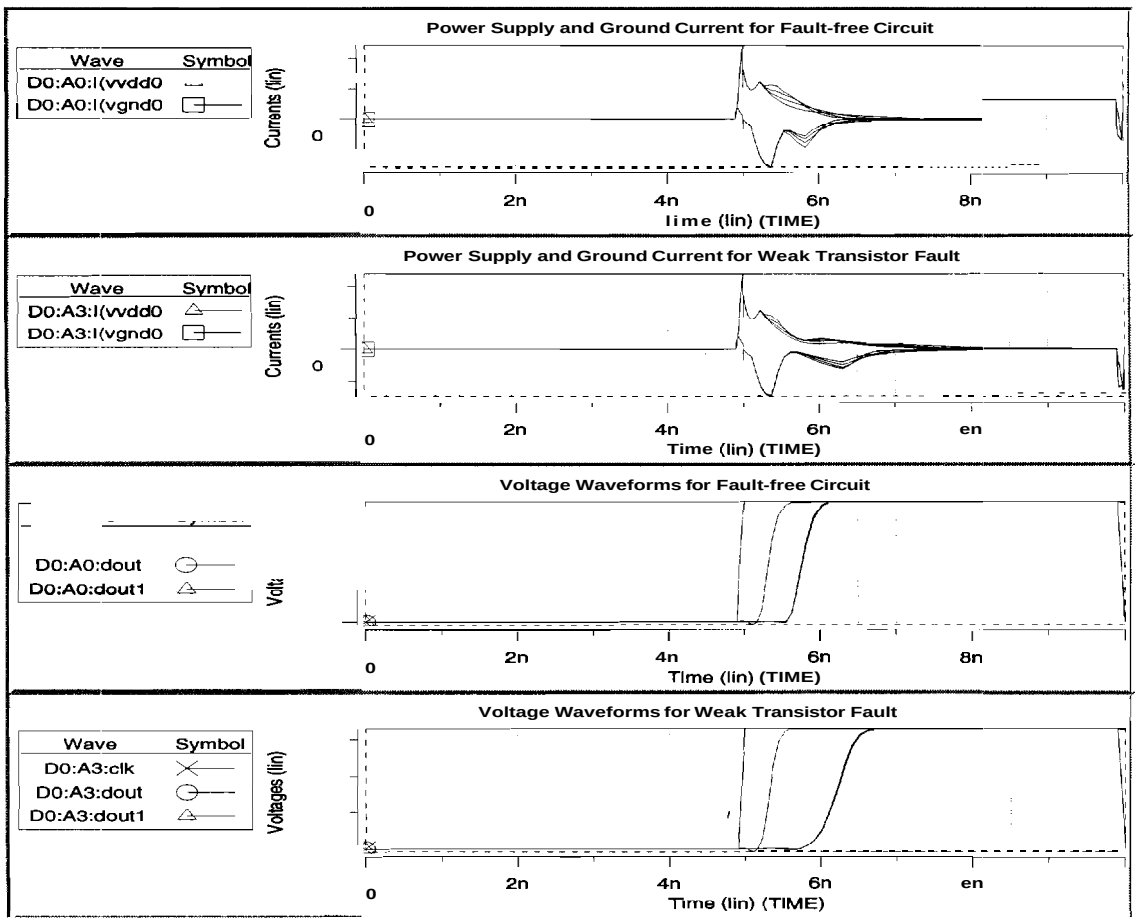


FIGURE 11. I_{DD}, I_{GND}, and input-output waveforms for domino NAND with weak transistor faults

The normalized Fourier components of the I_{DD} waveforms for good circuit and circuit with weak transistor faults are shown in the top and second quarter of figure 12, respectively. The third and last quarter of figure 12 show the Fourier components of the I, waveforms for good circuit and circuit with weak transistor faults respectively. By observing the first three components, we can again differentiate between a good and a faulty circuit.

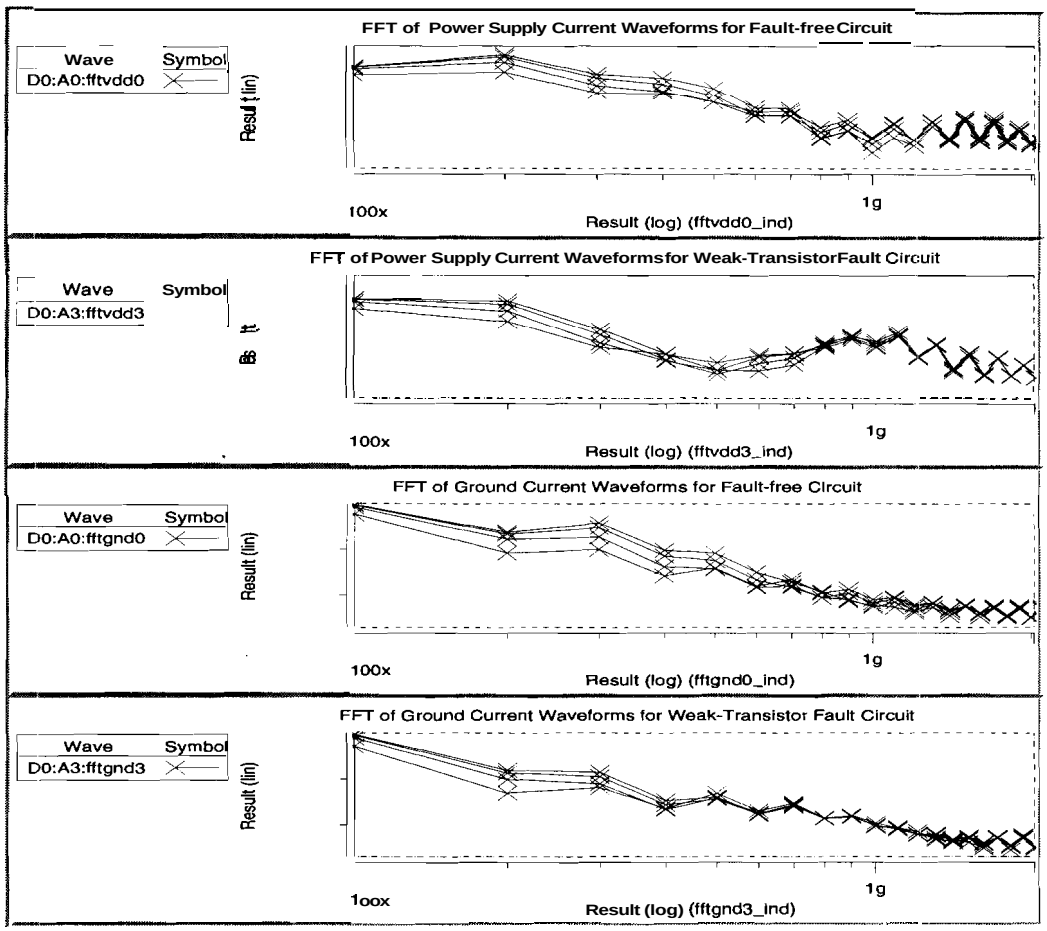


FIGURE 12. Fourier components for weak transistor faults in domino logic NAND gate

Figure 13 and 14 show the waveforms obtained by simulating the pre-charged domino logic: NAND gates in the presence of high resistive shorts. The I, and I_{GND} waveforms for good circuit and circuit with resistive shorts are shown in the top and second quarter of figure 13, respectively. The third and last quarter of figure 13 show the input-output waveforms for good circuit and circuit with resistive shorts respectively.

The top and second quarter of figure 14 show the normalized Fourier components of the I, waveforms for good circuit and circuit with resistive shorts, respectively. The Fourier components of the I_{GND} waveforms for good circuit and circuit with resistive shorts are shown in the third and last quarter of figure 14, respectively. Again, by comparing the first two or three harmonics of the Fourier components, we are able to differentiate between a good circuit and a circuit with resistive shorts.

The simulation results obtained for pre-charged domino logic gates show the feasibility of using the method of I, waveforms analysis to detect faults. The standard I_{DDQ} testing method cannot be easily applied to dynamic logic circuits. Hence, the I, waveforms analysis method can complement the I_{DDQ} testing to help detect faults in dynamic logic circuits.

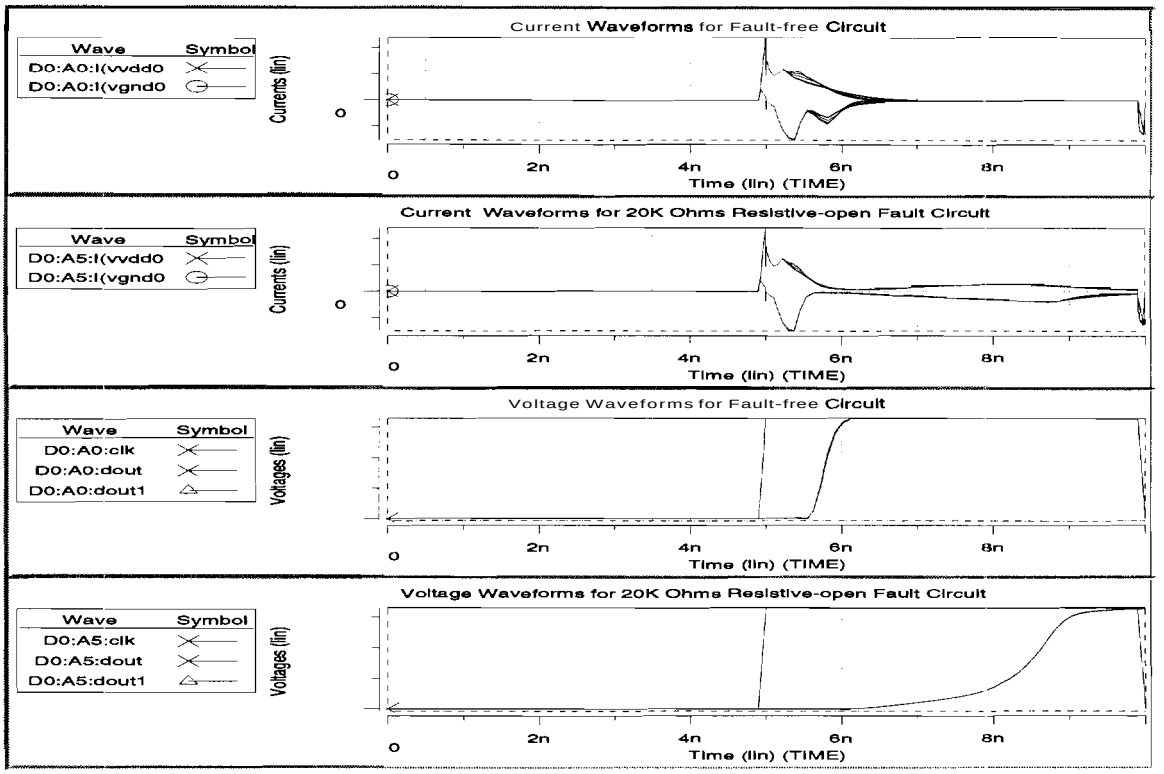


FIGURE 13. I, I, and input-output waveforms for a domino NAND gate with a resistive shorts

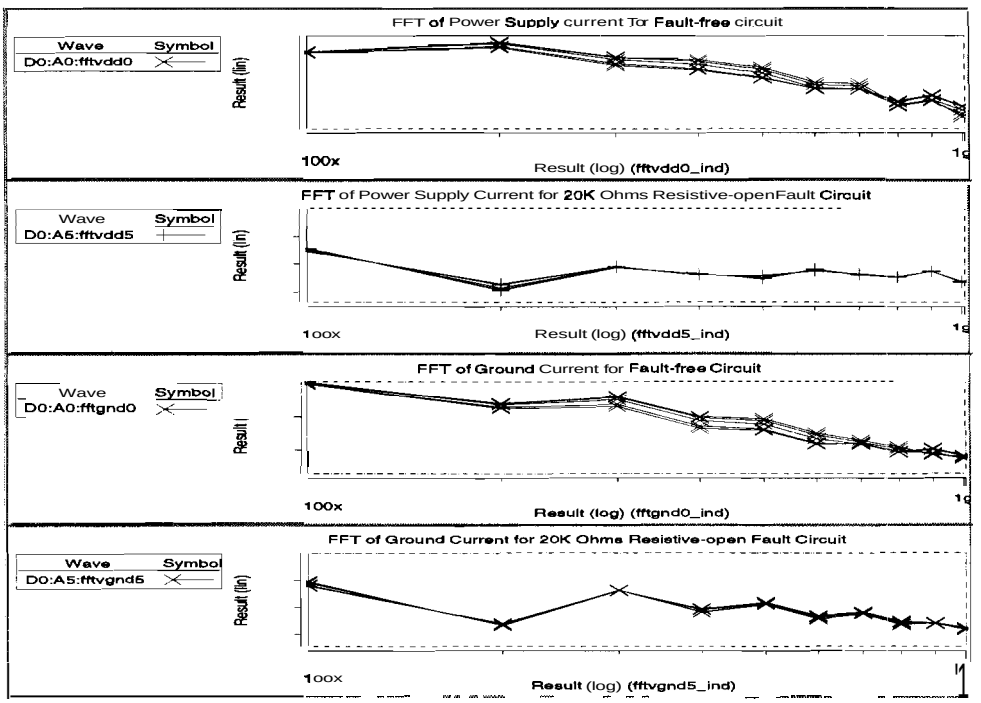


FIGURE 14. Fourier components of I_{DD} and I_{GND} waveforms for domino NAND with resistive shorts

IV. Current Sensor

In order to carry out the I_{DD} waveforms analysis, a good method to safely measure the current waveforms is needed. We need an accurate current sensor which can faithfully observe the current waveforms without significantly changing the waveform. We have designed a simple current sensor which proves to be adequate in fulfilling our need in verifying the feasibility of using the I_{DD} waveforms analysis to try to detect faults in CMOS circuits. The schematic of the current sensor is shown in figure 15. The circuit is a simple amplifier which senses the voltage difference at the source terminals of the PMOS transistors. The NMOS current mirror provides the load for the PMOS transistors. The reference voltage at the input gates of the PMOS transistors is set to a value such that all the transistors are in saturation mode.

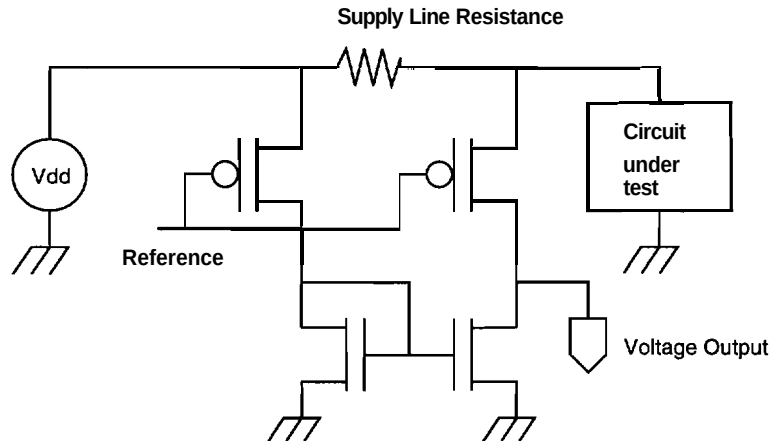


FIGURE 15. Current sensor

The applicability of the current sensor is put to a test by using it to measure the I_{DD} waveforms in our simulations. The circuit under test is modeled by 100 serially connected static CMOS inverters. The output waveforms obtained from the simulations and the resistive voltage drop across the source terminals of the PMOS transistors are shown in the top left and bottom left of figure 16, respectively. Certain amount of distortions in the waveforms are due to the lack of bandwidth in the current sensor. The right half of figure 16 shows the Fourier components of the supply current waveforms.

In typical CMOS circuits, the supply line capacitance is high, and this capacitance smooths out the current waveforms. As a single current sensor is being used for a large number of gates, the current waveforms are slow enough that they can be adequately measured by the current sensor circuit.

We define the partition of the circuit to be a collection of gates with a current sensor. The supply current of all gates is measured simultaneously with a single current sensor. Partitions sizes in the range of 2 to 128 are simulated. Increasing the partition size causes a smoothing effect to the current waveforms, and also slows down the current waveforms which makes it easier for the current sensor to accurately duplicate the current waveforms.

However, increasing the partition size makes it more difficult to observe the changes in the output waveforms. This is because the power supply line can be modeled as a low pass filter whose cutoff frequency is inversely related to the partition size. Hence, a loss of high frequency components occurs. From the simulation results for domino logic and FCMOS gates, we observe that a partition size of 64 identical gates can be safely used.

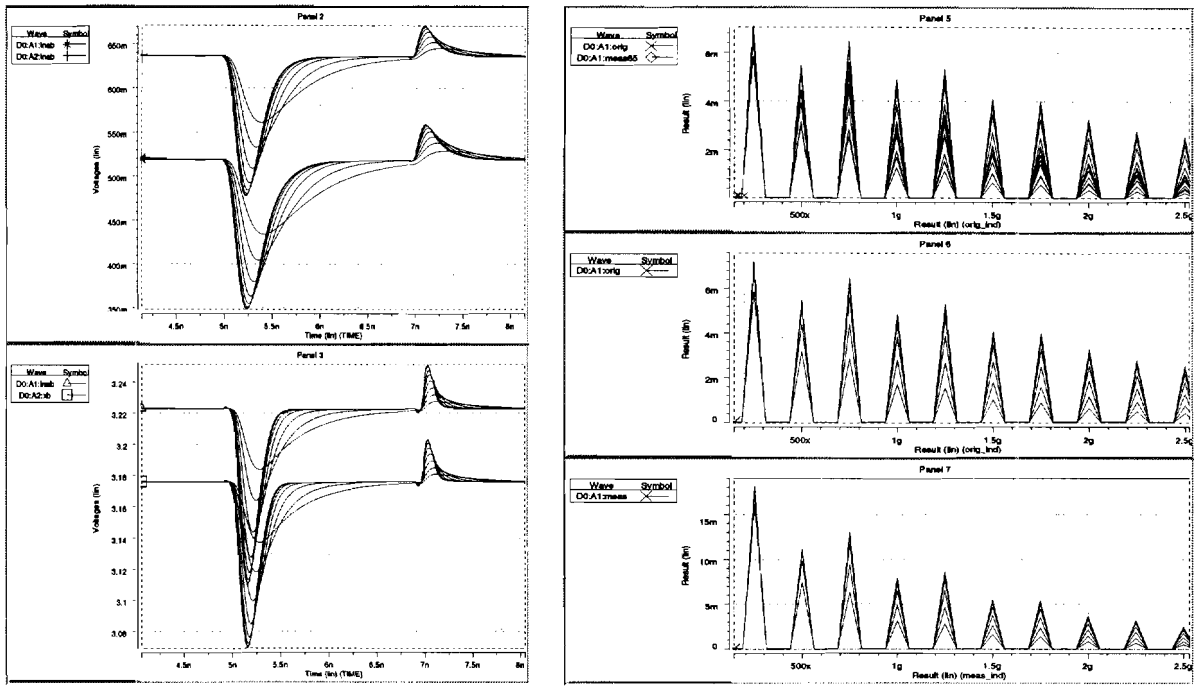


FIGURE 16. Resistive voltage drop, output waveforms and Fourier components of I_{DD} waveforms

V. 8-bit Adder

While the above results verify that the I_{DD} waveform analysis is capable of detecting defects; which are undetectable by standard I_{DDQ} techniques, we need to verify further that the method is practically tenablle for a large enough circuit. To verify this, we do HSPICE simulations on a FCMOS 8-bit carry propagate adder.

The adder consists of standard 26-transistors FCMOS full-adders. The layout of the whole: structure is done in HP CMOS $0.6\mu m$ process. The interconnect capacitances are fully extracted for simulation purposes. We introduce a 40R resistance in the power supply lead. Actual simulations show that the worst case supply noise is under 20mV. In practice, the 40R resistance can be achieved by using a small strap of polysilicon. The current sensor described in the previous section is used to sense the voltage across the 40R resistor.

We set the input test vectors such that the entire carry chain toggles by changing the input carry. We also ensure that all the sum outputs toggle. Using these inputs, we attempt to detect an error in the second bit position. Figure 17 shows the carry waveforms in the presence of a fault. The top half of figure 17 shows the even carry bits (bit positions 0,2,4,6), and the bottom half shows the odd carry bits (bit positions 1,3,5,7). Resistive shorts with resistances of $5k\Omega$, $10k\Omega$, and $20k\Omega$ are simulated. We observe that although the fault causes the delay of the second stage to increase, the functionality of the adder remains unchanged.

Figure 18 shows the current waveforms with various values of the resistive short. The top left half of figure 18 shows the voltage drop across a 40R resistor, which is around 20mV. The amplified output of the current sensor, shown at the bottom left half, is around 360mV. It clearly shows that although the current sensor does not faithfully follow the actual waveform, it does mimic the low frequency components well. The graphs on the right are the Fourier components of the corresponding waveforms plotted on a log scale. The bold line corresponds to the good circuit. We use the Fourier components over a large frequency range to highlight the lack of bandwidth. The clear difference in the Fourier components for the first three components makes it easy to detect faults in the circuit. The fact that the

zero order component is identical in all the cases implies that the fault is undetectable by the :standard I_{DDQ} testing methods.

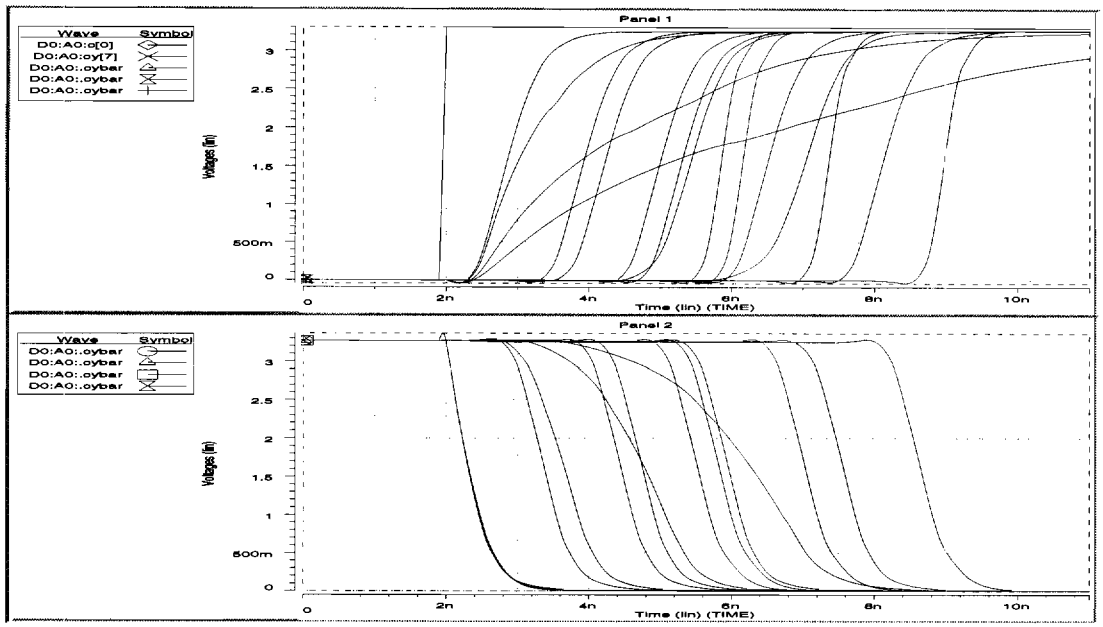


FIGURE 17. Carry waveforms for an 8 bit adder in the presence of a resistive short in the second bit position

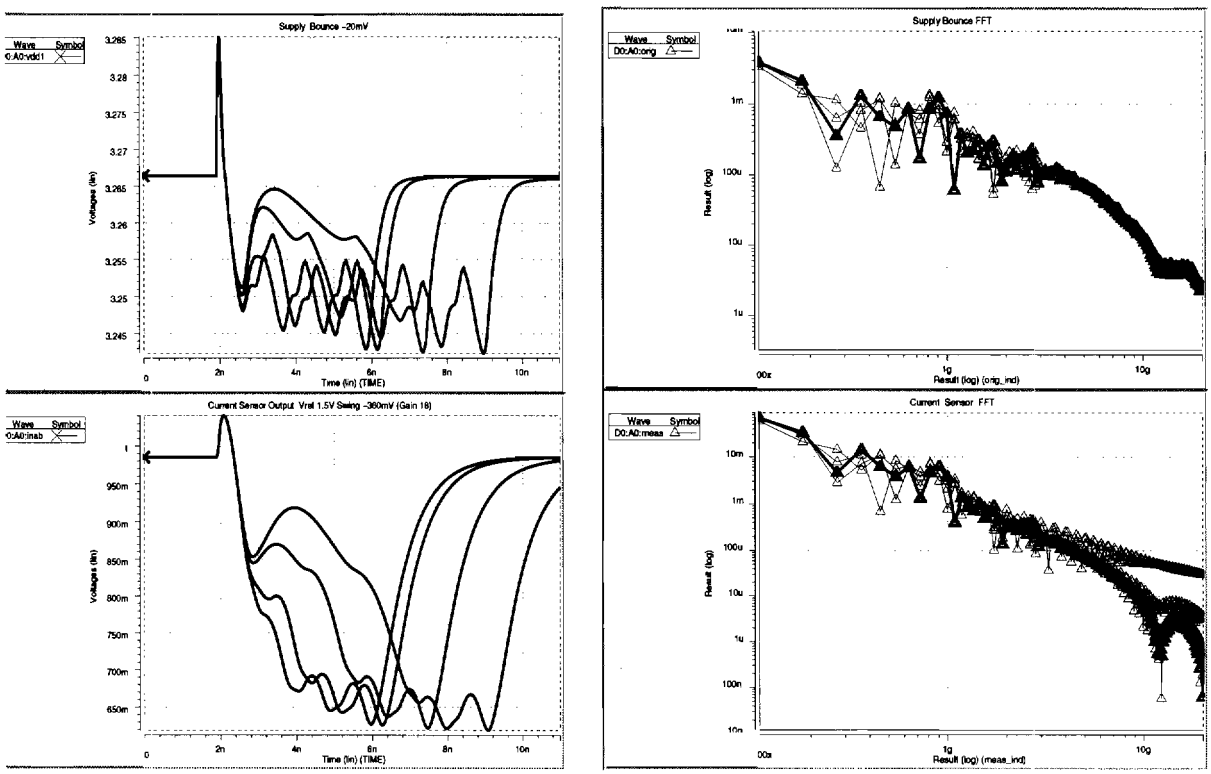


FIGURE 18. Current waveforms and Fourier components for an 8 bit adder

To diagnose that the fault is in the second bit position, it is sufficient to have the Fourier components from the faulty circuit to be pre-computed for various faults. These will be used as a reference for comparison to narrow down the fault location. However, this process can be time consuming. Alternatively, we can use a set of input test vectors which will toggle only a few nodes, by which we can narrow down the search area for the fault location. A fault in the NMOS stack shows up as an error in the I_{GND} waveform, while a fault in the PMOS stack shows up as an error in the $I_{}$ waveform. In the above simulations, the fault is in the PMOS stack.

The fact that we can detect the fault in spite of all the outputs switching shows us that $I_{}$ waveform analysis is quite a sensitive method. In fact, it may be possible that it detects faults which do not alter the proper operation of the circuit. However, it allows us to find marginal operation defects in both static and dynamic logic families.

VI. Summary and Directions for Future Work

I_{DDO} testing is a widely used technique to detect faulty CMOS circuits because of its effectiveness in detecting shorts and certain opens. However, I_{DDQ} testing has its limitations when it is applied to large circuits with small feature sized devices where the leakage component is high, and when it is used to detect defects such as high resistive shorts and weak transistors, which do not alter the quiescent current. I_{DD} waveform analysis addresses all these issues by the following techniques:

- Partition the circuit into smaller blocks and use built-in current sensors to measure the current of these blocks.
- Measure the waveforms generated by the $I_{}$ currents rather than the average current. We explicitly look at the first, second and third harmonics of the current waveforms and discard the zero order component. Hence, constant DC components like leakage currents do not affect this technique.
- Most defects, which cause a change in the pull down or pull up strength of NMOS or PMOS stacks, cause a change in the $I_{}$ waveform and can thus be detected. Furthermore, as we have shown, the $I_{}$ waveform analysis method is sensitive enough to detect small resistance shorts.
- $I_{}$ waveform analysis also acts as a fault diagnosis tool because of the capability of simultaneously monitoring a number of output nodes.

While this paper shows the viability of IDD waveform analysis, it is lacking in methods and algorithms for applying test vectors to locate faults. However, this should be a simple problem to solve since any method which can cause transitions to propagate from input to output while simultaneously prevent the gates at the same level from switching should suffice.

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