

Open Cortex-M0™ Modular Debug Unit

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The debug unit of a modern digital system on chip (SoC) is a critical unit that allows users to monitor and analyze the chip's activity that occurs throughout a SoC design. Selection of the debug unit's correct feature set and architecture are critical to the success of the design. Debugging systems that exist have different architectures and are closely coupled to their host SoCs. As a consequence they are resource intensive to improve on due to the different nature of each SoC designs. Moreover, the bus protocols that allow the debug unit to interact with the SoC design are often designed towards the SoC design itself and are not easily extensible. This project serves to analyze existing debug units in the public domain and classify their feature sets, architectures, speed and size vs. the developed modular debug unit. Hardware description languages now enable new forms of modular designs which allow the possibility of building a modular debugging core. This allows for integration with arbitrary on chip bus systems and actual CPU processor cores. A hierarchical finite state machine (HFSM) design approach also enables the debug unit to be extended with debugging features. The size and speed of synthesized designs targeting field programmable gate array (FPGA) technology are compared, and preliminary results show that the a modular design approach debug unit is able to significantly reduce development time and be extended with new features. Future work will be carried out to build on preliminary results obtained from a modular debug unit.