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Enhancement-mode quantum transistors for single electron spin

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Abstract

Using an InAs/GaSb composite quantum well, we demonstrate an enhancement mode single electron transistor. With a Hall bar geometry, we show that the device undergoes a transition from accumulation of two-dimensional (2D) holes in GaSb to a complete depletion and finally to an inversion layer of 2D electrons in InAs. When the top-gate area is reduced to nanometer scale, the inversion electrons are confined to a quantum dot, and the transistor displays single electron characteristics: a series of conductance peaks resulting from electrons tunnelling through the quantum dot. The occurrence of the first peak is the signature of one electron occupying InAs quantum dot. The unique configuration of enhancement quantum dots makes it possible to upscale to 2D arrays for manipulation and transporting of single spins.

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Keywords: Single electron transistor; Quantum computation; Resonant tunnelling

Single electron spin not only is of interest for studying quantum physics, but also has potential applications in quantum computing [1]. However, it is technically challenging to create a single electron in a semiconductor quantum dot (QD), because electrons must be confined to a nanometer-size QD so that their level spacing could be larger than thermal energy. To date, there have been only a few successful experimental demonstrations. In lateral $Al_xGa_{1-x}As/GaAs$ single electron transistors (SETs), applying negative bias to the plunger gate results in raising tunnelling barriers, thereby preventing a definitive observation of a totally depleted QD. To overcome this problem, a specific geometry has been engineered [3] to keep the plunger gates as far away from the tunnelling barriers as possible. To verify the presence of just one electron, novel spectroscopic techniques, such as those utilizing quantum point contact with conductance sensitive to one electron charge, have recently been developed [2]. In contrast, in vertical SETs [4] with resonant tunnelling structures, voltage change in the Schottky does not alter tunnelling rate, because the thickness and height of the tunnelling barriers in heterojunctions are fixed.

For quantum computing, each single electron confined in QD can serve as a qubit, and lateral array of qubits conceptually provides the possibility of scaling the system up. The QD spins need to be initialized, manipulated, entangled, transported [5], and finally measured. Two spins can be coupled via exchange interaction and form a CNOT (controlled-NOT) quantum gate. The strength of the exchange interaction between two spins and the overlap of wavefunctions, is controlled by gating.

In this paper, we propose and demonstrate a new approach for fabrication of QD qubits. The major component of our enhancement quantum transistors is a composite quantum well [6] (CQW), which consists of a 4 nm InAs and a 20 nm GaSb QW. A unique feature of our enhancement-mode single electron transistor is its use of a single top-gate to create two symmetric tunnelling barriers and, simultaneously, an empty QD. Further

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increase of the gate voltage produces a steep confinement and allows electrons to tunnel into the dot, one at a time.

Fig. 1(a) shows the schematic energy band diagram along the crystal growth direction, where the CQW is sandwiched by $Al_xGa_{1-x}Sb$ barriers. Effectively, the CQW is a narrow band gap semiconductor, with the band gap tuned by the thickness of InAs. The as-grown sample is p-type, i.e., the GaSb QW is populated with 2D holes, while the InAs QW is empty. Fig. 1(b) shows the schematics of a transistor structure. As the top gate is biased to be more positive, the 2D holes in the GaSb QW are gradually depleted. As the top gate bias is increased further, the 2DEG is formed eventually in the InAs QW. The band bending under the inversion condition is shown in Fig. 1(c), where the two tunnelling barriers are defined by the lateral p–n junctions. If the top gate area is small enough, the number of electrons induced in the QW increases by one at a time. Such single electron tunnelling can be observed in the transconductance of the single electron transistor, as depicted in Fig. 1(d).

To verify the presense of 2D holes and the formation of 2DEG, we fabricated large-sized Hall bars (10 μm channel width) with a top gate. The DC current-voltage characteristics measured at 4.2 K in the common-source configuration, shown in Fig. 2, clearly demonstrates the switching between the accumulation, depletion, and inversion regions.

We have also used electron-beam lithography and wet etching, and successfully fabricated narrow (approximately 1 μm) channels with short (less than 100 nm) gates. When the physical channel width is less than 0.7 μm, the channel is completely depleted, indicating a depletion length of around 0.35 μm. With such a small dimension, the transistors display the expected Coulomb blockade. Fig. 3 shows a typical example. At 4.2 K, the DC drain current is measured at a fixed drain voltage of 1 mV, and the gate voltage is swept from zero to 9 V. Throughout the entire gate voltage range, gate leakage current is negligible. The drain current drops (see Fig. 3(a)) as the transistor is biased from the accumulation regime to depletion. But, when the gate voltage is swept higher, to 6 V, the single electron quantum state beneath the gated region is formed at the Fermi level, resulting in a peak in drain current (see Fig. 3(b)). As the gate voltage becomes more positive, the resonances due to the second and the third electron occupation are observed at near 7 and 8.5 V, respectively.

The quantum dot addition energy for the second and the third electrons are found to be 15 and 35 meV, respectively. If we model the QD as a disc with a radius r, the obtained capacitance of our QD suggests an effective diameter of about 20 nm, consistent with our numerical simulation considering a miniature MOS capacitor [7].

The inherent advantage of InAs that are relevant to quantum computation is its large g-factor ($|g^*| = 15$, versus 0.44 for GaAs). Therefore, in comparison with GaAs, the same amount of Zeeman splitting can be achieved by a magnetic field 30 times smaller. Other than the reduced external magnetic field, there is also an important consequence in power consumption when spins

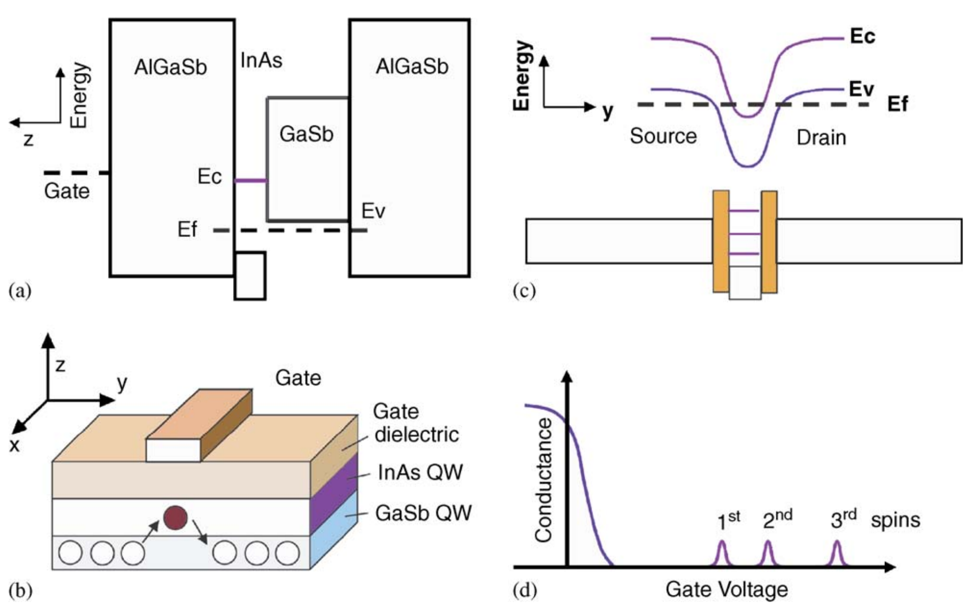

Fig. 1. (a) Schematic potential profile along the crystal growth direction (z) of the composite quantum well, which consists of an InAs/GaSb quantum well sandwiched between two AlGaSb barriers. (b) Schematic of the transistor structure. The inversion layer of electrons is formed by biasing the top gate to be more positive than the threshold voltage. Electrons are supplied by the conductive GaSb quantum well. (c) Schematic potential profile along the source-drain (normal to z-direction). The top gate is biased to induce an inversion layer underneath. The two barriers at the p–n junctions are similar to the tunnelling barriers in a double barrier interband resonant tunnelling diode, for which the energy band diagram is shown. (d) The expected dependence of transconductance versus gate voltage. The peaks indicate the first, the second, and the third spins populating the quantum dot.

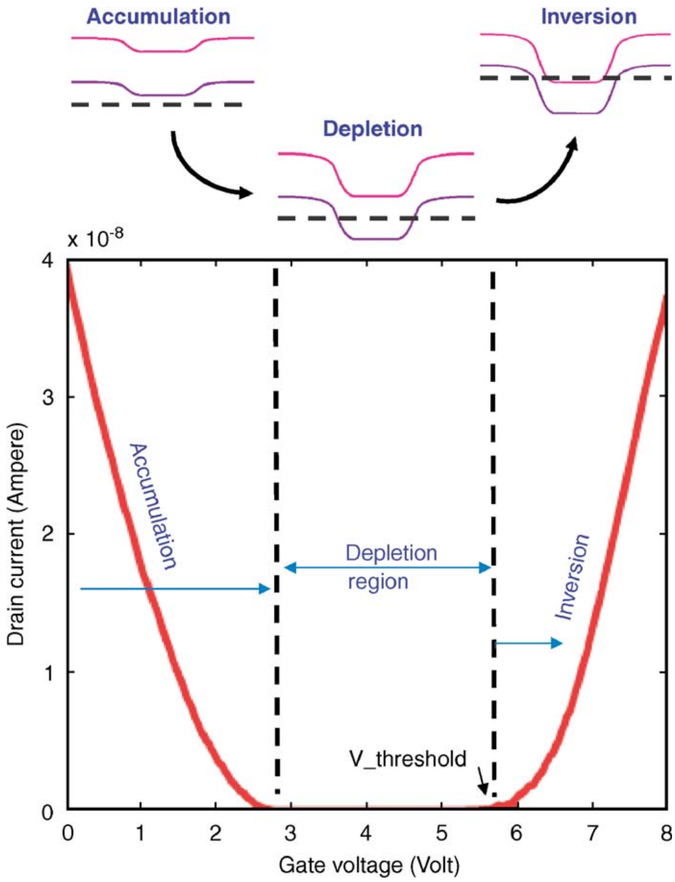

Fig. 2. The DC current-voltage characteristic of a gated Hall bar, where the source and the drain are two ohmic leads. The change in the operating regimes as the gate bias gradually increases is schematically shown. The measured drain current decreases initially due to depletion, but then increases when the 2DEG is induced. A threshold voltage ~6 V is obtained.

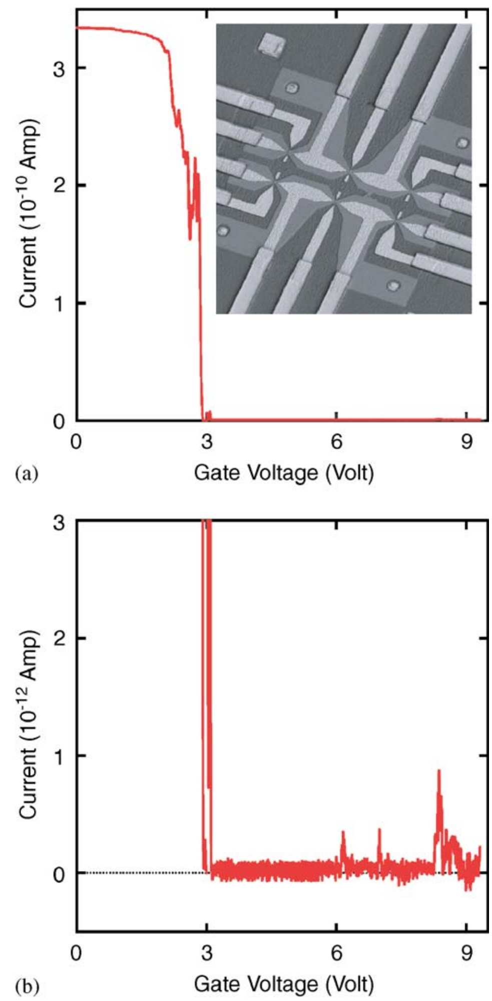

Fig. 3. (a) The DC current-voltage characteristic of a gated single electron transistor, where the drain current is plotted against the sweeping gate voltage. The drain voltage is kept at 1 mV. The inset shows a scanning electron micrograph of transistors with submicron gate length. (b) Same as that in (a), but with a different drain current scale. The peaks in current result from single electron tunnelling.

are rotated by Rabi pulses. The period of Rabi pulses should be much shorter than the spin dephasing time T_2. That is, the AC magnetic field for Rabi pulses ($B_{ac} > \hbar(g \times \mu_B T_2)^{-1}$) is about 30 times (= 15/0.44) smaller for InAs compared to GaAs, provided that T_2 are the same. A 30 times reduction in the excitation current corresponds to a factor of 900 decrease in Joule heating in the cryostat. Fig. 4 shows how our design can implement the Rabi pulse. [8] The D-gate is to induce one electron underneath, and the I-gate is DC biased to deplete holes in the surrounding area, isolating the single spin further to minimize the spin dephasing. In addition, both the D-gate and the I-gate can be AC driven to generate two perpendicular magnetic fields for controlled spin rotation. We can estimate that for $T_2 \geqslant 100$ ns, $B(\text{Rabi}) \leqslant (\hbar(g \times \mu T_2)^{-1}) = 71\,\mu$T. If the vertical spacing between the I-gate and the single spin is assumed to be 100 nm, then the AC current $I(\text{Rabi}) \leqslant 2\pi \cdot 100\,\text{nm} \times B(\text{Rabi}) = 36\,\mu$A. Were $50\,\Omega$ impedance used for impedance matching to a coax cable, the AC voltage is to be 1.8 mV. The AC Joule heating would be approximately 46 μW per qubit. With GaAs, merely from the g-factor difference, it would cost 41.4 mW per qubit.

Our InAs qubit can serve as a building block for quantum computation applications, because it is easier to scale up the qubits into a two dimensional array. The T_2 time of single electrons confined in InAs should be at least of the same order of magnitude as that in GaAs quantum dots [9]. More discussions can be found in Ref. [5]. The thermal energy, kT, at 4.2 K is much smaller than the orbital confinement energy, allowing confinement of one single electron. The tunnelling life time at the current peak is determined by the structure, and it is much larger than $\hbar/(kT)$. Finally we note that the measurement temperature is much smaller than the addition energy and the Coulomb energy, so the operation of our SET ought to be stable in a wide range of temperatures.

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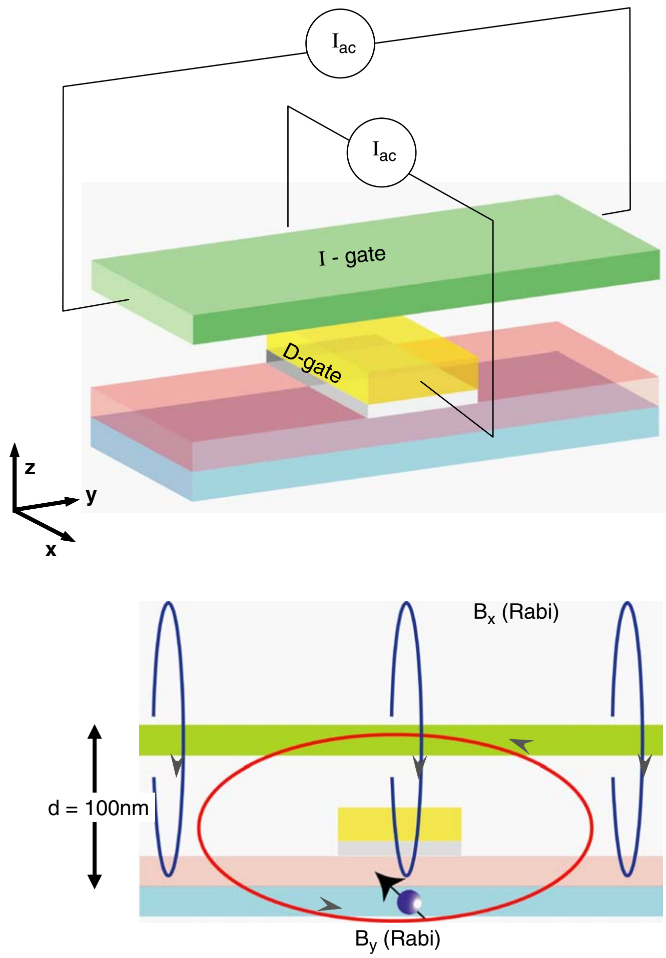

Fig. 4. (Top) Schematic of the qubit, where the D-gate induces a single spin in the InAs quantum well, and the I-gate is DC biased to deplete the region surrounding the single spin. Both D-gate and I-gate are to be AC excited for generating pulsed magnetic field for spin rotation. (bottom) Side view of the same qubit, illustrating the orientation of the two perpendicular magnetic fields.

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