All-Silicon Technology for High-Q Evanescent Mode Cavity Tunable Resonators and Filters

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Abstract—This paper presents a new fabrication technology and the associated design parameters for realizing compact and widely-tunable cavity filters with a high unloaded quality factor ($Q_u$) maintained throughout the analog tuning range. This all-silicon technology has been successfully employed to demonstrate tunable resonators in mobile form factors in the C, X, Ku, and K bands with simultaneous high unloaded quality factors ($\geq 500$) and tuning ratios ($\geq 1:2$). It is shown that by employing high-precision micro-fabrication techniques and careful modeling, the measured RF and tuning performance of the fabricated device closely match the simulated results. The capability of monolithic (system-on-chip) integration, low-cost batch processing, and compatibility with CMOS processing is some of the key advantages of this 3-D tunable filter fabrication technology over conventional approaches. This technology also has the potential to be extended to produce tunable resonators and filters in the millimeter wave region.

Index Terms—Evanescent-mode cavity, MEMS, silicon, tunable resonator, electrostatic, tunable filter, high-$Q$.

I. INTRODUCTION

The vision of the next-generation software defined radio (SDR) is to have a single reconfigurable radio with multi-band and multi-standard compatibility, that can operate effectively in dense electromagnetic radiation environments by having the required frequency agility, necessary to communicate using multiple waveforms in rapid succession. The SDR concept has been under development for several years in both military and commercial sector [1], [2] but it is still far from complete. One main area requiring significant innovation is the tunable filters for their reconfigurable RF front-end (RFFE) [3]. The search for a tunable filter technology that completely fulfills the stringent SDR requirements like low insertion loss (high-$Q$), high tuning ratio ($T/R$), easy integration, high linearity, high power handling, small size and low manufacturing cost is ongoing [3]–[5].

Several existing tunable filter technologies have been evaluated for SDR applications. The yttrium-iron-garnet (YIG) crystal based tunable filters demonstrate a high-$Q$ ($\geq 1000$) with multiple octave tuning range [6]. [7]. However, YIG filters are not well suited for portable devices due to their relatively large size, difficulty in planar integration, high power consumption, need of controlled temperature environment for proper operation, and high cost [4]. The planar or 2-D tunable filter technology is another extensively explored approach. In these filters, transmission lines are loaded with lumped tunable elements (varactors) for frequency tuning. Some of the notable tunable filter demonstrations are based on solid-state (e.g Schottky or p.i.n diode) [8]–[10], ferroelectric (e.g Barium-Strontium-Titanate (BST)) [11], [12], and micro-electromechanical systems (MEMS) [13]–[15] varactors. Planar filters have the advantages of small volume, high tuning ratio, easy on-chip integration and good power handling. However, their RF performance is suboptimal for SDR due to their low-$Q$ ($\leq 200$) [4], [16].

A third tunable filter family is the non-planar (3-D) approach, which includes cavity-based technologies with integrated tuners. This approach is rapidly gaining popularity due to their significantly small size (compared to wavelength) and weight unlike half-wave cavity resonators, their ability to achieve a higher $Q_u$ as compared to planar approach, wide tuning, large spurious-free region, high linearity and good power handling [5], [17]–[26]. Of these 3-D technologies, the capacitive-post loaded cavity filter technology has demonstrated state-of-the-art performance in the S and C-bands with a simultaneous high-$Q$ ($\geq 300$) and tuning ratio ($\geq 1:2$) [5], [17], [18]. In the capacitive-post loaded filters, the resonant frequency is highly sensitive to the parallel-plate capacitance between the post-top and cavity ceiling. By incorporating a MEMS tuner directly above the capacitive post (as a moveable cavity ceiling), few micrometers of tuner displacement causes several gigahertz shift in the resonant frequency. High-$Q$ resonators/filters with an octave (1:2) tuning range or higher can therefore be realized in both microwave and millimeter wave frequencies. Table I summarizes some simulated designs of such capacitive-post loaded resonators with a maintained $Q_u$ $\geq 500$ throughout the frequency tuning.

It may be noted from Table I that fabrication tolerances become critical in realizing repeatable and reliable filters, especially for millimeter wave applications. Existing implementations are based on cavities machined in the metallic or ceramic substrates using conventional tooling techniques, and their tuners are attached using solder, physical pressure or conductive epoxy [5], [17], [18], [27]. A conventionally machined cavity suffers from high fabrication uncertainties ($\pm 20 \mu m$) which inhibits reliable scaling of capacitive-post loaded filter technology beyond X-band (a capacitive-post radius of $\leq 100 \mu m$ is needed with a precision of $\pm 10 \mu m$). Moreover, the uncertainty due to surface
roughness in the metallic or ceramic cavity substrates, and the uniformity issues inherent with the solder paste or conductive epoxy attachment like uneven application, shrinkage, and irregular grain size can cause substantial error in the desired post-ceiling gap (>2 μm) [5], [18], [27]. These uncertainties tend to create a significant disparity between the designed and fabricated performance. For instance, in the designs of Table I, a 1-μm error in $d_{\text{min}}$ due to epoxy attachment can lead to >15% reduction in the tuning ratio.

Consequently, a fundamentally different fabrication technology with tighter tolerances is needed for high-frequency applications. This requirement becomes the premise for all-silicon capacitive-post loaded tunable filter technology based on micro-fabrication. Several topologies for high-$Q$ fixed-frequency (static) resonators and filters using micro-machined silicon cavities have already been demonstrated in the microwave and millimeter-wave regions [28]–[33]. Similarly, single-crystal-silicon has also been extensively explored as a choice material for MEMS actuators due to its superior mechanical properties [5], [34]–[37]. The all-silicon tunable filter technology aims to successfully exploit both the RF and mechanical advantages of silicon. Two noticeable performance outcomes demonstrated using this approach include 1) an X to Ku band capacitive-post loaded cavity tunable resonator with a tuning range of 9.5 to 17 GHz (1:1.87) and $Q_a$ of 650 to 950 using magnetostatic actuation [38], and 2) a C to K-band electrostatically tunable resonator demonstrating continuous tuning from 6.1 to 24.4 GHz (1:4) with a $Q_a$ varying from 300 to 1000 [39], which is state-of-the-art in the tunable filter technology for simultaneous high-$Q$ and wide tuning range.

This paper details the groundwork, design methodology and the fabrication considerations involved in the implementation of capacitive-post loaded tunable cavity filters using all-silicon approach. In the design section, simple analytical expressions are presented to predict and optimize the $Q_a$, tuning range and biasing voltage. The fabrication section explains the steps needed to produce high quality tunable filters and to minimize disparity between the simulated and measured performance. Some advantages of the all-silicon fabrication technology like accuracy, high reliability, compatibility with the growing on-chip RF technology and low-cost are briefly discussed to emphasize its potential from commercial viewpoint. Finally, notable performances of some tunable resonators fabricated and demonstrated to date are summarized and compared with some existing tunable microwave filter technologies.

### II. ALL-SILICON TECHNOLOGY OVERVIEW

In the presented all-silicon approach, silicon is used as the substrate material for fabricating all constituent components of the tunable resonator. Fig. 1(a) and (b) show the concept schematics and working principle of an electrostatically actuated all-silicon resonator, (b) Schematics and working principle. Tuning is achieved by applying bias voltage to the electrode, causing a change in capacitive gap between the post and the Au/Si diaphragm due to electrostatic actuation.

![Fig. 1. (a) The assembly of three individually micro-fabricated constituents to form an electrostatically-tuned all-silicon capacitive-post loaded cavity resonator. (b) Schematics and working principle. Tuning is achieved by applying bias voltage to the electrode, causing a change in capacitive gap between the post and the Au/Si diaphragm due to electrostatic actuation.](image-url)
is determined from the desired filter tuning range through electromechanical analysis of the diaphragm deflection.

Although the fabrication steps are customized based on specific designs as in [38] and [39], some important fabrication steps which represent the core of this all-silicon approach are given below.

A. Cavity Fabrication

As shown in Fig. 2(a), the fabrication starts with a cavity substrate Si wafer coated with a film of LPCVD silicon nitride (SiNₓ) layer. The silicon wet-etching mask is patterned in the nitride layer by selectively etching it in SF₆ plasma using a photo-resist (PR) mask. The cavity and post of desired dimensions are formed using a well-characterized silicon wet-etching process. The nitride layer is stripped and the cavity is sputtered with a gold film to provide uniform metal coverage to the sidewalls and the post.

B. Diaphragm Fabrication

The Au/Si diaphragm fabrication begins with an SOI wafer of appropriate device layer thickness. First, a gold film is deposited on the SOI device layer. Then by using a PR mold, a Au bonding ring is created over the existing gold film using electroplating or lift-off process. The thickness of the bonding ring is defined by the initial post-ceiling gap. Backside lithography is carried out to pattern the PR mask, required for creating the diaphragm by etching away the SOI handle substrate using Deep Reactive Ion Etching (DRIE). The buried oxide of SOI acts as the etch-stop layer for DRIE. Finally, the oxide layer is removed using Buffered Oxide Etch (BOE) to release a smooth and flat gold-coated SCS diaphragm. Major diaphragm fabrication steps are shown in Fig. 2(b).

C. Bias Electrode Fabrication

In order to get high precision in the electrode/diaphragm gap for electrostatic actuation, the bias electrode is also micro-fabricated. The electrode fabrication process steps are similar to cavity wet-etching process and are shown in Fig. 2(c). A Si post of appropriate height and diameter is wet-etched in the Si substrate using a (SiNₓ) mask. The nitride film is removed and the bias electrode is uniformly coated with an insulation film like PR to provide electrical isolation.

D. Assembly

After their fabrication, the cavity and tuner parts are thoroughly solvent-cleaned and UV-treated to remove any debris or organic contamination on the surface. They are subsequently aligned and bonded using Au-Au thermo-compression bonding carried out under high temperature (∼310 °C) and pressure (∼5 MPa). The assembly of these micro-machined parts to form a single resonator is shown in Fig. 1(a).

III. A Capacitive-Post Loaded Evanescent-Mode Cavity Resonator Design

Craven [40] proposed that a cutoff guide (which can be approximated as a lumped inductance), when appropriately loaded with capacitive obstacles at suitable intervals, acts as a waveguide equivalent of a lumped element circuit filter. The capacitive-post loaded evanescent-mode cavity resonators and filters are designed on the same principle. The advantages include considerable size and weight reduction compared to a half-wave resonator with the same resonant frequency and a large spurious-free region [28]. Fig. 3 shows the cross-section of a typical capacitive-post loaded cylindrical cavity operating in evanescent mode. The important design parameters are
Fig. 3. Concept schematics of a capacitive post loaded cavity resonator showing important dimensions and reactive elements of the cavity.

Fig. 4. Change in frequency and unloaded quality factor as a function of post gap.

capacitive post radius \(a\), cavity radius \(b\), capacitive post height \(h\) and gap \(d\) between the post-top and cavity ceiling. The resonant frequency \(f_0\) can then be approximated by [32], [41]

\[
f_0 \approx \frac{1}{2\pi \sqrt{L_0(C_0 + C_{ff} + C_{pp})}}
\]

\[
C_{pp} = \frac{\epsilon_0 \pi a^2}{d}
\]

where \(L_0\) and \(C_0\) are the fixed equivalent cavity inductance and capacitance respectively. \(C_{pp}\) and \(C_{ff}\) are the parallel-plate and fringing-field capacitances between the post and cavity ceiling. When the post-height approaches the cavity-height (highly loaded) such that \(C_{pp}\) dominates other capacitances, the gap \(d\) becomes the main resonant frequency determining parameter, as shown in Fig. 4.

Based on the fabrication technology, various cavity and post shapes have been explored such as cylindrical [5], [18], square [17] and pyramidal [31], [32], [38], [39]. From the design viewpoint, a cylindrical cavity and post is relatively easy to model as it can be closely approximated as a small segment of coaxial transmission line shorted at one end, and a series capacitor at the other [5]. Using this analogy the resonant frequency, tuning range and \(Q_u\) for a cylindrical cavity can be analytically predicted. The unique shape of the micromachined Si cavity and post, due to the anisotropic Si wet-etching, makes it difficult to relate the \(Q_u\) and resonant frequency with cavity dimensions analytically. Therefore, FEM based solvers like Ansys HFSS® [42] are initially used even for preliminary design parameters. However, a comparison of the simulated electric and magnetic field patterns of a cylindrical to pyramidal cavity of similar dimensions \((a, b, h\ and \ d)\) show strong similarities (refer Fig. 5). As a result, the resonant frequency and \(Q_u\) of these cavities are also found similar as shown in Fig. 6 and Fig. 7 respectively. Hence, the analytical expressions obtained from cylindrical cavity analysis can provide a good starting point for our all-silicon cavity resonator designs.

Fig. 5. Field comparison for a cylindrical and micromachined Si cavity: (a) Electric field, mainly concentrated at the post, (b) Magnetic field, circling around the post.

Fig. 6. Frequency vs. gap plot for different shaped cavities of similar dimensions.
A. Resonant Frequency and Tuning Ratio

The LC-tank model from (2) can be expanded to relate the resonant frequency with cavity dimensions \((a, b\) and \(h\)) as follows:

\[
f_0 \approx \frac{1}{2\pi \sqrt{L_0(C_{\text{parasitic}} + C_{pp})}}
\]

where

\[
C_{\text{parasitic}} = C_0 + C_{ff}
\]

\[
L_0 \approx \frac{\mu_0 h}{2\pi} \ln(b/a)
\]

\[
C_0 \approx \frac{2\pi \varepsilon_0}{\ln(b/a)}
\]

\[
C_{ff} \approx K_1 \varepsilon_0 \ln(h/d)
\]

\(C_{\text{parasitic}}\) is a capacitance that does not contribute to the sensitivity of resonant frequency \(f_0\) with change in gap \(d\). \(K_1\) is an empirically fitted constant which is sensitive to \(a/b\) ratio. For \(a/b \leq 0.3\), this constant has been found to be 2.78 [43]. The tuning ratio of the resonator can then be computed by

\[
T.R = \frac{f_{\text{max}}}{f_{\text{min}}} \approx \sqrt{\frac{C_{\text{parasitic}} + \varepsilon_0 \pi a^2/d_{\text{min}}}{C_{\text{parasitic}} + \varepsilon_0 \pi a^2/d_{\text{max}}}}
\]

where \(d_{\text{min}}\) and \(d_{\text{max}}\) are the minimum and maximum gaps between post-top and the cavity ceiling respectively, achieved through ceiling deflection. From (3) and (8), the \(f_0\) and \(T.R\) of the resonator depend on 1) cavity shape and dimensions, 2) minimum gap \(d_{\text{min}}\), and 3) ceiling deflection.

1) Cavity Shape and Dimensions: The effects of \(a\), \(b\) and \(h\) on the resonant frequency are highlighted in Fig. 8(a), (b) and (c) respectively. Reducing any of these dimensions, corresponds to lowering the overall capacitance and therefore causes the resonant frequency to increase. The resonant frequency is more sensitive to the post radius \(a\) than the other two dimensions because \(a\) directly impacts the dominant parallel-plate capacitance, whereas \(b\) and \(h\) affect the parasitic capacitance. For millimeter-wave applications, a capacitive post of very small radius (10s of micrometers) with high precision is needed. This constraint plays a major role in the choice of suitable fabrication technology for high frequency applications. A lower parasitic capacitance compared to parallel plate capacitance results in higher tuning range.

2) Minimum Gap \((d_{\text{min}})\): The parallel plate capacitance \(C_{pp}\), which is the dominant capacitance for tuning purposes, have an inverse relationship with \(d\). Therefore, for the same ceiling deflection, a higher tuning ratio can be achieved through lower \(d_{\text{min}}\).

3) Ceiling Deflection: A higher actuation stroke corresponds to better tuning ratio for the same \(d_{\text{min}}\). The resonator frequency \(f_0\) tends to saturate as the post-ceiling gap increases such that \(C_{pp}\) approaches \(C_{\text{parasitic}}\). The ceiling deflections beyond this point has negligible impact on the tuning ratio. The extent of ceiling deflection is determined by the the actuation mechanism and the stiffness of the ceiling. The stiffness \(k\)
for a circular diaphragm of radius \( R \) and thickness \( t \) under uniform loading can be calculated by [9]:

\[
k = k' + k'' = \frac{16\pi E t^3}{3R^2(1-\gamma^2)} + 4\pi \sigma t
\]  

(9)

where \( E \) is the Young’s modulus, \( \gamma \) is the Poisson’s ratio and \( \sigma \) is the residual stress in the diaphragm. The \( k' \) component of stiffness depends upon material properties and dimensions, whereas \( k'' \) depends mainly upon the fabrication technology and is generally the dominant stiffness contributing mechanism due to difficulty in fabricating low-stress diaphragms. In case of a Au/Si diaphragm, which is extensively used in this work, the Au thickness \( t_{Au} \) and residual stress \( \sigma_{Au} \) are the dominant stiffness contributors due to the stress-free nature of crystalline silicon [5]. Therefore the \( k'' \) part of the stiffness in (9) is generally several times higher than \( k' \) and we can approximate the diaphragm stiffness to be

\[
k \approx k'' = 4\pi \sigma_{Au} t_{Au}
\]  

(10)

Electrostatic actuation is the most widely used MEMS actuation scheme due to its near-zero power consumption, design-simplicity and high-speed [9]. Fig. 9 shows the schematic of an electrostatically actuated Au/Si bi-morph diaphragm. When a voltage \( V \) is applied to the bias electrode, the electrostatic force pulls the diaphragm towards the electrode by a displacement \( x \). The diaphragm stiffness \( k \) creates a reactionary restoring force proportional to this displacement. At equilibrium, the electrostatic and restoring forces balance each other i.e.

\[
kx = \epsilon_0 \frac{A_{bias} V^2}{2(g_0 - x)^2}
\]  

(11)

where \( A_{bias} \) is the bias electrode area and \( g_0 \) is the initial gap between the bias electrode and the un-deflected diaphragm. Using this parallel-plate actuation of diaphragm, a continuous deflection can be achieved for only one-third of the actuation gap (\( g_0/3 \)), followed by the “pull-in” instability. Therefore, for analog resonator designs, the initial gap between the diaphragm and bias electrode should be, at least, three times the required diaphragm deflection to achieve the desired tuning range. The bias voltage needed to achieve the required deflection therefore depends mainly upon \( k \), \( A \) and \( g_0 \). From (9) and (11), the Au/Si diaphragm parameters \( \sigma_{Au}, t_{Au}, R \) and \( t_{Si} \) should be carefully considered in the design process to determine the bias voltage for the required diaphragm deflection as shown in Fig. 10.

### B. Quality Factor

The unloaded quality factor of a cylindrical evanescent-mode cavity can be analytically approximated using the following equation [44]:

\[
\frac{1}{Q_u} \approx \frac{R_s}{2\pi \mu f_0} \left( \frac{1}{b} + \frac{1}{h} \right) \left( \ln\left(\frac{2}{h}\right) + \frac{2}{h} \right)
\]  

(12)

where \( R_s \) is the sheet resistance of the cavity sidewalls. From (12), the \( Q_u \) of the resonator at a particular frequency is mainly dependant on: 1) cavity dimensions and 2) sheet resistance.
1) **Cavity Dimensions**: Two general rules can be employed to maximize the quality factor of the resonator on the basis of cavity dimensions, provided it does not affect the desired tuning range: 1) increasing $b$ or $h$ results in higher quality factor because it allows more volume for energy to be stored in a resonator, as shown in Fig. 11 and Fig. 12 respectively, as long as $b$ and $h$ are much smaller than the resonant wavelength, 2) when the post radius $a$ is approximately $0.28 \times$ the cavity radius $b$, which can be mathematically validated from (12).

2) **Sheet Resistance**: $Q_u$ is inversely proportional to the resistance offered by the cavity walls to the RF current which is approximated by:

$$R_s = \frac{\rho}{t} \approx \frac{1}{\sigma \delta} \quad (13)$$

$$\delta = \frac{1}{\sqrt{\pi} \mu f_0 \sigma} \quad (14)$$

where $\rho$ and $\sigma$ are the cavity metal resistivity and conductivity respectively. The metal thickness $t$ can be replaced by the skin depth $\delta$, provided $t \gg \delta$. Therefore highly conductive metals like Cu, Au and Ag are desirable for high-$Q$ resonator fabrication.

IV. **FABRICATION TECHNOLOGY**

The important considerations in determining the suitability of all-silicon technology for realizing capacitive-post loaded tunable microwave filters include precision, reliability, compatibility and cost.

A. **Precision**

A successful fabrication technology should be accurate and consistent. In order to realize high frequency capacitive-post loaded tunable filters, precision is mainly needed in 1) dimensions, 2) surface profile (roughness), and 3) integration of constituent parts.

1) **Dimensional Accuracy**: As can be seen from Fig. 8, for millimeter wave applications the capacitive post dimensions are in the order of 10s of micrometers, and a small deviation in post size can cause a major shift in resonant frequency and tuning performance. The resolution of existing machining techniques is inadequate for these tight tolerances. Silicon wet micro-machining, when carried out in a well characterized, temperature and concentration controlled etch-bath, can provide the precise dimension control necessary for this application. High-precision characterization tools like laser confocal microscope or profilometer are required to accurately monitor to dimensions. In our work, laser confocal microscope LEXT$^{TM}$ from Olympus® is used for the etch characterization which has the capability to measure cavity dimensions with sub-micrometer precision [45]. The etch-depth (Fig. 13(a)) and post-area (Fig. 13(b)) is measured at regular intervals and plotted against etch time (Fig. 13(c)), to extract the lateral and vertical etch rates. These etch rates can then be used for fabricating cavities with post of desired dimensions with high precision.

2) **Sidewall Roughness**: In transmission lines, RF losses increase with surface roughness and are especially pronounced at higher frequencies when the roughness is comparable to skin-depth [46], [47]. Similarly, since the RF current concentrates to the “skin” of the cavity sidewalls and post, the surface roughness increases the sheet resistance of the cavity and degrades the $Q_u$. To estimate the impact of roughness on $Q_u$ at different frequencies in a capacitive-post loaded resonator, we have used HFSS simulations and found a $Q_u$ degradation trend with increased roughness, as expected. The impact of roughness on $Q_u$ is higher at high frequencies as shown in Fig. 14. Since the purpose of these simulations is to measure the trend not the actual values, the roughness is approximated by uniformly spaced ridges in the cavity base, sidewalls, and post as shown in the inset of Fig. 14. When the cavities are fabricated using conventional machining, the tooling process leaves its tracks and irregular marks on the cavity sidewalls and
post, which are extremely difficult to polish in small cavities (few millimeters) with a fragile rough post in their center. Depending upon the equipment precision, this roughness can be in the order of 2–20 μm. Using the wet chemical etching of silicon, cavity/ posts sidewalls with mirror-like surface finish and sub-micrometer roughness can be obtained. Fig. 15 shows sidewall roughness comparison of a conventionally machined cavity with post in bulk copper to a micro-machined Si cavity of similar dimension.

3) Cavity-Ceiling Attachment: High conductivity, uniformity and accuracy are three essential requirements in the cavity-ceiling integration. A highly conductive attachment will offer less resistance to the RF current whereas a uniform attachment will result in symmetric current distribution. Both of these factors impact the resonator $Q_u$. In the ceramic cavities, the cavity-tuner attachment is done using conductive silver epoxy [5], [18] with an approximate conductivity of $2 \times 10^6$ S/m [48]. The $Q_u$ of a resonator with Cu or Au as the cavity metal suffers a substantial degradation (more than 30% simulated for Au vs. epoxy) in $Q_u$ due to this bonding metal conductivity variation (Fig. 16). Another disadvantage
of epoxy based cavity-ceiling attachment with rough cavity surfaces, is the high-uncertainty in determining the post-ceiling gap \(d_0\) and parallel-plate capacitance \(C_{pp}\). This is explained in Fig. 17. In an all-silicon approach, we eliminate the issue of roughness of mating surfaces by exploiting the smoothness and flatness of the Si wafers which are received polished and leveled to sub-micrometer accuracy at the foundries. With Au as the cavity metal, several precise and conductive attachment methods are available including the highly conductive Au-Au thermo-compression bonding \(\sigma_{Au} \approx 4.1 \times 10^7 \text{ S/m}\). Au-Au thermo-compression bonding has been successfully employed in several micromachined static resonators and filters [28], [29], [31], [32], and [49]. The role of a bonding ring in this all-silicon approach is very important in accurately establishing the initial-gap \(d_0\). The thickness of the bonding ring can be accurately controlled using well-characterized metal deposition methods commonly used in microfabrication, like e-beam evaporation, sputtering and electroplating.

### B. Reliability

The reliability of a contact based MEMS (DC and capacitive switches) has been challenged by problems like stiction, fatigue and creep and dielectric charging [9]. Special techniques like use of novel contact material, modified actuation waveform and proprietary fabrication processes have been developed to mitigate these failure mechanisms and currently several switch technologies have reliably demonstrated over a billion switching cycles [50]–[53]. Contact-less MEMS are preferred in the tunable filter applications where analog tuning
range is desired. In contact-less MEMS, creep and hysteresis are the two main failure mechanisms that can reduce the device repeatability and reliability [5]. The piezoelectric actuation of a copper clad lead-zirconate-titanate (PZT) diaphragm as used in [18] suffer from substantial hysteresis. Whereas electrostatic actuation of gold coated single-crystal-silicon (SCS) diaphragm used in this work has been demonstrated to be almost creep-free with no hysteresis in the analog tuning range [5].

C. Ease of Integration

The monolithic integration of the RF components minimizes fabrication complexity and interconnect losses [28], [29], [32], [49], and [54]. Silicon has become the most highly used RF substrate with the popularity of CMOS RFICs, therefore the compatibility of filter fabrication with CMOS processes is highly desirable. The all-silicon filter technology has this unique edge over the previous cavity based tunable filter approaches that it allows system-on-chip integration with CMOS and SOI CMOS RFICs. Two variations of planar integration have been demonstrated where the RF feed can either be on the SOI diaphragm (Fig. 1) or on the cavity substrate [38]. In addition, coaxial pin feed for filters has also been successfully investigated and demonstrated in this all-silicon approach [39], to show the compatibility of this technology with the modular RF designs.

D. Cost

All-silicon filters can be reliably and economically produced using standard microfabrication equipment and processes. Unlike conventional filter fabrication methods which required individual machining and assembling of each filter, it is a wafer-level batch fabrication approach which is fast, consistent and cost-effective.

V. PERFORMANCE ANALYSIS

We summarize the results of three different all-silicon resonator designs, to demonstrate the versatility of this approach along with its performance.
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Fig. 24. All-Si tunable resonators performance comparison with other tunable resonator/filter technologies [5], [14], [17], [18], [22], [23], [38], [39], [56]–[58]. The comparison is based on the highest $Q_u$ reported at their highest $f_0$ and the tuning ratio.

A. 15.5 GHz Static Resonator

A proof-of-concept resonator is fabricated to check the feasibility of our all-silicon approach for making high frequency capacitive-post loaded cavity filters with high accuracy and desired performance. The resonator is designed for a fixed resonant frequency of 15.5 GHz with a $Q_u$ of 780, when the post-ceiling gap is fixed to 10-μm. It is excited with a planar short-ended CPW feed on the cavity ceiling, that enters the cavity via feed-through slots etched on cavity top sidewalls. The fabricated cavity and ceiling parts are shown in Fig. 18. The measured device demonstrated a $Q_u$ of 700 at 15.71 GHz which corresponds to 90% of the simulated $Q_u$ with ≤2% deviation from targeted frequency, as shown in Fig. 19. The extracted $d_0$ from simulations is 10.6 μm which corresponds to ≤1 μm fabrication uncertainty in $d_{\text{min}}$.

B. 8–18 GHz Resonator With Magnetostatic Actuation

In [38], the all-silicon tunable filter technology is demonstrated for the first time using magnetostatic MEMS actuation. The cavity and diaphragm are fabricated and assembled using the procedure described earlier in section II. However, to implement magnetostatic actuation of the diaphragm, magnetic field interactions between a PCB mounted current carrying coil and a small permanent magnet attached to the back of the diaphragm are exploited. Using bi-directional magnetostatic actuation, the diaphragm is designed to actuate between 5–40 μm from the post to achieve 8 to 18 GHz tuning with a $Q_u$ of 950–1500. The resonator is fed by an open-ended microstrip line patterned at the back of the cavity. The field is coupled through a rectangular slot etched inside the cavity gold. A coplanar waveguide (CPW) to microstrip transition is incorporated to perform on-wafer probing. Fig. 20 shows the measured transmission ($S_{21}$) parameters of a weakly coupled, magnetostatically actuated all-silicon resonator. The resonator tuned from 9.5 to 17 GHz with the $Q_u$ of 650–950 when the coil current was changed between ±70 mA.

C. 12–24 GHz Resonator With Electrostatic Actuation

The electrostatic actuation of an Au/Si diaphragm is employed for a 12–24 GHz all-silicon resonator. A diaphragm deflection from 2–15 μm from the post is required to achieve the desired tuning range, with a simulated $Q_u$ of 600–1350. The cavity is excited using a coaxial pin inserted through a via etched in Si cavity bottom. The fabricated parts and resonator assembly is shown in Fig. 21. From the measured reflection ($S_{11}$) parameters presented in Fig. 22, the resonator continuously tuned from 12.3 to 23.7 GHz when the bias voltage is ramped to 370 V. A further increase in voltage resulted in a discrete frequency jump to 25 GHz due to electrostatic pull-in effect. An unloaded quality factor of 510–1020 is extracted through data post-processing using reflection method [55].

1) Tuning Range Enhancement: The tuning range of this electrostatic is enhanced by introducing a thin (0.5 μm) low-loss Parylene-N ($\epsilon_r = 2.65$, $\tan \delta = 0.0006$ at 1 MHz) spacer film between the post and the diaphragm as demonstrated in [39]. This Parylene-N film accurately allows sub-micrometer gaps between the cavity and the post, not easily possible with an air-gap. Moreover, the high relative permittivity of Parylene-N further enhances the capacitive density at small deflections. With this modified approach, the fabricated resonator demonstrated a tuning range from 6.1 to 24.4 GHz (see Fig. 23) with a $Q_u$ of 300–1000. To the best of authors’ knowledge, this is the highest reported tuning ratio (1:4) to date in the MEMS based tunable filter technology.

A comparison has been made between the existing tunable filter technologies with the all-silicon approach, based on the
reported performance in terms of highest operating frequency, unloaded quality factor and tuning ratio in Fig. 24. It can be seen that the performance of all-silicon resonators is superior to all other approaches demonstrated to date.

VI. CONCLUSION

The capacitive-post loaded 3-D filter technology has great potential for realizing compact, high-$Q$ ($\geq 500$) and widely tunable ($\geq 1:2$) filters suitable for microwave and millimeter wave SDR applications. However, this performance is strongly dependent on the fabrication technology due to tight design tolerances. Conventional fabrication methods used for realizing capacitive-post loaded filters have suboptimal precision which impedes reliable scaling of these filters beyond X-band. The presented all-silicon technology utilizes microfabrication tools and techniques to achieve the desired accuracy. This paper focused on design, optimization and fabrication techniques for the all-silicon capacitive-post loaded cavity resonators to simultaneously achieve high-$Q$ and tuning ratio. Three different RF feed variations are presented to show the diversity in the all-silicon approach. Some notable technology demonstrations include 1) a 9.5–17 GHz (1:1.87) magnetostatically tunable all-silicon resonator with a $Q_u$ of 650 to 950, and 2) an electrostatically tunable 12.3–23.7 GHz (1:1.93) resonator with a $Q_u$ of 510 to 1020. The tuning ratio of the electrostatically actuated resonator has been doubled to 6.1 to 24.4 GHz (1:4) by introducing a low-loss dielectric film between the post and diaphragm to achieve a sub-micrometer capacitive gap. This two octave (C to K-band) tunable resonator with a high-$Q$ of 300 to 1000 is state-of-the-art in the present tunable filter technology. With this supreme RF performance and advantages like high reliability, compatibility with the on-chip RF technology and a low cost batch production, it is believed that the all-silicon filters will have a significant contribution in the realization of next-generation reconfigurable RF front-ends.

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