All Two-Dimensional, Flexible, Transparent, and Thinnest Thin Film Transistor

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ABSTRACT: In this article, we report only 10 atomic layer thick, high mobility, transparent thin film transistors (TFTs) with ambipolar device characteristics fabricated on both a conventional silicon platform as well as on a flexible substrate. Monolayer graphene was used as metal electrodes, 3–4 atomic layers of h-BN were used as the gate dielectric, and finally bilayers of WSe2 were used as the semiconducting channel material for the TFTs. The field effect carrier mobility was extracted to be 45 cm2/(V s), which exceeds the mobility values of state of the art amorphous silicon based TFTs by ~100 times. The active device stack of WSe2–hBN–graphene was found to be more than 88% transparent over the entire visible spectrum and the device characteristics were unaltered for in-plane mechanical strain of up to 2%. The device demonstrated remarkable temperature stability over 77–400 K. Low contact resistance value of 1.4 kΩ-μm, subthreshold slope of 90 mV/decade, current ON–OFF ratio of 107, and presence of both electron and hole conduction were observed in our all two-dimensional (2D) TFTs, which are extremely desirable but rarely reported characteristics of most of the organic and inorganic TFTs. To the best of our knowledge, this is the first report of all 2D transparent TFT fabricated on flexible substrate along with the highest mobility and current ON–OFF ratio.

KEYWORDS: 2D Crystal, graphene, thin film transistor, flexible electronics

Two dimensional (2D) layered materials like graphene, hexagonal boron nitride (h-BN), and transition metal dichalcogenides (TMDs) are receiving significant attention across all scientific disciplines due to their unique electrical, mechanical, thermal, and optical properties.1–4 High carrier velocity, exceptional mechanical stability, and near invisibility of graphene had already resulted in its commercialization as stretchable and transparent electrodes and interconnects.1–4 Graphene has also been substantially investigated as an alternative to silicon for beyond CMOS nanoelectronics. However, the absence of a sizable bandgap prevents the use of graphene in the logic circuits and has paved the way for the exploration of semiconducting TMDs like MoS2, WSe2, MoSe2, among others. Several high-performance field effect transistors (FETs) based on TMDs have been demonstrated in the recent literature.7–12 Various studies also indicate the potential of TMDs for optical, mechanical, chemical, and thermal applications.13–17 Finally, h-BN complements both, highly conductive graphene and semiconducting TMDs, not only by being a large bandgap insulator, but also, often as a substrate with better interface qualities.5,6 Integrating the unique properties of these different 2D materials therefore provides numerous possibilities to shape the future of nanoelectronics.

One of the most promising applications of optimally stacked 2D materials is as thin film transistors (TFT). The recent outburst of the display technology has made it even more appealing because the light emitting diodes (LEDs) and liquid crystal displays (LCDs) are driven by TFTs. TFTs are also used in RFID tags, flexible electronic devices, and for sensing applications. Although, the thin film transistor industry is reasonably mature, it is nowhere close to the ultimate potential due to limited material choices. Amorphous silicon (a-Si) is the most popular and widely used material for the TFTs,18,19 Numerous organic and inorganic materials had also been extensively explored.20–23 However, search for the better materials is still on. The most desirable features of TFTs are high carrier mobility, high ON–OFF current ratio, low contact resistance, presence of both electron and hole conduction, high optical transparency, temperature stability, and mechanical flexibility.24 The 2D layered materials are a natural choice for the TFTs in order to meet these requirements. Moreover, their inherent electrostatic integrity allows them to operate at low
power and also make them more scalable. In this article, we experimentally demonstrate all 2D TFTs with monolayer graphene as metal electrodes, 3–4 atomic layers of h-BN as the gate dielectric and bilayers of WSe₂ as the semiconducting channel material. We extracted electron mobility of 34 cm²/(V s) and hole mobility of 45 cm²/(V s) that exceed the channel material. We extracted electron mobility of 40 cm²/(V s) and hole mobility of 45 cm²/(V s) that exceed the channel material.

Figure 1. (a) False color SEM image (b) 3D cartoon, and (c) cross sectional view of an all 2D TFT with graphene as metal electrode, h-BN as gate dielectric and WSe₂ as the semiconducting channel material.

underlying WSe₂ acts as just an additional dielectric layer. Figure 2c shows the position of the Fermi level inside graphene in response to the applied back gate bias screened by bilayer WSe₂. We have used the Landauer formalism for current transport and taken into account the quantum capacitance contribution in order to solve the self-consistent Poisson equation to calculate \( \Psi_{\text{GRAPHENE}} \). The details can be found elsewhere. The numerical calculations backed by experimental observations suggest that the Fermi level in graphene can be moved by ~300 meV on either side of the Dirac point over the applied gate bias range. This is an important finding in the context of graphene to WSe₂ contact as will be discussed next.

The presence of both the electron and the hole conduction in our WSe₂ thin film transistor (Figure 2a) strongly suggests that the Dirac point of graphene aligns close to the middle of the bandgap of WSe₂. Because the bandgap of bilayer WSe₂ is ~1.3 eV, this would indicate the existence of large Schottky barrier heights at graphene to WSe₂ contacts for both electron injection into the conduction band (\( \Phi_{\text{NB}} \)) and hole injection into the valence band (\( \Phi_{\text{NP}} \)) as shown in the associated band diagram in Figure 2d (brown box). When a negative gate bias is applied, the energy bands in WSe₂ bend to facilitate hole injection into the valence band and at the same time the Fermi level in graphene also moves closer to the valence band, thereby reducing the effective Schottky barrier height for hole injection to \( \Phi_{\text{P}} \) as shown in the purple box in Figure 2d. Similarly for positive gate bias, the energy bands in WSe₂ bend to facilitate electron injection into the conduction band and at the same time the Fermi level in graphene also moves closer to the conduction band, thereby reducing the effective Schottky barrier height for electron injection to \( \Phi_{\text{P}} \) as shown in the black box in Figure 2d. Using the technique proposed by Das and adjusting the effective bandgap of WSe₂ to take into account the band movement in graphene, the height of the Schottky barrier at the graphene-WSe₂ contact was extracted to be 0.38 eV for the electron injection into the conduction band and 0.22 eV for the hole injection into the valence band at threshold bias condition. Figure 2e,f shows the partially top-gated transfer characteristics of the same TFT with h-BN as the gate dielectric and graphene as the gate electrode corresponding to two different biasing condition of the back gate, \( V_{\text{BG}} = 10 \text{ V} \) and \( V_{\text{BG}} = 25 \text{ V} \).
For negative back gate biases, the WSe₂ flake is electrostatically p-doped and hence the top gated device exhibits p-FET characteristics, while for positive back gate biases the WSe₂ flake is electrostatically n-doped and hence the top gated device exhibits n-FET characteristics. The subthreshold slope was found to be \( \sim 90 \, \text{mV/decade} \) for the p-FET and \( \sim 130 \, \text{mV/decade} \) for the n-FET.

The field effect mobility values were extracted using the conventional equation for \( g_m = \mu C_{OX} (W/L) V_{DS} \) (where \( g_m \) is the trans-conductance, \( \mu \) is the field effect mobility, and \( W \) and \( L \) are the channel width and the channel length, respectively, \( C_{OX} = \epsilon_{OX}/d_{OX} \) where \( \epsilon_{OX} \) is the dielectric constant and \( d_{OX} \) is the thickness of the gate oxide, \( d_{OX} = 3 \, \text{nm} \) and for h-BN, \( \epsilon_{OX} = 6 \times 10^{-11} \), which gives \( C_{OX} \sim 3.10^{-2} \, \text{F/m}^2 \), and finally \( L \sim 5 \, \mu\text{m} \)) from the back-gated device characteristics. The field-effect mobility values were found to be 24 and 45 cm²/(V s) for electrons and holes, respectively. The reader should note that the mobility of amorphous Si is in the range of 0.5–1 cm²/(V s).
s) while the mobility of most of the organic semiconductors is <1 cm²/(V s).²⁰,²⁴ Our mobility values therefore outperform the state of the art TFT technologies by ∼2 orders of magnitude. Metal oxide semiconductors like indium tin oxide, ZnO, and most recently alloys like InGaZnO had demonstrated mobility values as high as 1−100 cm²/(V s) but the oxide TFTs suffer significantly from threshold voltage shift and hence electrical instability due to doping created by oxygen vacancies.²²−²⁴ Our all 2-D TFTs show remarkable threshold voltage stability when measured in vacuum and air as well as over a span of time. Nanowire and carbon nanotube based TFTs had also demonstrated mobility values in the range of 10−100 cm²/(V s).³⁰,³¹ However, the placement of the wires/tubes and the variability in their transport properties depending on their dimensions (diameters) and connectivity (percolation path in a film) are major challenges in the realization of TFTs using these materials. The fact that the 2D materials can be grown over large area eliminates the placement problem and at the same time their natural sheet like structure keeps the diffusive transport models applicable in order to benchmark their performance limits.

The drive current (I_{DRIVE}) is another important parameter for the TFTs in the context of LEDs and LCDs. Depending upon the material and the desired brightness, a single pixel of an organic LED requires 1−10 μA of current. Note that this drive current is easily achieved in our all 2D TFTs at a drive voltage of as low as V_{DS} = V_{GS} = 1 V. Also note that our experimental prototype device is not scaled properly (channel lengths are in several micrometers). A properly scaled device can have much higher drive current densities at even lower voltages. This will allow reduction of active device area for the TFTs. Moreover, a single TFT can potentially drive several LEDs, which will reduce cost, power dissipation, as well as open up avenues for innovative circuit design.

The drive current is also important in the context of LCDs. The charging time of a pixel is inversely proportional to the drive (charging) current (τ = V_{DD}C_{PIXEL}/I_{DRIVE}, where τ is the charging time, V_{DD} is the supply voltage, and C_{PIXEL} is the pixel capacitance). For a standard pixel capacitance in the range of 0.1−1pF, our all 2D TFTs will have a charging time of 0.1−1 μs. The resolution of an LCD (β = V_{DD}C_{PARA}/C_{PIXEL}, where C_{PARA} is the parasitic capacitance) can also be significantly enhanced by using our all 2D TFT. For a standard parasitic capacitance of 50 fF, resolution of 5−50 mV can be achieved. Finally a figure of merit (γ = τ^{−1}β^{−1}) as high as 10⁸−10¹⁰ can be obtained which is 2−4 orders of magnitude higher than the state of the art a-Si TFTs.

One of the major reasons for fabricating our all 2D TFT on silicon platform is to demonstrate high degree of compatibility with the conventional CMOS technology. As the fundamental limitations do not allow Si to scale below 10 nm technology node without compromising severely on the device performance, low-dimensional materials, especially 2D semiconducting transition metal dichalcogenides (TMDs) will become more and more relevant in the context of high-performance CMOS as well. Our earlier studies related to channel length scaling, good quality contact formation, and layer thickness optimization of TMDs has shown a lot of promise.³²−³⁵ We have also implemented low power device concepts like tunneling FETs with the TMDs. There is a widespread concern about the low mobility values of the TMDs impacting the ON state performance of FETs.³⁶ However, one should remember that for technology nodes beyond 10 nm the devices will be dominated by ballistic transport and hence the more important parameters are going to be the carrier injection velocity and 

![Figure 3](image-url)

**Figure 3.** (a) Thinnest field effect transistor on flexible PET substrate. (b) Transfer characteristics and (c) output characteristics of the TFT. (d) Experimental setup to measure the strain effect. (e) Device characteristics under strain and (f) transparency of the TFT and its individual components.

dx.doi.org/10.1021/nl5009037 | Nano Lett. 2014, 14, 2861−2866
density of conducting modes. While carrier injection velocity of the TMDs are very similar to Si, the number of conducting modes for the TMDs far exceed Si due to their large effective masses (by a factor of 2−3).\textsuperscript{37} Moreover, the quantum effects (mostly reflected in increasing the bandgap of Si) will be absent when the channel thickness is scaled down for the TMDs. One of the major concerns for scaled transistors based on low-dimensional materials is the nonscalability of contact resistance due to finite transfer length and schottky barrier at the interface with the metal electrode. In this article, we have clearly demonstrated that such contact resistance values can be significantly reduced by using graphene as the electrode material.

Finally, Figure 3a shows our all 2D thin film transistors fabricated on a flexible PET substrate. Flexible electronics is another burgeoning industry with a lot of promise. The fact that most of the 2D materials are mechanically stable make them the natural choice for flexible electronics. Figure 3b,c shows the transfer and output characteristics of fully top gated device (note that the TFTs on shows the transfer and output characteristics of fully top gated another burgeoning industry with a lot of promise. The fact fabricated on a

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