Current and Noise Properties of InAs Nanowire Transistors With Asymmetric Contacts Induced by Gate Overlap

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Current and Noise Properties of InAs Nanowire Transistors With Asymmetric Contacts Induced by Gate Overlap

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Abstract—Nanowire transistors are typically fabricated as geometrically symmetrical devices, with metal/semiconductor source and drain contacts rather than a graduated doping profile. While the source and drain contacts are nominally identical, contact asymmetry can arise when the gate contact is not centered over the nanowire, leaving uneven access regions with no gate coverage on one or both sides of the channel. Measuring the characteristics of devices with symmetric and asymmetric contact geometries allows contact effects to be studied. In this paper, indium arsenide nanowire transistors were fabricated with symmetric and asymmetric gate coverage. It is shown that devices with highly asymmetric gate coverage can exhibit a factor of 10 change in current and a shift in threshold of up to 0.5 V upon reversing the source–drain orientation. Devices with highly asymmetric properties show nearly identical channel-generated noise yet a significant difference in contact-generated noise levels when the contact orientation is reversed. Fully symmetric devices show higher current levels, lower threshold voltages, and lower contact-generated noise than asymmetric devices with either source or drain gated, but channel-generated noise levels are similar.

Index Terms—Low-frequency noise, metal-semiconductor contact, nanowire MOSFET, Schottky barrier.

I. INTRODUCTION

NANOWIRE transistors have been extensively studied for use in future electronic applications, such as high-speed electronics [1], chemical sensors [2], and transparent flexible devices [3]. The nanowires used in transistors typically are not intentionally doped, although modest doping levels are generally inferred [4], and therefore the electrical characteristics are not dictated by p-n junctions but by electron and hole injection properties from the metal–semiconductor contacts.

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Large variations in mobility and subthreshold swing have been observed in nanowire transistors with the same channel material but different wire diameters or oxide thicknesses and gate geometries [5], likely due to the effects of the contacts. It has also been shown how the on/off ratio and threshold voltage are influenced by the contacts and band alignment between contacts and channel [6]. In undoped nanowire transistors with strong metal–semiconductor contacts, at high drain bias, the device properties are largely determined by the source contact only [7], as any charge carrier that can be injected from the source contact into the channel will eventually make its way to the drain, but drain contact effects can be observed at lower drain voltages.

It is generally assumed that low-resistance ohmic contacts to InAs are straightforward to realize due to Fermi level pinning, yet the experimental results on InAs nanowires consistently exhibit contact effects and series resistance, in part due to ungated access regions [8], [9]. In this paper, we further investigate the role of contacts using InAs nanowire transistors with the gate overlapping both contacts and with the gate overlapping only one contact.

Typically, nanowire transistors are fabricated by depositing a source and drain contact on either end of the wire and a gate contact nominally centered over the wire, leading to a geometrically symmetrical device. This paper considers highly asymmetric devices fabricated by overlapping the gate with only one of the two metal contacts. Due to slight alignment variations, the partially gated devices were fabricated with varying proportions of the source–drain gap covered by the gate, ranging from about 25% to 100% of the nanowire. The current–voltage (I–V) characteristics were measured in each device, then the contacts reversed and the current remeasured in this new orientation. When the gate overlaps the source contact, a much higher current level can be achieved, but when the gate overlaps only the drain contact, the current remains lower because of the stronger source barrier. Low-frequency noise measurements were also made in each orientation to help investigate the symmetry of the devices.

II. FABRICATION AND MEASUREMENTS

Two types of devices were fabricated on the same wafer, both shown in Fig. 1. One type has a top gate that overlaps both source and drain contacts while the other device type has a top gate that only overlaps one of the metal contacts. The devices were fabricated using 30-nm-diameter InAs wires.
grown by a vapor–liquid–solid process, which were removed from their growth substrate by sonication in isopropanol and then dispersed onto silicon wafers with 100-nm SiO$_2$. The wires were located by photography through an optical microscope so that source and drain contacts could be aligned to individual wires using electron-beam lithography and liftoff of nickel, forming channel lengths of 500 nm. Next a 10-nm layer of aluminum oxide was deposited by atomic layer deposition to serve as the gate dielectric. A Ti/Au gate contact was then deposited by electron-beam lithography and liftoff, with gate coverage of devices ranging from the entire 500-nm channel covered to about 25% of the channel covered by the gate electrode.

The $I$–$V$ curves were measured on both types of devices, as shown in Fig. 2. The devices with complete gate overlap [Fig. 2(a)] show comparable current levels when remeasured after interchanging the source and drain contacts. Devices with one-sided overlap [Fig. 2(b)] exhibit asymmetrical $I$–$V$ curves, having much higher current when the gate overlaps the source contact, although still less current than the symmetrical devices. The current ratio $I_{LO}/I_{HI}$ parameter is the ratio of current in drain-gated configuration to that in source-gated configuration at a drain voltage of 1 V and the same gate overdrive voltage, and acts as a measure of symmetry for the device. A current ratio of one corresponds to a fully symmetric device. A sampling of devices on the wafer show differing levels of asymmetry, due to slight variations in gate alignment, up to 10x difference in current levels are observed.

The threshold voltage for each device and each configuration was determined by extrapolating the linear portion of the measured $I_d$–$V_{GS}$ curve at $V_D = 100$ mV to $I_D = 0$. A shift in threshold voltage is observed between gating only the source and gating only the drain, as shown in Fig. 3. Near symmetric devices ($I_{LO}/I_{HI}$ near one) show a little change in threshold voltage between the two orientations, but the threshold voltage of an asymmetric device with the source gated ($V_{TH−SG}$) is up to 0.5 V higher than the threshold the same device with drain gated ($V_{TH−DG}$).

Low-frequency noise was also measured in each device under both orientations at varying gate voltages to determine the role of contacts and channel in noise generation. Noise in the channel of the device can be modeled as

$$A = \frac{S_f f}{I^2} \propto \frac{1}{(V_g - V_t)^p},$$

where $S_f$ is the power spectral density of current noise and $f$ is the frequency [10]. The factor $p$ varies based on the
mechanism of the noise. It is generally assumed that $p = 1$ for mobility fluctuations, and $p = 2$ for number fluctuations. In this paper, the actual mechanism is not significant; however, the ungated region of asymmetric devices, being independent of gate voltage, will have a constant carrier concentration $N$, and therefore constant noise $S_I/I^2$, yet the channel noise contribution will show the gate voltage dependence.

The measured noise spectral power density $S_I$ at 100 Hz and $V_{DS} = 50$ mV is normalized by current squared and the resulting noise amplitude $A$ is plotted in Fig. 4. The symmetric current devices show nearly identical noise levels in each bias direction across all gate voltages. Each bias direction in the asymmetric devices exhibits nearly the same noise level at low gate voltages near and below threshold, but noise splits at higher gate voltages with the source-gated configuration demonstrating lower noise.

III. DISCUSSION

In classical, channel-dominated devices, such as long-channel MOSFETs (MESFETs), the gate voltage forms an inversion (undepleted) layer with some carrier density, and the drain voltage accelerates those carriers through the device. Threshold voltage is defined as the gate voltage at which an inversion (undepleted) layer begins to form. Low-frequency noise in such devices is determined by a Hooge parameter constant and the number of carriers in the channel inversion layer [11].

In nanowire devices, however, the current and noise characteristics are heavily influenced by the source and drain contacts. The source contact of a nanowire transistor is often the main bottleneck of charge transport [12] at high drain bias, and therefore the contacts can play a major role in device operation. For contacts with gate overlap, each contact forms a Schottky barrier with an associated band-bending length

$$\lambda = \sqrt{\frac{\epsilon_{nw}}{\epsilon_{ox}}} d_{nw} d_{ox}$$

(2)
determined by the nanowire and oxide permittivities and diameters [13] ($\epsilon_{nw}$, $\epsilon_{ox}$, $d_{nw}$, and $d_{ox}$, respectively). In these devices, $\lambda \approx 22$ nm under the top gate, much shorter than the minimum gate length, leading to a portion of the channel whose potential is dominated by the gate potential and not significantly influenced by the contact. While InAs typically forms metal contacts, which are pinned near the conduction band, these devices show a small barrier height of 40–80 meV based on independent low-temperature measurements on similar devices [14], and is supported by observation in these devices of the nonlinear behavior at low drain voltages in the asymmetric device. The band diagrams in Fig. 5 show how the overlap and nonoverlap contacts have different band-bending lengths. In the case where the gate overlaps the contact, $\lambda$ is small and thermionic field emission typically dominates. For contacts with a significant gap between gate and contact, $\lambda$ is larger and the bands generally bend much more slowly, therefore thermionic emission dominates. In the devices in this paper, the source and drain contacts of a given device have different band-bending lengths due to the asymmetrical gating of the contacts. Simply calculating a contact resistance from the $I–V$ curves results in contact resistances of about 500 KΩ for nonoverlapping and 35 KΩ for overlapping contacts. For comparison, in another study of InAs nanowires with comparable diameters [15], extrinsic contact resistances above 50 KΩ can be inferred for devices with Ni contacts.

In this discussion, the source always refers to the contact held at zero potential, and the drain refers to the contact at
higher voltage relative to the source, therefore either physical contact to the nanowire can be considered as the source or the drain depending on bias configuration. Symmetric devices, with the gate overlapping both contacts, show comparable current levels in each bias direction, showing symmetric contacts. When an asymmetric device is operated with the drain contact gated, it exhibits much lower current, up to 10 times, compared with the same device when operated with the gated contact as the source, although it is the same wire with the same nominal metal–semiconductor contacts. To understand this behavior, consider the band diagrams in Fig. 5. The shaded gray area shows the gated portion of the device. When the source (left) contact is gated [Fig. 5(a)], the source contact can be made transparent by the gate bias. The drain voltage is the main factor affecting the drain contact transparency, where at low drain bias, a significant barrier exists for carriers to leave the channel, but at higher drain bias, that barrier is collapsed, allowing significant current flow. This drain-dependent behavior can be observed in the \( I-V \) curve in Fig. 2(b) as the nonlinearity of the source-gated curve at low drain bias.

In the opposite direction, when the drain (left) contact is gated [Fig. 5(b)], the drain contact can be made transparent by the gate for any drain voltage so the nonlinearity is reduced. The source (right) contact, however, always remains a thermionic emission barrier for injection into the channel, thus significantly limiting current flow at all gate and drain bias points. In symmetrical devices where the top-gate overlaps both contacts [Fig. 5(c)], the gate can modulate the transparency of both contacts, reducing the nonlinear effects at low drain bias and leading to higher on-current [Fig. 2(b)].

To aid in understanding the measured asymmetry behavior, a simple model for the voltage-dependent behavior of the contacts can be developed. While, in general, the overall device resistance would include components from the channel as well as the contacts, the contact components can be calculated by assuming that the channel is ballistic and that 1-D electrostatics result in strong gate control of the channel potential. In this case, the current through the device depends on the transmission of each contact and can be calculated using the Landauer model [16]

\[
I_{DS} = \frac{4e}{h\pi} \int_{0}^{\infty} T_{S}(E)T_{D}(E)\left[f_{S}(E) - f_{D}(E)\right]dE \tag{3}
\]

where \( T_{S}(E) \) and \( T_{D}(E) \) are the energy-dependent transmission probabilities of the source and drain contacts, and \( f_{S} \) and \( f_{D} \) are the Fermi distributions at each contact. Taking the difference in Fermi distributions will model the current as two components: one injected from the source contact into the channel and the other in the opposite direction from the drain contact into the channel. Considering the band diagrams of Fig. 5, the gated contact will follow an exponential band bending with characteristic length \( \lambda \) determined by (2), with an energy profile at the source of

\[
V(x) = \left(\frac{E_{b}}{q} - \phi_{f}\right)e^{-x/\lambda} + \phi_{f} \tag{4}
\]

and at the drain contact, when covered by the gate

\[
V(x) = \left(\frac{E_{b}}{q} + V_{DS} - \phi_{f}\right)e^{-x/\lambda} + \phi_{f} \tag{5}
\]

with \( E_{b} \) the barrier height and \( \phi_{f} \) the channel potential set by the gate voltage in a region with no contact influence. \( x \) is the distance from the source contact into the channel and \( x' \) is the distance from the drain contact. The transmission probability of the gated contact can be calculated using a Wentzel–Kramer–Brillouin (WKB) approximation for this exponential energy barrier [17]. The contact not covered by the gate will have a much longer \( \lambda \) length making the tunneling component minimal. In this case, only the thermionic emission component over the barrier is considered, with transmission probability of one above the barrier and zero below. The \( I-V \) curves calculated by this model are shown in Fig. 6, calculated for current in both directions. In Fig. 6(a), both contacts are identical, tunneling contacts. In Fig. 6(b), only one contact is gated, first with the source contact tunneling and the drain contact thermionic only, then swapping the contacts so the source contact is thermionic only and the drain contact is tunneling. This model captures the features observed in the measured data of Fig. 2(b), including the relative current levels between the two directions and the nonlinearity at low drain voltages for the source-gated direction. The main discrepancy between the model and measured data is the drain voltage at which current saturation occurs. In the model, saturation begins near the point, which the drain voltage collapses the

![Fig. 6. Output characteristics of (a) symmetric and (b) asymmetric device in both contact directions modeled using WKB approximation for both contacts.](image-url)
drain Schottky barrier, or \( V_{DS} = E_b/q \), around 80 mV in this simulation. However, the model ignores the influence of drain bias on the channel. In the real device, the channel potential \( \phi_f \) near the drain end is also a function of drain voltage, so the drain barrier will not be completely collapsed until a higher drain bias is reached, leading to the saturation at a drain voltage several times higher, as observed in the measured data. Note that saturation still occurs at a drain voltage much lower than \( V_D - V_T \) predicted by channel pinchoff.

Because a given device exhibits two different threshold voltages depending on bias orientation, the threshold voltage in these devices is not determined by channel doping and forming an inversion layer, but by the point at which the contacts begin to allow significant carrier injection into and out of the channel. A shift of up to 0.5 V was observed in the least symmetrical devices. Symmetric devices show negligible change in threshold voltage upon switching contact orientation. In symmetric devices and devices configured with the source end gated, the drain contact becomes relatively transparent at modest drain voltages, and the threshold voltage corresponds to the gate bias point where the source allows significant injection into the channel. When only the drain end is gated, the source barrier remains for all bias points, so threshold is influenced by the reduction of the drain barrier, which is enabled by both gate and drain voltages.

Noise characteristics of the devices can be explained with the noise versus gate voltage plots of Fig. 4. The contacts and channel each contribute to noise with their own effective Hooge parameter and unique gate voltage dependence, thus the dominant noise mechanism at a given bias point can be determined from the slope of the noise versus gate voltage plots [18]. When the contacts are the dominant factor of both current and noise, the log-scale plot of noise \( A \) versus \( V_g \) will be independent of gate voltage, as observed at higher gate bias points. When the channel dominates both current and noise, noise depends on gate voltage with differing slopes depending on the particular noise generation mechanisms and relative contribution of the channel and the contacts. The asymmetric device shows nearly equal noise levels for both directions at low gate voltages (channel-dominated regime) because the channel portion of the device is identical regardless of contact orientation. At high gate voltages (contact-dominated regime), there is a split between noise levels, with the higher current direction showing lower noise due to the effect of gating the source contact. The orientation with a gated source contact shows a contact noise level about 4–5 times lower than with a gated drain contact. When the source is gated, the transmission probability at high gate voltages is much higher, reducing the resistance and the noise generated by the contact. When the source is not gated, transmission remains lower, leaving a higher resistance and noise level. In the symmetric device, noise is nearly the same for both bias directions across all gate voltages, yet the contact noise level is lower than the asymmetric device in either bias direction. The lower resistance contact leads to lower contact-generated noise. A +2 slope can also be observed in the lower current orientation, showing contact/access region dominates noise relative to the channel due to the ungated source barrier, whereas the channel dominates overall source-to-drain resistance [19].

Comparing symmetric with asymmetric devices in Fig. 4, the asymmetric device [Fig. 4(b)] in either bias direction shows higher contact noise levels than the symmetric device [Fig. 4(b)]. This difference is due to the low drain bias (50 mV) used to measure the noise, leaving the ungated contact barrier in place for each bias direction. The higher contact resistance leads to higher contact noise. In the channel-dominated region, the two device types show a little difference in noise levels.

Nanowire transistors are often fabricated and operated without a top gate contact, but with the back substrate used as the gate. A back gate would overlap both contacts and leads to a symmetrical device with no ungated access regions. The associated exponential band bending at the contacts can account for the observation that a simple back gate can often outperform a top gate even when the top gate uses a lower effective oxide thickness [5].

IV. CONCLUSION

It was shown how the metal–semiconductor contacts are important in nanowire transistor current level, threshold, and noise properties. The contacts influence threshold voltage by limiting the injection into or out of the channel, causing the threshold to shift upon changing bias directions. When the source contact, but not the drain contact, is controlled by the gate, the overall device exhibits higher current and lower ON-state noise than the same device with the source ungated, yet shows nonlinear effects at low drain bias. In a symmetric device with the entire nanowire is controlled by the gate, the current levels are higher, threshold voltage is lower, and ON-state noise is lower than an asymmetric device in either bias direction. OFF-state noise is not affected by the contact orientation or asymmetry because it is mostly generated in the nanowire itself, not in the contact regions. Obtaining quality low-resistance contacts is a key to fabricate a high-current and low-noise nanowire device.

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REFERENCES


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