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Reliability of High-Mobility InGaAs Channel n-MOSFETs Under BTI Stress

Ming-Fu Li, Guangfan Jiao, Yaodong Hu, Yi Xuan, *Member, IEEE*, Daming Huang, and Peide D. Ye, *Fellow, IEEE*

(Invited Paper)

***Abstract*—The reliability performance of $In_xGa_{1-x}As$ n-MOSFETs with Al_2O_3 gate dielectric under positive-bias temperature instability stress is investigated. The following new phenomena are demonstrated: 1) There are high densities of fast interface traps $N_{\rm it}$ and slow oxide border traps $N_{\rm SOX}$ near the interface between InGaAs and Al_2O_3. The border traps are more fragile under stress, and therefore, the stress mainly induces border traps. 2) The stress-induced border traps consist of permanent acceptor traps and recoverable donor traps. Acceptor trap energy density $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$ is mainly distributed above the conduction band edge E_c of InGaAs with a tail extending to the midgap, whereas donor trap energy density $\Delta D_{\rm SOX}^{\rm Donor}(E)$ has a large distribution inside the InGaAs energy gap with a tail extending to the conduction band. 3) Flicker noise variation after stress and its correlation to the acceptor and donor trap generation and recovery are demonstrated. 4) The recoverable donor traps induce the subthreshold slope and off-current degradation in the stress phase and recover in the recovery phase and also induce continuous degradation of on-current in the recovery phase. The permanent acceptor traps induce the transconductance and on-current degradation. The long-term device lifetime is mainly determined by the generation rate of the acceptor traps. 5) Comprehensive comparison between the Si and InGaAs MOSFETs' degradation behaviors under bias temperature instability stress is presented. The physical recovery of donor oxide traps in dielectric in InGaAs/Al_2O_3 has never been observed in a Si MOS structure, deserving special attention and further investigation.**

***Index Terms*—Bias temperature instability (BTI), border traps, InGaAs, n-MOSFETs, reliability.**

I. INTRODUCTION

InGaAs is a promising candidate among various high mobility channel materials for future n-MOSFETs for low voltage low power applications [1]–[11]. In this paper, we would summarize and elaborate our recent investigations [12], [13] regarding the impact of interface traps and border traps in the InGaAs/Al_2O_3 interface to the reliability performance of the n-MOSFETs under the positive-bias temperature instability (PBTI) stress.

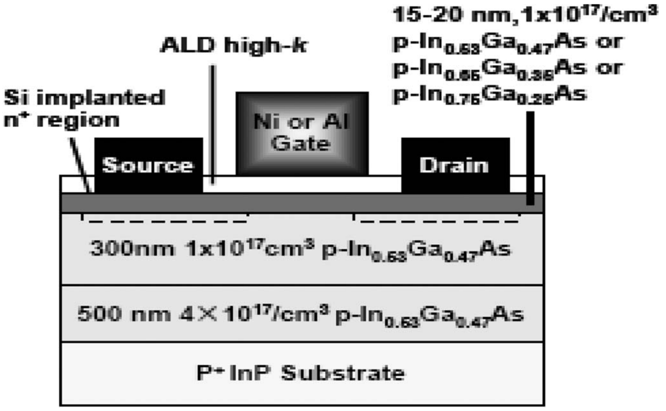
15-20 nm,1x10^{17}/cm^3
p-In$_{0.53}$Ga$_{0.47}$As or
p-In$_{0.65}$Ga$_{0.35}$As or
p-In$_{0.75}$Ga$_{0.25}$As
ALD high-*k*
Si implanted
n$^+$ region
Ni or Al
Gate
Source
Drain
300nm 1x10^{17}cm^3 p-In$_{0.53}$Ga$_{0.47}$As
500 nm 4× 10^{17}/cm^3 p-In$_{0.53}$Ga$_{0.47}$As
P+ InP Substrate

Fig. 1. The structure of the planar inversion mode $In_xGa_{1-x}As$ n-MOSFET with ALD Al_2O_3 gate dielectric [3].

$In_xGa_{1-x}As$ n-MOSFETs with $x = 0.53$ and 0.65 are used with the device structure shown in Fig. 1. The fabrication processes of these devices were illustrated in [3]. The FETs have channel width 100 μm and channel length 2–40 μm, ALD grown Al_2O_3 gate dielectric with physical thickness of 8 nm, and Ni/Au metal gate. P-type channel doping is about 1–2 $\times$ 10^{17} cm^{-3}.

DC current-voltage (I_s–V_g), charge pumping (CP), fast pulsed I–V measurement (FPM), and flicker $(1/f)$ noise measurements are carried out to characterize the degradation of n-MOSFETs under PBTI stress. Agilent 4156C parameter analyzer, pulse generator 81110A, and Cascade probe station are used for DC I_s–V_g and CP measurements. In the I_s–V_g measurements, V_d is set to 50 mV, while source and substrate are grounded. I_s rather than I_d is measured to avoid the drain-substrate junction reverse biased leakage interference. In the CP measurements [14], the source, drain, and substrate are all grounded. The CP currents $I_{\rm cp}$ are measured from the source/drain $(I_{\rm s/d})$ and from the substrate $(I_{\rm sub})$ with the similar results, indicating that the geometric component [14] due to electron-hole recombination in the channel is small and can be ignored. Comparing with $I_{\rm sub}$, $I_{\rm s/d}$ has smaller noise and therefore is used to characterize $I_{\rm CP}$. During the PBTI stress phase, gate stress voltage $V_g = 3.0$ V, while $V_s = V_d = V_b = 0$ V.

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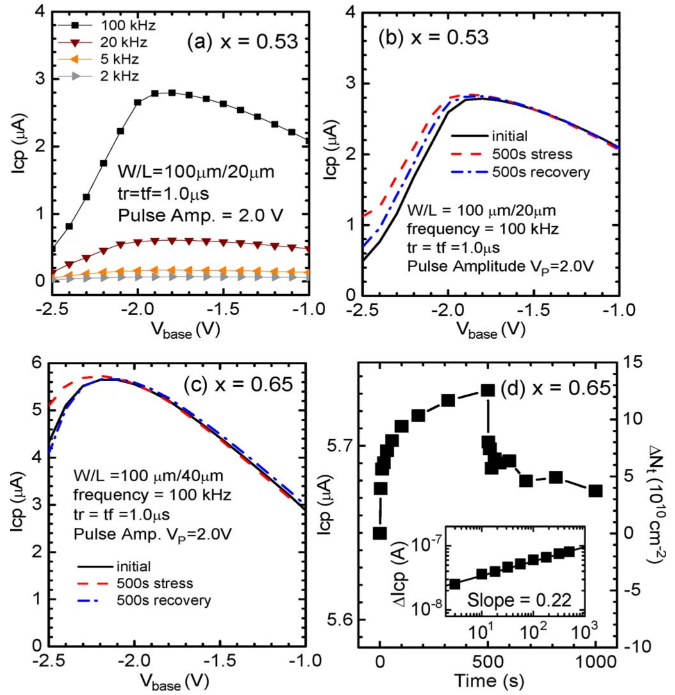


Fig. 2. (a) CP current $I_{\rm cp}$ for the $\rm In_{0.53}Ga_{0.47}As$ n-MOSFET fresh device measured at different frequencies. When $V_{\rm base}$ scans to -1.85 V, the bottom level of CP pulse is at -1.85 V and the FET is under accumulation, while the top level of CP pulse is at $+0.15$ V (CP pulse amplitude 2 V), exceeding the $V_{\rm th} = +0.1$ V and the FET is under inversion. The CP current has a peak accordingly; (b) same FET measured by $f = 100$ kHz at the different states; (c) same as (b), however for $\rm In_{0.65}Ga_{0.35}As$ FET. The interface trap area density is estimated by $N_t = I_{\rm cp}/(fqA_G)$, A_G is the gate area. From the $I_{\rm CP}$ peak of the fresh device, $N_t^0 \approx 9 \times 10^{12}$ cm^{-2}. (d) The time evolution of $I_{\rm cp}$ (left coordinate) and ΔN_t (right coordinate) in the stress phase (0–500 s) and recovery phase (500–1000 s). Inset: The time evolution of $\Delta I_{\rm cp}$ in the stress phase plotted in log scale.

During the recovery phase, all the electrodes are grounded. The flicker noise measurements are conducted by SR570 low noise amplifier and Agilent 35670A spectrum analyzer. All measurements are taken at room temperature.

For the fresh transistors used in this work, the threshold voltage $V_{\rm th}$ is in the range of $+(0.1 \sim 0.2)$ V for the $x = 0.53$ FETs and $-(0.1 \sim 0.2)$ V for $x = 0.65$ FETs. The sub-threshold swing SS is around 130 mV/decade for $x = 0.53$ FETs and 160 mV/decade for $x = 0.65$ FETs. Other electrical performance information can be found in [3].

In this paper, we mainly focus on the new phenomena under BTI stress in the InGaAs n-MOSFETs and compare to the traditional Si MOSFETs with SiON or high-k gate dielectric [15]–[21].

II. TRAPS GENERATION UNDER BTI STRESS–FAST INTERFACE TRAPS OR SLOW OXIDE BORDER TRAPS?

Fig. 2 shows the charge pumping (CP) spectra for the $\rm In_xGa_{1-x}As$ n-MOSFET during the PBTI stress phase and the following recovery phase, indicating generation of interface traps ΔN_t in the stress phase and partial recovery in the recovery phase. Fig. 2(d) shows the time evolution of the CP currents $I_{\rm cp}$ and the areal density of the stress induced interface traps ΔN_t. From the $I_{\rm cp}$ of the fresh device, the process induced interface trap density N_t^0 is derived to be about 9×10^{12} cm^{-2}, very high comparing to 10^{10} cm^{-2} for a good quality Si MOSFETs. The stress-induced interface trap density $\Delta N_t = N_t - N_t^0$ is only about 1.3×10^{11} cm^{-2} after 500 s stress. The inset of Fig. 2(d) illustrates that the time evolution of ΔN_t in the stress phase shows a power law $\Delta N_t \infty t^n$ with index $n = 0.22$, close to the index n of Si/SiON p-MOSFET under negative BTI (NBTI) stress with similar CP measurement at room temperature [18]. On the other hand, N_t decreases in the recovery phase.

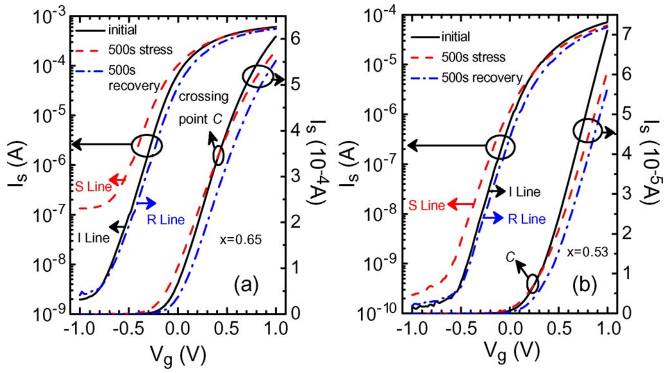


Fig. 3. I_s–V_g curves for the fresh $\rm In_xGa_{1-x}As$ n-MOSFET (solid lines, denoted by I lines), after 500 s PBTI stress ($V_g = 3.0$ V) (dashed lines, denoted by S lines), and then after 500 s recovery ($V_g = 0$ V) (dashed-dot lines, denoted by R lines). $V_d = 50$ mV. (a) $x = 0.65$, $W/L = 100$ μm/4 μm. (b) $x = 0.53$, $W/L = 100$ μm/8 μm. Comparing S lines with I lines, the V_g shift ΔV_g at constant current I_s is negative in the sub-threshold region and is positive at high I_s in the on-current region. A crossing point C is defined at $\Delta V_g = 0$.

Fig. 3 shows the DC I_s–V_g curves measured for the fresh device before stress (initial state, I lines), after 500 s PBTI stress (S lines), and with additional 500 s recovery (R lines) for $x = 0.65$ and 0.53 devices respectively.

Notice that by $f = 100$ kHz CP measurements showed in Fig. 2, the stress induced interface trap area density ΔN_t is only 1.3×10^{11} cm^{-2}, comparing with the process induced interface trap area density $N_t^0 (\approx 9 \times 10^{12}$ cm$^{-2})$ of the fresh device. However by I_s–V_g measurements showed in Fig. 3, ΔN_t is very large, $> 10^{12}$ cm^{-2} estimated by the gate voltage shift ΔV_g in the sub-threshold (SS) region by $\Delta N_{\rm t} = (C_{\rm OX}/q)\Delta V_g$, ($C_{\rm OX}$ is the gate oxide capacitance) [22], as explained in more details in Section IV. To resolve this issue, two additional experiments have been conducted.

Fig. 4 shows the frequency (f) dependence of N_t^0 and ΔN_t estimated by CP experiments. The f dependent CP results indicate that CP detected N_t has two trap components. The conventional fast interface trap component $N_{\rm it}$ which has f independent CP current component in the measured frequency range. The near interface slow oxide border trap component $N_{\rm SOX}$, which has CP current decreasing with increasing f [23], [24], since when increasing f, the exchange of electrons between the slow border traps and the channel can not follow the rapid change of surface potential under CP measurement. The measured CP data in Fig. 4 shows that when f is decreased from 100 kHz to 1 kHz, the process induced N_t^0 increases slightly while the stress induced ΔN_t increases more significantly. This indicates that the process induced N_t^0 mainly includes the conventional fast interface traps $N_{\rm it}$, while the stress induced ΔN_t mainly consists of the slow oxide border

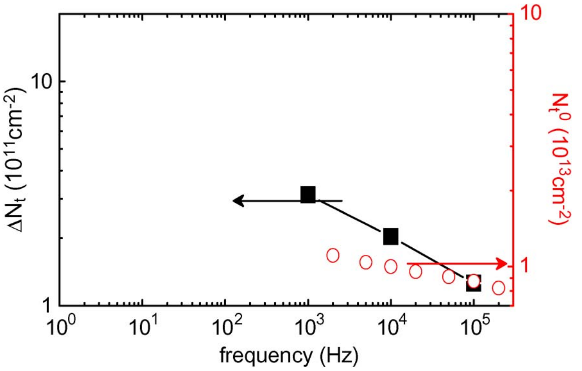


Fig. 4. Frequency dependence of N_t^0 (open circle symbols, scaled by the right coordinate) and ΔN_t (solid square symbols, scaled by the left coordinate) estimated from CP experiments with the CP pulse with the constant rising and falling rates $dV/dt = 2$ V/μs. N_t^0 or ΔN_t is estimated by $I_{\mathrm{cp}}/(fqA_G)$.

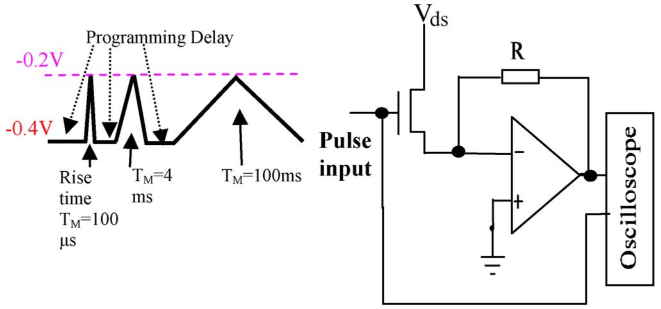


Fig. 5. Left: The pulse waveform for the FPM measurement. Each measurement procedure consists of three sequential pulses with $T_M = 100$ μs, 4 ms and 100 ms respectively. The pulse is used to input to the circuit shown in the right side in Fig. 5 [12], [26].

traps ΔN_{SOX}. The later is seriously underestimated by CP measurements. In other words, the border traps N_{SOX} are more fragile under stress than the conventional fast interface traps N_{it}. By extrapolating the data in Fig. 4 to frequency of 1 Hz, the magnitude of ΔN_t could exceed 10^{12} cm^{-2}, in consistent with the results estimated by the DC I_s–V_g measurements in the similar time zone of measurements. Using the method in [23], the volume density of the stress induced border traps is estimated to be $\sim 5 \times 10^{18}$ cm^{-3}.

The second additional experiment to support this argument is to use the fast pulsed I_s–V_g measurement (FPM) we have developed [25], [26], however extend to the SS region with lower detected current level and more challenging, as shown in Fig. 5. Three I_s–V_g curves are measured by FPM in sequence using different measurement times T_M in 10^{-1}–10^{-4} s time zone. Reducing T_M should reduce the sub-threshold slope (S) degradation if the slow border traps ΔN_{SOX} can not follow the fast surface potential change in the FPM measurement. This is demonstrated in Figs. 6–8. Combining Fig. 4 and Fig. 7 gives very strong support of domination of slow oxide border traps ΔN_{SOX} in the stress induced traps ΔN_t.

III. DONOR OR ACCEPTOR TRAPS? A UNIFIED BORDER TRAP MODEL

In the Fig. 3, by comparing the I and S lines, ΔV_g extracted at low I_s (SS region) is negative after stress, accompanied by

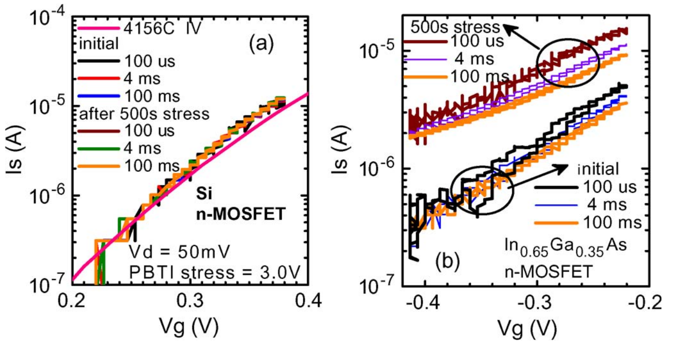


Fig. 6. I_s–V_g curves in the sub-threshold region measured by the FPM method. (a) For Si n-MOSFET all curves measured by different T_M coincide completely, implying no error introduced by the FPM method. Small deviation from the curve measured by Agilent 4156C is due to scaling difference between 4156C and the amplifier used in FPM. (b) For fresh (initial) In$_{0.65}$Ga$_{0.35}$As n-MOSFET and after 500 s PBTI stress. The curves measured by faster T_M has smaller sub-threshold swing S and larger $\Delta \mathrm{V_g}$, indicating existence of slow donor oxide traps.

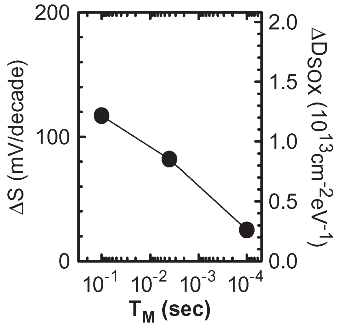


Fig. 7. Degradation of sub-threshold swing ΔS after 500 s PBTI stress (left coordinate), extracted from the data in Fig. 6(b). The generated slow oxide trap energy density $\Delta D_{\mathrm{SOX}} = [C_{\mathrm{OX}}/(qkT \ln 10)]\Delta S$ [22] is also plotted (right coordinate). ΔD_{SOX} is seriously underestimated when T_M is reduced, indicating domination of slow donor oxide traps.

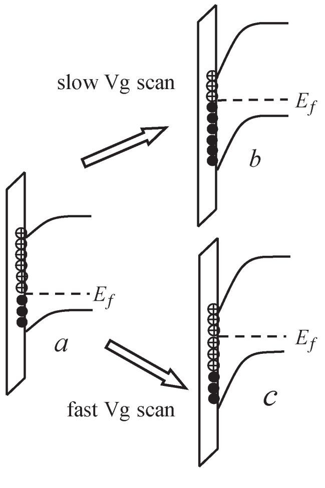


Fig. 8. Surface potential band diagrams of In$_{0.65}$Ga$_{0.35}$As n-MOSFET used to explain the results of Fig. 6(b) and Fig. 7. (a) Surface potential for $V_g = -0.4$ V, (b) Surface potential for $V_g = -0.2$ V by slow V_g scan from -0.4 V. Slow donor traps can response to capture electrons from the channel to reduce the positive charge, causing smaller ΔV_g and larger ΔS. (c) Same as (b) however for fast scan of V_g, slow donor traps can not response, no change of positive charge, causing larger ΔV_g and smaller ΔS.

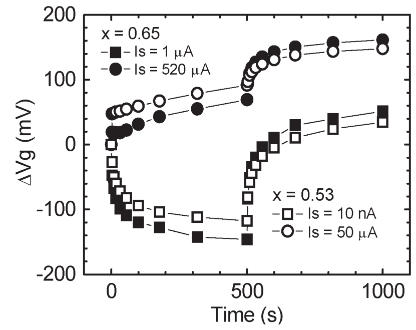


Fig. 9. Time evolution of ΔV_g in the SS region and in the on-current region in stress (0–500 s) and recovery (500–1000 s) phases, extracted from DC I_s–V_g curves shown in Fig. 3. Note the strange phenomena that (1) ΔV_g in the on-current region continuously degrade (increases) in the recovery phase, (2) ΔV_g in the SS region turns to positive at the end of the recovery phase.

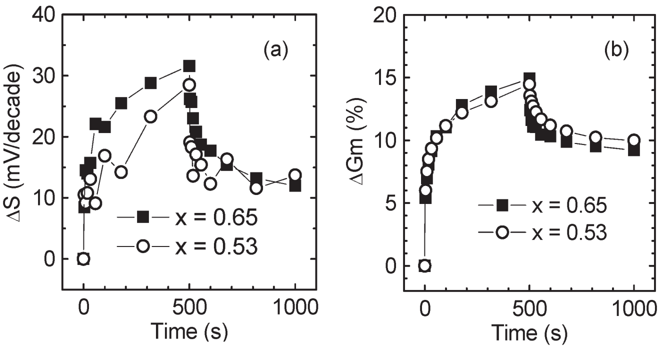


Fig. 10. Time evolution of (a) the ΔS extracted at $I_s = 5.0\ \mu$A for $x = 0.65$ device and extracted at $I_s = 10$ nA for $x = 0.53$ device. (b) Time evolution of the degradation in peak transconductance.

a degradation in sub-threshold swing S. The time evolutions of ΔV_g and ΔS are shown in Figs. 9 and 10(a). ΔV_g extracted at high I_s ("on-current" region) is positive after stress, accompanied by a degradation in transconductance G_m, as shown in Figs. 3, 9, and 10(b). There is a crossing point between the I and S lines in Fig. 3, denoted by C at which $\Delta V_g = 0$. On the other hand, by comparing the I and R lines in Fig. 3, ΔV_g extracted at low I_s in the SS region is positive, with a degradation in S, as also shown in Figs. 9 and 10(a) at $t = 1000$ s. The most strange thing is that, at high I_s, ΔV_g further degrade (increase) when the stress is released in the recovery phase as shown in Fig. 3 S and R lines, and in Fig. 9, and it saturates gradually towards a constant.

Interestingly, these results are totally different from the BTI degradation in the Si MOSFETs. For Si MOSFET with SiON gate dielectric, BTI stress induces dominant donor interface traps [27], [28], and very small amount of acceptor interface traps [29]. When using DC current measurement, the donor interface traps induce negative V_g shift in the p-MOSFET under negative BTI stress [18], [19], [27]. The small amount of acceptor interface traps induce very small positive V_g shift in the n-MOSFET under PBTI stress [29] while donor interface traps keep neutral under inversion surface. For Si n-MOSFET with high-k gate dielectric HfO_2, I_s–V_g curve sustains positive shift in the PBTI stress phase and partially recover in the recovery phase [25]. The shift of I–V curve is due to trapping and de-trapping of the process induced pre-existing traps in the dielectric [25], [30]–[32].

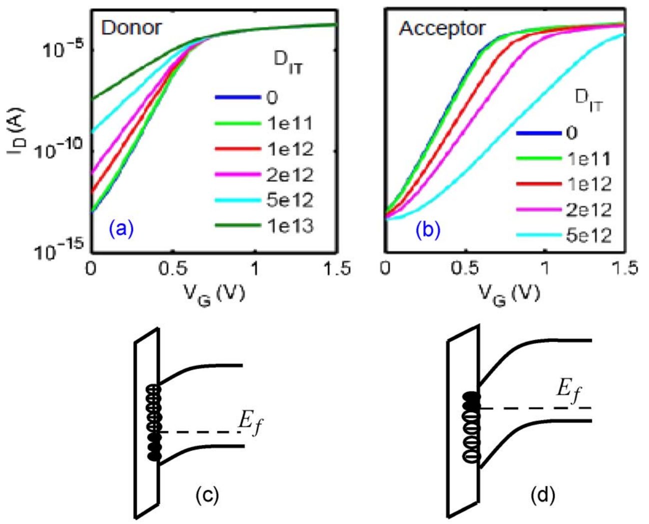
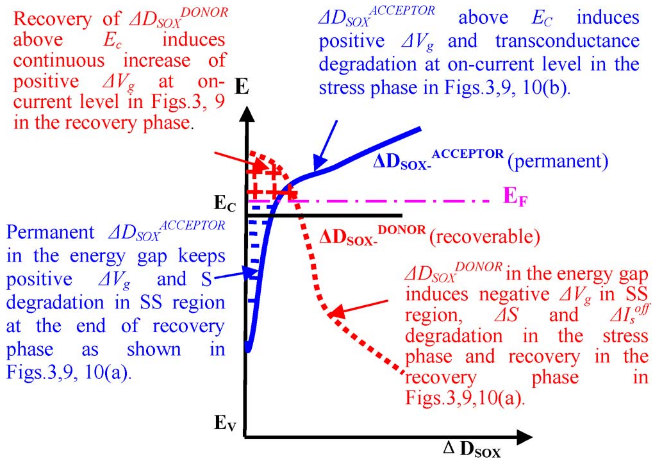


Fig. 11. (a) Donor traps at the interface induce negative V_g shift of the I–V curves, larger shift with lower I_s current level. (b) Acceptor traps at the interface induce positive shift of the I–V curves, larger shift with higher I_s current level (courtesy of M. A. Alam [33]). This can be understood by the MOS band diagrams in (c) (d). Higher I_s level corresponds to stronger inversion with deeper band bending, inducing lower positive interface charge area density for donor traps (c), causing smaller V_g shift as shown in (a); or higher negative interface charge area density for acceptor traps (d), casing larger V_g shift as shown in (b). Both acceptor and donor traps give rise degradation of S.

To interpret the experimental results in Figs. 3, 9 and 10, the following picture in Fig. 11 to distinguish the donor or acceptor traps is useful [33]. Comparing I and S lines in Fig. 3 and Fig. 11, it is clear that the stress induces donor border traps in the stress phase, responsible for the negative ΔV_g and the degradation of S in the SS region in Fig. 3. The stress also induces acceptor interface traps or the fixed charge, responsible for the positive ΔV_g in the high I_s region and the degradation of transconductance G_m as shown in Figs. 3, 9, and 10(b).

Comparing the R lines with I lines in Fig. 3 in the SS region, there are two possible cases to interpret the lines after the recovery phase. (1) There are recoverable donor traps and permanent acceptor traps. At the end of recoverable phase, donor traps are recovered and only acceptor traps exist, which can explain the positive ΔV_g and the S degradation [see the difference between the I and R lines in Fig. 3 and compare it with Fig. 11(b)]. (2) There are recoverable donor traps and fixed negative oxide charge. In the case (2), the R lines in Fig. 3 are the combined effect of the fixed negative oxide charge and the residual donor traps. The fixed negative charge induces parallel positive shift in the I_s–V_g curve. The residual donor traps at the end of the recoverable phase induce the degradation of S and the negative ΔV_g. If it is the case (2), the residual donor traps must have high enough density to compensate the positive shift induced by the fixed negative charge. As a result, the net ΔV_g is close to zero only when I_s is very low (4×10^{-9} A for $x = 0.65$ devices and 3×10^{-10} A for $x = 0.53$ devices), as shown in Fig. 3. The case (2) should be ruled out because the recovered off-current I_s^{off} (discussed in Section V, Fig. 15) reveals that the stress induced donor traps almost completely


E
E_C
E_F
E_V
$\Delta D_{SOX\text{-}}^{ACCEPTOR}$ (permanent)
$\Delta D_{SOX\text{-}}^{DONOR}$ (recoverable)
ΔD_{SOX}

Recovery of ΔD_{SOX}^{DONOR} above E_c induces continuous increase of positive ΔV_g at on-current level in Figs.3, 9 in the recovery phase.

$\Delta D_{SOX}^{ACCEPTOR}$ above E_C induces positive ΔV_g and transconductance degradation at on-current level in the stress phase in Figs.3,9, 10(b).

Permanent $\Delta D_{SOX}^{ACCEPTOR}$ in the energy gap keeps positive ΔV_g and S degradation in SS region at the end of recovery phase as shown in Figs.3,9, 10(a).

ΔD_{SOX}^{DONOR} in the energy gap induces negative ΔV_g in SS region, ΔS and ΔI_s^{off} degradation in the stress phase and recovery in the recovery phase in Figs.3,9,10(a).

Fig. 12. Stress induced oxide border trap density $\Delta D_{\text{SOX}}(E)$ which consists of permanent acceptor traps $\Delta D_{\text{SOX}}^{\text{Acceptor}}$ (solid line) and recoverable donor traps $\Delta D_{\text{SOX}}^{\text{Donor}}$ (dashed line). During the I_s–V_g measurement, when E_F is moved to a level that the positive donor trap charge is equal to the negative acceptor trap charge, corresponding to the crossing point C at which $\Delta V_g = 0$ in Fig. 3.

recovered in the end of the recovery phase. These results are in conflict with the case (2), but in supporting the case (1).

By the above arguments, a unified border trap model can be established to explain perfectly every details of all experimental results. As explained in Fig. 12, the stress induces slow border traps with density ΔN_{SOX} include recoverable donor traps with energy density $\Delta D_{\text{SOX}}^{\text{Donor}}(E)$ and permanent acceptor traps with energy density $\Delta D_{\text{SOX}}^{\text{Acceptor}}(E)$. The recoverable $\Delta D_{\text{SOX}}^{\text{Donor}}(E)$ traps is not only distributed within the InGaAs energy gap but also extended to the conduction band. The donor traps within the energy gap induce the negative ΔV_g and the S degradation in the stress phase and the recovery in the SS region during the recovery phase [Figs. 3, 9, and 10(a)]. The donor traps in the conduction band induce the strange phenomena of continuous increase of positive ΔV_g in the recovery phase (Figs. 3 and 9). On the other hand, the permanent acceptor traps energy density $\Delta D_{\text{SOX}}^{\text{Acceptor}}(E)$ is mainly distributed in the conduction band with a tail extending to the energy gap. The acceptor traps in the conduction band induce the positive ΔV_g and the degradation in G_m in the high I_s region in the stress phase [Figs. 3, 9, and 10(b)]. The acceptor traps in the energy gap result in the positive ΔV_g and the small S degradation in the SS region at the end of recovery phase [Figs. 3, 9, and 10(a)]. Finally, all the border traps are seriously underestimated by the CP measurements when they cannot follow the fast change of the surface potential during the CP measurements.

It should be emphasized that the properties of the oxide border traps in the InGaAs/Al$_2$O$_3$ is totally different from the oxide traps in SiON or high-k dielectrics in the Si MOSFETs. In Si MOSFETs, many works demonstrated that the oxide traps are mainly pre-existing traps during transistor fabrication process in the gate dielectric of SiON [26], [34] or high-k [25], [30]–[32]. The degradation and recovery reflected in the I–V curves are mainly trapping and de-trapping of electrons (or holes) in the pre-existing traps in the stress phase and recovery phase. However in the InGaAs/Al$_2$O$_3$ case, the oxide traps are generated in the stress phase. The trapping and de-trapping are reflected in the degradation of S, the transconductance, and the off current (as shown in Section V) in the I–V curves. Particularly, donor oxide traps physically recover in the recovery phase. This is very unique and has never been observed by the Si MOSFETs community so far. The origin and physical mechanism of generation and recovery of donor oxide border traps in the InGaAs/Al$_2$O$_3$ interface deserve special attention and investigation in the future.

IV. EXTRACTIONS OF BORDER TRAP ENERGY DENSITIES FROM EXPERIMENTS

We can use the I_s–V_g curves in Fig. 3 to extract the energy distribution of stress induced border traps based on the following assumptions for the trap model described in Section III. (1) At the end of 500 s stress, there are both stress induced donor traps and acceptor traps in the devices. (2) At the end of 500 s recovery, the stress induced donor traps fully recover (see Section V, Fig. 15) while the acceptor traps are permanent. The extraction procedure is as follows.

The first step: ΔV_g is extracted from the I (initial) and R (after 500 s recovery) lines as a function of I_s for all the current range shown in Fig. 3. The result is denoted by $\Delta V_g^{IR}(I_s)$. Since only the acceptor traps remain after 500 s recovery, the density $\Delta N^{-\text{Acceptor}}_{\text{SOX}}(I_s)$ of negatively charged acceptor traps as a function of I_s can be obtained by [22]

$$\Delta N^{-\text{Acceptor}}_{\text{SOX}}(I_s) = (C_{\text{ox}}/q)\Delta V_g^{IR}(I_s) \tag{1}$$

where C_{OX} is the gate oxide capacitance per unit area and is 10^{-6} F/cm^2 estimated by 8 nm Al$_2$O$_3$ gate dielectric. On the other hand, the density difference of negatively charged acceptor traps and positively charged donor traps, $\Delta N^{-\text{Acceptor}}_{\text{SOX}}(I_s) - \Delta N^{+\text{Donor}}_{\text{SOX}}(I_s)$, can be extracted from the I and S (after 500 s stress) lines, shown in Fig. 3, by

$$\Delta N^{-\text{Acceptor}}_{\text{SOX}}(I_s) - \Delta N^{+\text{Donor}}_{\text{SOX}}(I_s) = (C_{\text{ox}}/q)\Delta V_g^{\text{IS}}(I_s) \tag{2}$$

where $\Delta V_g^{\text{IS}}(I_s)$ is the V_g difference between the S and I lines at the same I_s. From (1) and (2), the density of positively charged donor traps can be obtained from

$$\Delta N^{+\text{Donor}}_{\text{SOX}}(I_s) = (C_{\text{ox}}/q)\Delta V_g^{IR}(I_s) - (C_{\text{ox}}/q)\Delta V_g^{IS}(I_s). \tag{3}$$

The second step: the surface potential ψ_s and the energy difference $E = E_F - E_V$ at the interface as a function of I_s can be calculated by SILVACO Atlas simulation tool for In$_x$Ga$_{1-x}$As n-MOSFETs. The device structures for simulations are the same as real devices shown in Fig. 1. From these simulations, the relationship between I_s and the corresponding $E(I_s)$ are obtained. Combining (1), (3), and $E(I_s)$, we obtain $\Delta N^{+\text{Donor}}_{\text{SOX}}(E)$ and $\Delta N^{-\text{Acceptor}}_{\text{SOX}}(E)$ as functions of energy E as shown in Fig. 13.

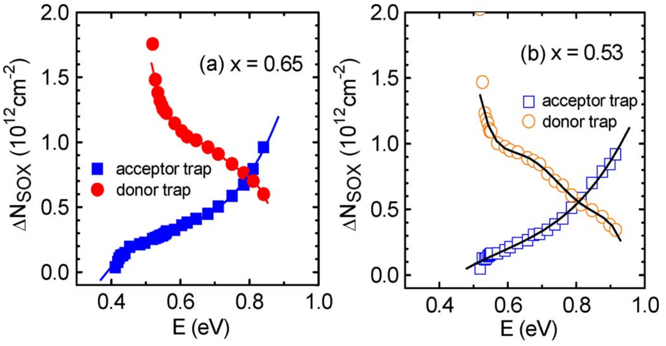


Fig. 13. The charged donor and acceptor border trap area densities as a function of $E = E_F - E_V$ extracted from ΔV_g. The solid lines are least square fits by polynomials.

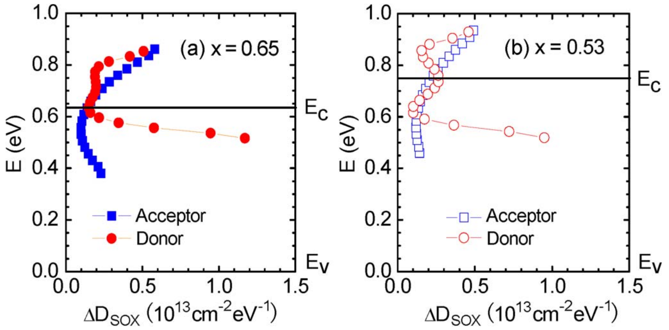


Fig. 14. The donor and acceptor trap energy densities extracted from (4) and (5) for (a) $\mathrm{In}_{0.65}\mathrm{Ga}_{0.35}\mathrm{As}$ and (b) $\mathrm{In}_{0.53}\mathrm{Ga}_{0.47}\mathrm{As}$ n-MOSFETs.

The energy distribution of donor and acceptor traps can be obtained from

$$\Delta D_{\mathrm{SOX}}^{\mathrm{Donor}}(E) = -\frac{d\Delta N^{+}{}_{\mathrm{SOX}}^{\mathrm{Donor}}}{dE} \tag{4}$$

$$\Delta D_{\mathrm{SOX}}^{\mathrm{Acceptor}}(E) = \frac{d\Delta N^{-}{}_{\mathrm{SOX}}^{\mathrm{Acceptor}}}{dE}. \tag{5}$$

The results of (4) and (5) are plotted in Fig. 14.

There are two possible error sources in obtaining the donor and acceptor trap densities using the above derivations. (1) The mobility degradation induced ΔV_g in the strong inversion region [27] has been overlooked. Therefore both the donor and acceptor trap densities may be overestimated, giving rise to distortions of the curves in the horizontal direction in Fig. 14 in the conduction band region. (2) The Atlas simulator for III-V MOSFETs simulation is not matured, and may introduce some error in $E(I_s)$ relation, giving rise to distortions of the curves in the vertical direction in Fig. 14. In spite of these distortions, the overall energy distributions of donor and acceptor traps demonstrated in Fig. 14 can explain all the experimental results. The stress induced donor traps have a large density in the energy gap and their distribution extends to the conduction band. The stress induced permanent acceptor traps are mainly distributed in the conduction band, with a tail extending to the mid-gap.

We can also extract the energy distributions of stress induced acceptor and donor traps from the ΔS in the SS region with the results in consistent with the results in Fig. 14. The details are described in [13].

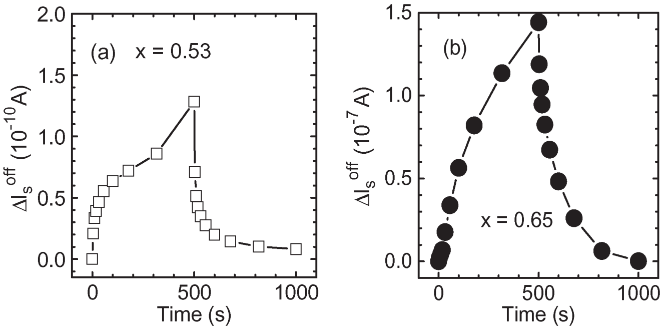


Fig. 15. Time evolutions of the $\Delta I_s^{\mathrm{off}}$ at constant gate voltage $V_g = -0.8$ V in the stress (0–500 s) and recovery (500–1000 s) phases.

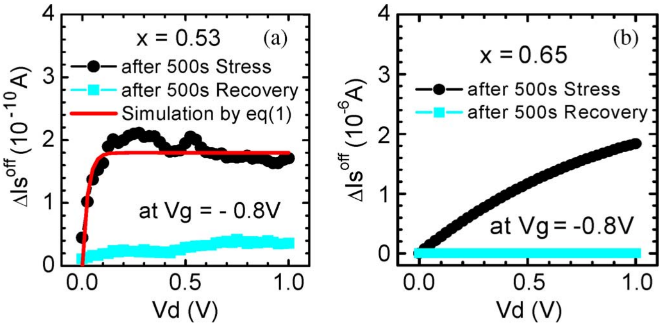


Fig. 16. (a) $\Delta I_s^{\mathrm{off}}$–$V_d$ curves after 500 s PBTI stress and 500 s recovery for the $x = 0.53$ n-MOSFET. The curve after stress satisfies (6), implying that $\Delta I_s^{\mathrm{off}}$ under stress is due to generation of large amount of donor traps, causing change of surface potential pinning, (b) Same as (a) but for $x = 0.65$ FET. $\Delta I_s^{\mathrm{off}}$–$V_d$ after 500 s PBTI stress does not satisfy equation (6).

V. OFF-CURRENT DEGRADATION

In this section, we focus on the degradation under BTI stress and recovery in the recovery phase of the off-current in the range of $V_g = -0.8$ V to 1.0 V in Fig. 3, denoted by I_s^{off}. Fig. 15 shows the time evolutions of the change of $I_s^{\mathrm{off}}\,(\Delta I_s^{\mathrm{off}})$ at a constant gate voltage $V_g = -0.8$ V in the stress and recovery phases. $\Delta I_s^{\mathrm{off}}$ increases with time in the stress phase and almost completely recovers in the recovery phase, implying that $\Delta I_s^{\mathrm{off}}$ is related to the recoverable donor traps as discussed in Section III.

As shown in Figs. 3 and 15, both I_s^{off} and $\Delta I_s^{\mathrm{off}}$ show large quantitative difference between $x = 0.53$ and 0.65 devices. For $x = 0.53$ device, the I_s^{off} is in the range of 10^{-10} A for the fresh device, and increases by a factor of 2 ∼ 3 after 500 s stress. For $x = 0.65$ device, the I_s^{off} is in the range of 10^{-9} A for the fresh device, and increases by two orders of magnitude after 500 s stress. In order to clarify this issue, the $\Delta I_s^{\mathrm{off}}$–$V_d$ curves measured after 500 s stress and 500 s recovery were conducted. If $\Delta I_s^{\mathrm{off}}$ is due to the change of surface potential pinning [35], [36], $\Delta I_s^{\mathrm{off}}$ should be the diffusion current of minority carriers in the SS region satisfying the following equation [22]:

$$\Delta I_s^{\mathrm{off}} = A\left[1 - \exp(-qV_d/kT)\right] \tag{6}$$

which saturates when $V_d > 3kT/q \approx 0.1$ V. As shown in Fig. 16(a), for $x = 0.53$, $\Delta I_s^{\mathrm{off}}$ measured after 500 s stress satisfies equation (6). It implies that the degradation (recovery) of $\Delta I_s^{\mathrm{off}}$ is due to the generation (recovery) of very large density

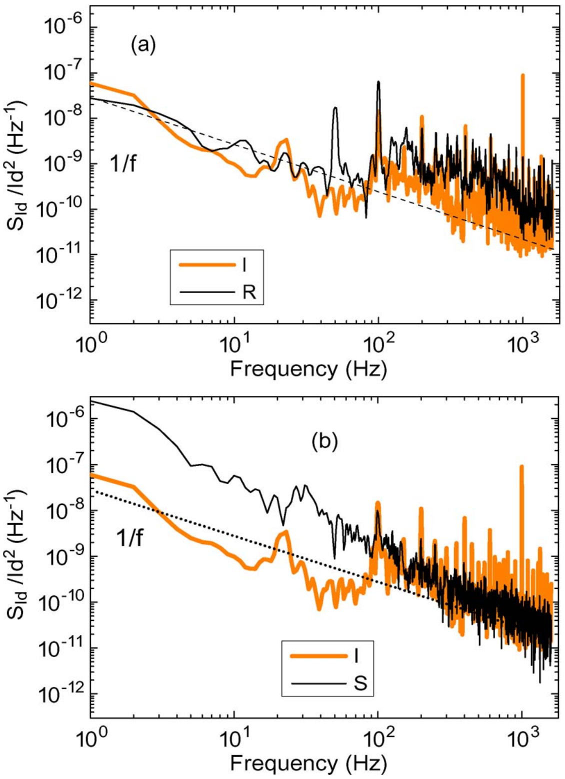


Fig. 17. The normalized flicker noise power spectral densities $S(f)/I_d^2$ of $In_{0.53}Ga_{0.47}As/Al_2O_3$ n-MOSFET, measured at $V_g - V_{\rm th} = 0.1$ V, $V_d = 0.1$ V. (a) comparison of I spectrum for the fresh device with R spectrum after 500 s PBTI stress ($V_g = 3$ V) and subsequently after 2000 s recovery phase ($V_g = 0$ V). (b) comparison of I spectrum with S spectrum measured right after 500 s PBTI stress. The additional peaks at the frequencies of $n \times 50$ Hz (n is integer) are due to 50 Hz city electric power interference and should be ignored.

of donor traps in the energy gap as shown in Figs. 12 and 14, causing the change of surface potential pinning. However, as shown in Fig. 16(b) for $x = 0.65$ device, $\Delta I_s^{\rm off}$ measured after 500 s stress does not satisfy equation (6). In that case, $\Delta I_s^{\rm off}$ is likely due to the drift of electrons in a new surface conduction path across the source and drain, generated by high areal density of donor traps under stress, and therefore the $I_s^{\rm off}$–V_d has a quasi- ohmic relationship. This surface conduction path could be due to the hopping conduction [37] between the neighboring donor traps induced by the stress.

VI. FLICKER NOISE CHARACTERIZATION

The flicker $(1/f)$ noise measurement could be a powerful technique to characterize the oxide trap distribution in the gate dielectric of MOSFETs [38]–[40]. Since there are high densities of acceptor and donor oxide border traps in InGaAs n-MOSFET generated under PBTI stress as described in the Sections III and IV, $1/f$ noise measurements should be useful to further understand the oxide trap properties as well as the MOSFET performance under stress. In this section, a preliminary $1/f$ noise measurement result of $In_{0.53}Ga_{0.47}As$ n-MOSFETs under PBTI stress is presented.

Fig. 17 shows the normalized noise power spectral densities $S(f)/I_d^2$ [38] versus frequency f for $In_{0.53}Ga_{0.47}As$ n-MOSFETs for the fresh device (spectrum I), right after 500 s PBTI stress (spectrum S), and after 2000 s recovery phase (spectrum R) respectively. Obvious correlations between the donor and acceptor border traps described in Sections III and IV and the shape of the $S(f)/I_d^2$ spectra in Fig. 17 are observed. (1) Since there are only acceptor oxide traps while all donor traps are almost completely recovered after the 2000 s recovery phase as described in Sections III–V, the difference between spectra I and R in Fig. 17(a) reflects the contribution of generated acceptor border tarps to the $S(f)$ spectrum. It is observed that acceptor border traps mainly affect (increase) the flicker noise in the frequency range around and above 100 Hz. (2) Since there are both donor and acceptor border traps at the instance right after 500 s PBTI stress, the difference between spectra I and S in Fig. 17(b) reflects the contribution of both donor and acceptor traps to the $S(f)$ spectrum. The S spectrum has significant increase in the frequency range below 100 Hz comparing to the I spectrum. Combining Fig. 17(a) and (b), it indicates that donor traps mainly affect (increase) the spectrum below 100 Hz. More detailed and quantitative investigations of flicker noise measurements and their correlation to the donor and acceptor border traps for the InGaAs n-MOSFET will be published else where.

VII. EFFECTS OF BORDER TRAPS ON THE DEVICE PERFORMANCE AND LIFETIME

As described in Sections III–V, the donor traps mainly induce the off-current degradation. However the trapping and de-trapping of the donor traps response very slowly and may not response in fast switching applications in logic circuits. In the analog applications in a class A amplifier, a constant DC bias is applied with a constant DC operating current and therefore the off-current is also not important. Particularly, the degradation induced by donor traps is recoverable when the stress is released. Therefore the degradation is not cumulative in many ac switching circuit applications and in daily turn-on turn-off system. On the other hand, the acceptor traps degrade the on-current and transconductance permanently and the degradations are cumulative. In the long term device lifetime determination, acceptor traps generation rate is the key factor to be concerned.

VIII. CONCLUSION

We have presented the charge pumping, DC and fast pulsed I_s–V_g measurements results to investigate the degradations under PBTI stress for the $In_xGa_{1-x}As$ n-MOSFETs with $x =$ 0.53 and 0.65. The stress induced traps are mainly slow oxide border traps including two components: (1) The recoverable donor traps with energy density $\Delta D_{\rm SOX}^{\rm Donor}(E)$. It has a large distribution in the InGaAs energy gap, with a tail extending to the conduction band. It is responsible for the negative ΔV_g in the sub-threshold region, the S degradation, the $I_s^{\rm off}$ degradation of the I_s–V_g curve in the stress phase, and continuous degradation of positive ΔV_g in the on current region in the recovery phase. The donor taps are almost completely recovered in the recovery phase. (2) The permanent acceptor traps with energy density $\Delta D_{\rm SOX}^{\rm Acceptor}(E)$. It is mainly distributed in the conduction band of InGaAs with a tail extending to the mid-gap. It is responsible for the positive ΔV_g and transconductance degradation in the on current region of the I_s–V_g curve after stress. The flicker noise power spectra and their correlation to the donor and acceptor border traps are also shown. The device lifetime is mainly determined by the acceptor border trap generation rate under stress. The border traps generated in InGaAs/Al$_2$O$_3$ MOS devices are very different from the traps in Si MOS devices with SiON or high-k dielectrics, and deserve more comprehensive investigations in the future.

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