8-2-2013

Interface studies of N-2 plasma-treated ZnSnO nanowire transistors using low-frequency noise measurements

Seongmin Kim
Birck Nanotechnology Center, Purdue University, kim482@purdue.edu

Hwansoo Kim
Kyonggi University

David B. Janes
Birck Nanotechnology Center, Purdue University, janes@purdue.edu

Sanghyun Ju
Kyonggi University

Kim, Seongmin; Kim, Hwansoo; Janes, David B.; and Ju, Sanghyun, "Interface studies of N-2 plasma-treated ZnSnO nanowire transistors using low-frequency noise measurements" (2013). *Birck and NCN Publications.* Paper 1446.
http://dx.doi.org/10.1088/0957-4484/24/30/305201

Interface studies of N_2 plasma-treated ZnSnO nanowire transistors using low-frequency noise measurements

2013 Nanotechnology 24 305201

(http://iopscience.iop.org/0957-4484/24/30/305201)

Nanotechnology **24** (2013) 305201 (7pp) doi:10.1088/0957-4484/24/30/305201

Interface studies of N_2 plasma-treated ZnSnO nanowire transistors using low-frequency noise measurements

Seongmin Kim[1], Hwansoo Kim[2], David B Janes[1] and Sanghyun Ju[2]

[1] School of Electrical and Computer Engineering and Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907, USA
[2] Department of Physics, Kyonggi University, Suwon, Gyeonggi-Do, 443-760, Republic of Korea

E-mail: shju@kgu.ac.kr

Received 8 January 2013, in final form 9 May 2013
Published 27 June 2013
Online at stacks.iop.org/Nano/24/305201

Abstract
Due to the large surface-to-volume ratio of nanowires, the quality of nanowire–insulator interfaces as well as the nanowire surface characteristics significantly influence the electrical characteristics of nanowire transistors (NWTs). To improve the electrical characteristics by doping or post-processing, it is important to evaluate the interface characteristics and stability of NWTs. In this study, we have synthesized ZnSnO (ZTO) nanowires using the chemical vapor deposition method, characterized the composition of ZTO nanowires using x-ray photoelectron spectroscopy, and fabricated ZTO NWTs. We have characterized the current–voltage characteristics and low-frequency noise of ZTO NWTs in order to investigate the effects of interface states on subthreshold slope (SS) and the noise before and after N_2 plasma treatments. The as-fabricated device exhibited a SS of 0.29 V/dec and Hooge parameter of $\sim 1.20 \times 10^{-2}$. Upon N_2 plasma treatment with N_2 gas flow rate of 40 sccm (20 sccm), the SS improved to 0.12 V/dec (0.21 V/dec) and the Hooge parameter decreased to $\sim 4.99 \times 10^{-3}$ (8.14×10^{-3}). The interface trap densities inferred from both SS and low-frequency noise decrease upon plasma treatment, with the highest flow rate yielding the smallest trap density. These results demonstrate that the N_2 plasma treatment decreases the interface trap states and defects on ZTO nanowires, thereby enabling the fabrication of high-quality nanowire interfaces.

(Some figures may appear in colour only in the online journal)

1. Introduction

Due to several advantages of nanowires such as transparency, flexibility, low operating voltages, and low fabrication temperatures, various studies have considered their applications to the development of various electronic, display, thermoelectric, environmental, and sensor devices [1–4]. The scope of nanowire transistor (NWT) integration in semiconductor complementary metal–oxide–semiconductor (CMOS) circuits is also increasing along with the high demand for device downscaling. In particular, many studies have been conducted on the development of NWTs and circuits using wide band-gap semiconducting oxides such as ZnO, SnO_2, In_2O_3, and Zn_2SnO_4 for applications including memory and displays [5–9]. However, in order to apply nanowires to practical and commercial devices, it is important to prioritize the optimization of the different characteristics required for various applications. For applications that require high performance, high current along with large mobility is essential. For low-power applications, low static power consumption at zero bias by achieving low off-current and steep subthreshold slope (SS) accompanied by threshold voltage (V_{th}) engineering is of great interest. For low-noise applications such as analog/mixed-signal circuits, low signal-to-noise ratio is essential for reliable device operation. Due to the large surface-to-volume ratio of the nanowires, nanowire

surface characteristics and nanowire–insulator interfaces are known to significantly influence the electrical characteristics of NWTs, which could potentially result in fluctuation of the device performance metrics such as SS, V_{th}, on/off current ratio (I_{on}/I_{off}), field effect mobility (μ_{eff}), and noise [10–13]. Hence, in order to achieve robust and stable device operation and improve the electrical characteristics of nanowires, it is important to evaluate and optimize the nanowire surface characteristics. Numerous studies have been performed to optimize the optical, chemical, and electrical characteristics of nanowires. Some studies have been conducted on controlling the characteristics by changing the nanowire growth temperatures and controlling the characteristics of grown nanowires through gas treatments, thermal annealing, or plasma treatments [14–17]. Other studies have focused on controlling the characteristics by changing the nanowire material through the doping of metals or rare-earth materials [18–20]. For instance, the electrical characteristics of ZnO nanowires—a representative oxide semiconductor—have been improved by Ni, Ga, and Sn doping [21–23]. Doping material or gas/plasma treatments influence the defects, such as oxygen vacancies, along with fixed charges and interface trap densities on the oxide nanowire surfaces. However, such nanowire transistors after optimization still exhibit large SS and low μ_{eff} showing that there is much room for improvement.

Low-frequency ($1/f$, flicker) noise has traditionally been utilized as a qualitative and a semi-quantitative measure of the origin of the noise, and a reliability indicator for semiconductor devices. The use of $1/f$ noise as a defect characterization method has become more popular in recent years, since $1/f$ noise is more sensitive to traps and defects in highly scaled devices such as nanotube- or nanowire-based field effect transistors (FETs) where scattering from surface states is enhanced [24]. The $1/f$ noise that originates from the trapping and detrapping of carriers at the channel, oxide, and their interface, provides significant information regarding the densities of the interface (surface) states in nanoscale devices [25–28]. The reported Hooge parameters (α_H) for non-Si nanowire transistors to date, however, are far higher than the ITRS 45 nm technology node requirement ($\alpha_H \sim 2.0 \times 10^{-4}$) indicating that further improvement in the interface quality is essential in order to achieve nanowire transistors that can be applied to commercial digital and analog circuits [11, 12, 40]. In this research, we synthesized ZnSnO (ZTO) nanowires using chemical vapor deposition (CVD), and then characterized the composition of ZTO nanowires using x-ray photoelectron spectroscopy (XPS). We then fabricated ZTO NWTs and investigated the changes in their characteristics during the N_2 plasma treatment. We have examined the quality of the device interfaces in ZTO NWTs before and after the N_2 plasma treatment using the SS characteristics and $1/f$ noise measurements. This reveals that the N_2 plasma-treated ZTO NWTs show excellent device performance suitable for high-performance (high μ_{eff}), low-power (low SS, V_{th} near zero), and low-noise (low α_H) applications.

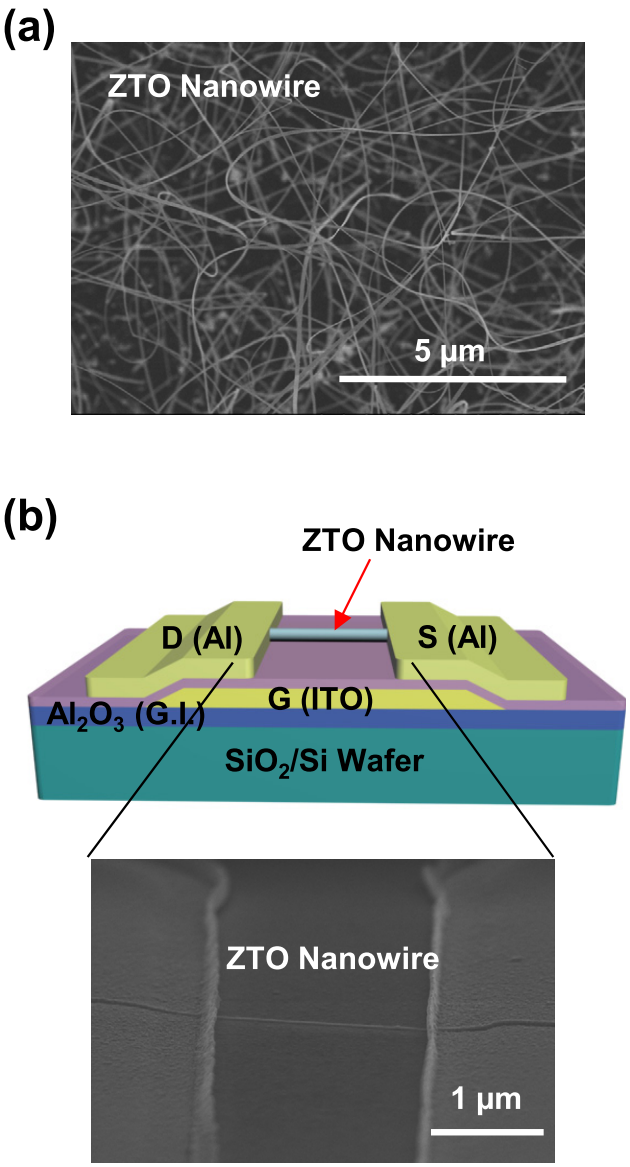

Figure 1. (a) FE-SEM image of as-grown ZTO nanowires. (b) Cross-sectional view of ZTO NWT with bottom gate structure. The inset shows the representative FE-SEM image of the nanowire channel region for a NWT with a single nanowire.

2. Experimental section

2.1. Synthesis of ZTO nanowires

The ZTO nanowires used in the fabrication process were grown by CVD method in a two-temperature-zone furnace that enabled us to adjust the source and substrate temperatures separately. We placed the combination of ZnO (99.999%, 0.6 g) and SnO (99.99%, 0.0149 g) in the source zone and located the SiO_2/Si wafer uniformly coated with catalyst particles (gold nanoparticles, diameter: 20 nm) in the substrate zone. We then increased the temperature to 1090 °C in the source zone and to 720 °C in the substrate zone to facilitate the nanowire growth. Figure 1(a) shows the field emission scanning electron microscope (FE-SEM) image of the grown ZTO nanowires. The ZTO nanowires exhibited

uniform growth throughout the substrate and their average diameter and length were ∼60 nm and ∼5 μm, respectively.

2.2. Fabrication of ZTO NWTs

For the fabrication of the ZTO NWTs, we employed a separate SiO_2/Si substrate and performed the following processes: bottom gate electrode formation, gate-dielectric layer formation, gate contact hole etching, nanowire dispersion, and source/drain electrode formation. First, the bottom gate electrode was formed by indium tin oxide (ITO, 100 nm) sputtering, and photolithographic patterning. Subsequently, a 30-nm-thick Al_2O_3 gate dielectric film was deposited by atomic layer deposition (ALD). The Al_2O_3 layer was removed selectively at the gate electrode pad area in order to apply voltages to the gate electrode. After separating the ZTO nanowires from the growth substrate in isopropyl alcohol solution by ultrasonication, the nanowires were dispersed on the device substrate. As the last step, source–drain electrodes were formed by sputtering Al (thickness of 100 nm) and subsequent photolithographic patterning. Figure 1(b) shows the schematic diagram of the ZTO NWT and a representative FE-SEM image of the nanowire channel region. The channel length and diameter of the representative device were ∼2 μm and 60 nm respectively.

2.3. Functionalization and characterization of ZTO NWTs

We performed two types of N_2 plasma treatments for the fabricated devices. Regarding the conditions of the N_2 plasma treatment, the N_2 flow rate was divided into two different conditions—20 and 40 sccm—but the remaining conditions remained consistent at a bias power of 50 W, pressure of 200 mTorr, and exposure time of 60 s. In order to analyze the results, the $1/f$ noise characteristics of the as-fabricated and the plasma-treated devices were measured using a SR 570 low-noise current pre-amplifier and a HP 3561A dynamic signal analyzer.

3. Results and discussion

X-ray photoelectron spectroscopy (XPS) was employed to observe the chemical structure of the ZTO nanowires before and after N_2 plasma treatment with varied N_2 gas flow rate of 20 and 40 sccm. Figure 2 shows the Zn 2p, Sn 3d and N 1s core-level spectra of ZTO nanowires before and after N_2 plasma treatment (20 and 40 sccm). As shown in figure 2(a), the binding energies of Zn $2p_{1/2}$ and Zn $2p_{3/2}$ were observed at 1044.58 and 1021.38 eV prior to N_2 plasma treatment. Following N_2 plasma treatment, the binding energies of Zn $2p_{1/2}$ and Zn $2p_{3/2}$ exhibit slight shifts towards the higher energy level by ∼0.1 eV (20 sccm) and ∼0.2 eV (40 sccm), respectively. Such slight shifts in binding energies can be attributed to the change of surface states and the increased number of oxygen vacancies at the nanowire surface which is also consistent with previous literature [29, 30]. The binding energies of Sn $3d_{3/2}$ and Sn $3d_{5/2}$ peaks were seen at 494.68

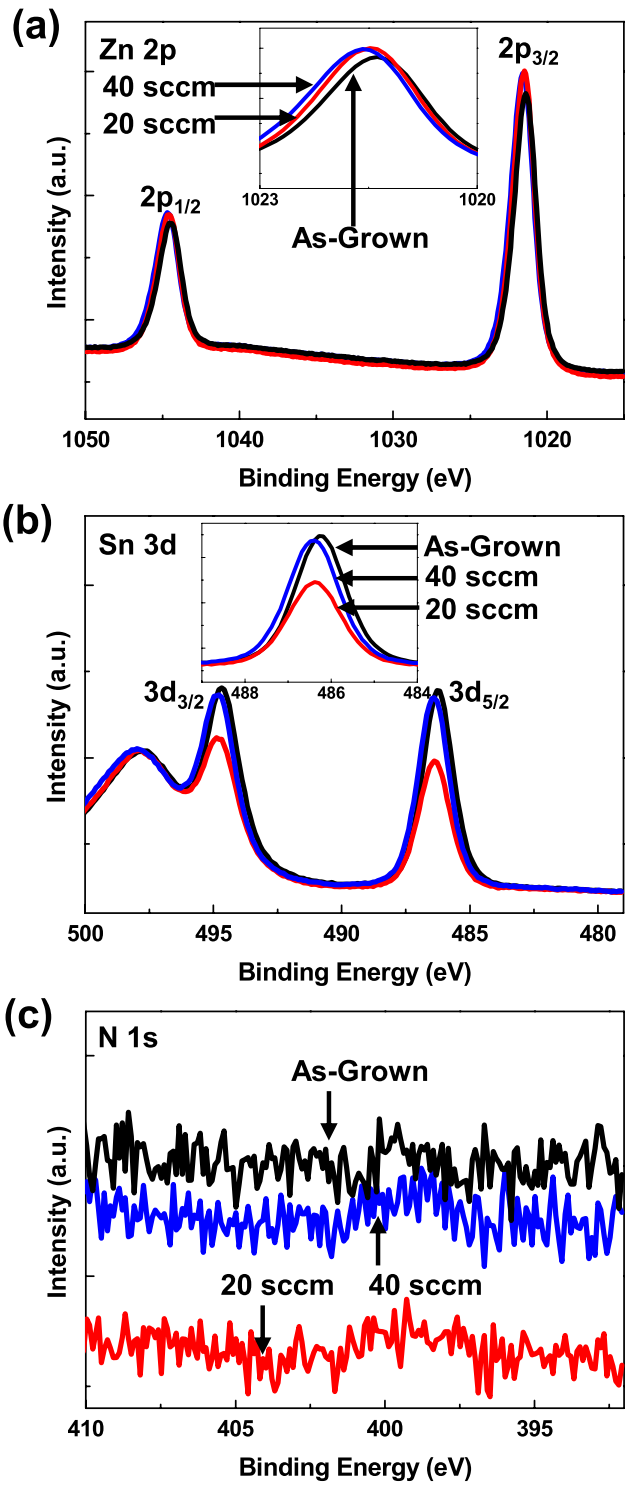

Figure 2. XPS profile for (a) Zn 2p peaks, (b) Sn 3d peaks, and (c) N 1s peaks of ZTO nanowires before and after N_2 plasma treatment (20 and 40 sccm).

and 486.28 eV before N_2 plasma treatment (figure 2(b)). As shown in the inset of figure 2(b), after N_2 plasma treatment, the binding energies of Sn $3d_{3/2}$ and Sn $3d_{5/2}$ peaks showed slight shifts towards higher energy level by ∼0.1 eV (Sn $3d_{5/2}$) and ∼0.2 eV (Sn $3d_{3/2}$) [31, 32]. On the other hand, the fine spectra of N 1s did not show any distinct peaks over

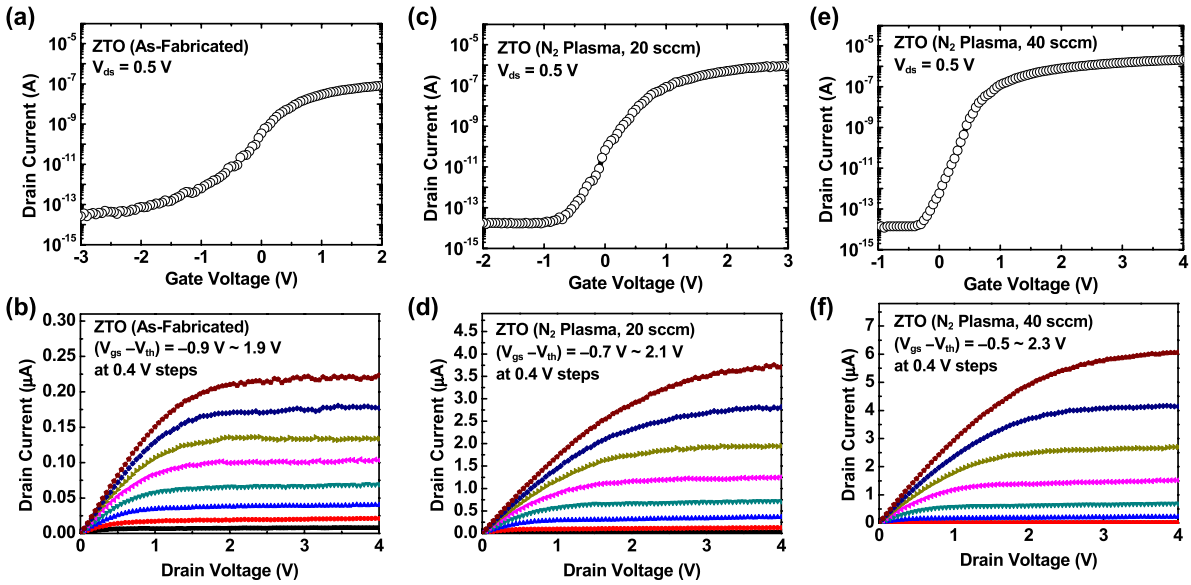

Figure 3. I_{ds}–V_{gs} characteristics and I_{ds}–V_{ds} characteristics of ZTO NWTs ((a), (b)) before and after N_2 plasma treatments with different N_2 flow rates of ((c), (d)) 20 sccm and ((e), (f)) 40 sccm.

the range even after N_2 plasma treatment (figure 2(c)). The absence of nitrogen shown from the XPS data indicates that there is no significant chemical bonding between the ZTO nanowires and the nitrogen ions generated by the plasma. The atomic percentage of Sn to the total amount of Zn and Sn (Sn/(Sn + Zn)) obtained by the XPS is approximately 22.4%.

Figure 3 shows the drain current versus gate–source voltage (I_{ds}–V_{gs}) and the drain current versus drain–source voltage (I_{ds}–V_{ds}) characteristics of the ZTO NWTs before and after the N_2 plasma treatment with different N_2 flow rate of 20 and 40 sccm, respectively. In all cases, the ZTO NWTs exhibit typical characteristics of n-channel transistors. The I_{ds}–V_{gs} curve of the as-fabricated ZTO NWT at $V_{ds} = 0.5$ V (as-fabricated) is shown in figure 3(a). The representative device exhibits V_{th} (V_{gs} at $I_{ds} = 1$ nA) of 0.1 V, SS of 0.29 V/dec, μ_{eff} of 10 cm^2 V^{-1} s^{-1}, and I_{on}/I_{off} of 4.8×10^6. Here, μ_{eff} was extracted using the MOSFET model at small V_{ds} ($\mu_{eff} = (dI_{ds}/dV_{gs}) \times L_{ch}^2/C_i/V_{ds}$), where $L_{ch} \sim 2$ μm is the channel length, and C_i is the gate-to-channel capacitance. The gate-to-channel capacitance is determined from the cylinder-on-plate model ($C_i = 2\pi\varepsilon_0 k_{eff}/\cosh^{-1}(1 + t_{ox}/r_{nw})$), where $k_{eff} \sim 9$ is the effective dielectric constant of Al_2O_3; $t_{ox} \sim 30$ nm, oxide thickness; and $r_{nw} \sim 30$ nm, the nanowire radius. Figure 3(b) shows the I_{ds}–V_{ds} curve of the as-fabricated ZTO NWT. The on-current (I_{on}) of the device is 0.19 μA ($V_{ds} = 4$ V and (V_{gs}–V_{th}) = 1.9 V). For the ZTO NWTs exposed to N_2 plasma with N_2 gas flow rate of 20 sccm, positively shifted $V_{th} = 0.3$ V, reduced SS = 0.21 V/dec, increased $\mu_{eff} = 79$ cm^2 V^{-1} s^{-1}, improved $I_{on}/I_{off} = 5.9 \times 10^7$, and increased $I_{on} = 3.7$ μA ($V_{ds} = 4$ V and (V_{gs}–V_{th}) = 2.1 V) are obtained from the I_{ds}–V_{gs} and I_{ds}–V_{ds} curves (figures 3(c) and (d)), respectively. Figures 3(e) and (f) show the I_{ds}–V_{gs} and I_{ds}–V_{ds} characteristics of the ZTO NWTs after the N_2 plasma treatment with the flow rate of 40 sccm. In this case, the device performance metrics further improve to $V_{th} = 0.5$ V, SS = 0.12 V/dec, $\mu_{eff} = 112$ cm^2 V^{-1} s^{-1}, $I_{on}/I_{off} = 1.2 \times 10^8$, and $I_{on} = 4.1$ μA ($V_{ds} = 4$ V and (V_{gs}–V_{th}) = 1.9 V). Note that the performance characteristics of ZTO NWTs following N_2 plasma treatment did not show significant changes under repeated measurement for seven days at room temperature in ambient air. In summary, upon N_2 plasma treatment with increased N_2 gas flow rate from 20 to 40 sccm, the device performance metrics of ZTO NWTs were improved in terms of SS, μ_{eff}, I_{on}/I_{off}, I_{on}, along with positive shift in V_{th}.

In order to investigate the effect of N_2 plasma treatment on the interface quality of ZTO NWTs, the $1/f$ noise was measured for ZTO NWTs before and after the N_2 plasma treatment with different N_2 flow rates of 20 and 40 sccm. According to Hooge's empirical model, low-frequency noise is often characterized by the relationship

$$\frac{S_I}{I_{ds}^2} = \frac{A}{f^\eta} = \frac{\alpha_H}{Nf^\eta} \tag{1}$$

where S_I is the drain current noise spectrum; I_{ds}, the drain current; A, the noise amplitude; α_H, Hooge parameter; N, the total number of carriers in the nanowire channel; f, the frequency; and η, the frequency exponent (ideally 1) [25, 26]. In the device on-region, where $V_{gs} > V_{th}$, the equilibrium charge in the channel can be re-written as

$$Q = qN = C_i|V_{gs} - V_{th}| \tag{2}$$

where q is the electronic charge. Combining equations (1) and (2), the current noise spectrum from the channel at the on-region can be expressed as

$$\frac{S_I}{I_{ds}^2} = \frac{q\alpha_H}{f^\eta C_i}|V_{gs} - V_{th}|^{-1} = \beta|V_{gs} - V_{th}|^{-1} \tag{3}$$

where $\beta = q\alpha_H f^{-\eta} C_i^{-1}$. Figure 4(a) shows the normalized current noise spectral density (S_I/I_{ds}^2) versus frequency (ranging from 1 Hz to 1.6 kHz) plot of ZTO NWTs prior to

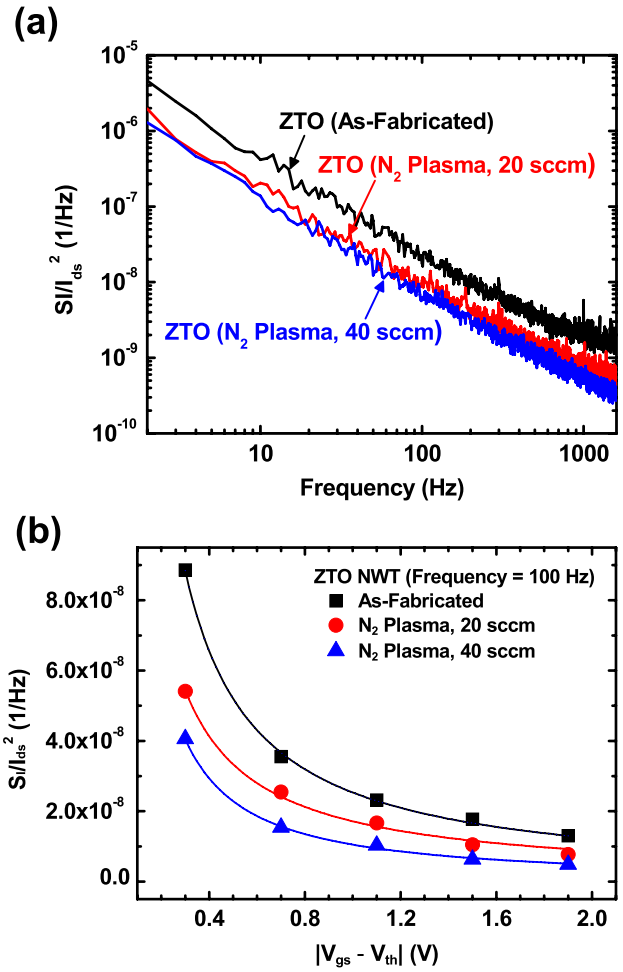

Figure 4. (a) Normalized drain current noise spectrum (S_I/I_{ds}^2) (at $(V_{gs}–V_{th}) = 1.5$ V) versus frequency and (b) S_I/I_{ds}^2 (at 100 Hz) versus $(V_{gs}–V_{th})$ of ZTO NWTs before and after N_2 plasma treatments with different N_2 flow rates (20 and 40 sccm). The solid curves shown in (b) are the non-linear curve fits to each data points (symbol).

and following N_2 plasma treatment at $(V_{gs}–V_{th}) = 1.5$ V. The frequency exponent η is obtained as 0.96–0.99, i.e., close to unity, from the linear fit of the spectrum. Note that η being approximately unity indicates that slow and fast traps are evenly distributed [33]. As shown in figure 4(a), S_I/I_{ds}^2 of the ZTO NWTs following N_2 plasma treatment with flow rates of 40 sccm (20 sccm) are reduced by 65% (41%) from that of the as-fabricated ZTO NWTs, respectively.

The $1/f$ noise in nanowire/nanotube-based transistors, which generally utilize metal source–drain electrodes similar to SB-FETs, may stem from (i) the excess noise in the metal–semiconductor Schottky barrier accompanying the generation–recombination noise in the space charge region, and/or (ii) electron trapping–detrapping events at the channel-to-dielectric interface, leading to carrier number fluctuations in the channel [12, 34]. In order to investigate the source of the noise in the fabricated ZTO NWTs, the current noise spectrum normalized by the drain current (S_I/I_{ds}^2) versus $(V_{gs}–V_{th})$ for ZTO NWTs before and after N_2 plasma treatment is plotted in figure 4(b). Note that the measured S_I/I_{ds}^2 decreases non-linearly under the given range of $(V_{gs}–V_{th})$ for all cases. From the curve fitting of $S_I/I_{ds}^2 = \beta(V_{gs} - V_{th})^m$ (solid curves) for each case (symbol), m values of -1.04 and -1.12 (-0.96) are obtained for ZTO NWTs before and after N_2 plasma treatment with flow rate of 40 (20) sccm, respectively. Such proportionality (m near -1) between S_I/I_{ds}^2 and $(V_{gs}–V_{th})$ has often been observed in FETs using carbon nanotubes and SnO_2 nanowires as the channel material [11, 27]. In studies of $1/f$ noise in the on-region of ZnO NWTs, $m = -1$ behavior is observed at low $(V_{gs}–V_{th})$ values, but $m = 0$ is observed when $(V_{gs}–V_{th})$ is very high (extreme on-region) [35]. It has also been reported that S_I/I_{ds}^2 in MODFETs and InAs NWTs exhibits different V_{gs}^m dependences (m values of -1, -3, 0, and $+2$) depending on whether the contacts or channel dominate the noise and resistance, where m equals -1 (0) when the channel (contact) dominates both noise and resistance [36, 37]. As the S_I/I_{ds}^2 in our ZTO NWTs show $m = -1$ behavior with no sign of a $m = 0$ region, the channel appears to dominate both the noise and resistance throughout the measured V_{gs} range. Furthermore, the low-field channel conductance (G_{ch}), which is directly measured from the slope of I_{ds}–V_{ds} curves (figure 3) at low V_{ds}, increases approximately linearly with V_{gs} from V_{th} without saturation due to contact resistance (R_{sb}) limit, indicating that the channel resistance is dominating the overall resistance in the measured V_{gs} range. Note that α_H can be extracted from equation (3) and the β values extracted from the non-linear fitting in figure 4(b). For the as-fabricated ZTO NWT, α_H is calculated as 1.20×10^{-2} where $\beta = 2.53 \times 10^{-8}$. Following N_2 plasma treatment of ZTO NWTs with N_2 flow rates of 20 sccm and 40 sccm, lower α_H of 8.14×10^{-3} ($\beta = 1.71 \times 10^{-8}$) and 4.99×10^{-3} ($\beta = 1.05 \times 10^{-8}$) are estimated, respectively. Hooge parameter α_H is often used as a figure-of-merit to compare the $1/f$ noise in different devices regardless of the measurement ambient and material which gives important information about the interface trap densities. The reduction of α_H upon N_2 plasma treatment indicates that the interface traps are reduced at the nanowire channel [11, 12, 40, 45]. Although the nanowires exhibit high surface-to-volume ratios, α_H value obtained from the N_2 plasma-treated ZTO NWTs (40 sccm) are comparable to or lower than that of the CMOS FETs developed using metal gate and high-k gate dielectric [38, 39]. Furthermore, the $\alpha_H \sim 4.99 \times 10^{-3}$ for ZTO NWT is among the lowest value reported in oxide-based TFTs and NWTs as shown in figure 5. Note that the α_H obtained from the N_2 plasma-treated ZTO NWT (40 sccm) is nearly one order of magnitude lower than the previously reported Hooge's parameter values extracted from oxide-based (ZnO, In_2O_3, and SnO_2) NWTs [11, 12, 40]. Although our measurements were performed in air, the $\alpha_H \sim 4.99 \times 10^{-3}$ for ZTO NWT is comparable to the value previously reported for ZnO NWTs measured in ultrahigh vacuum; 2–4 times higher values are typically observed for measurements in oxygen ambient [35].

The decrease in S_I/I_{ds}^2 (and α_H) and improvement of the device performance upon N_2 plasma treatment is known to be attributed to the decrease of interface trap density and

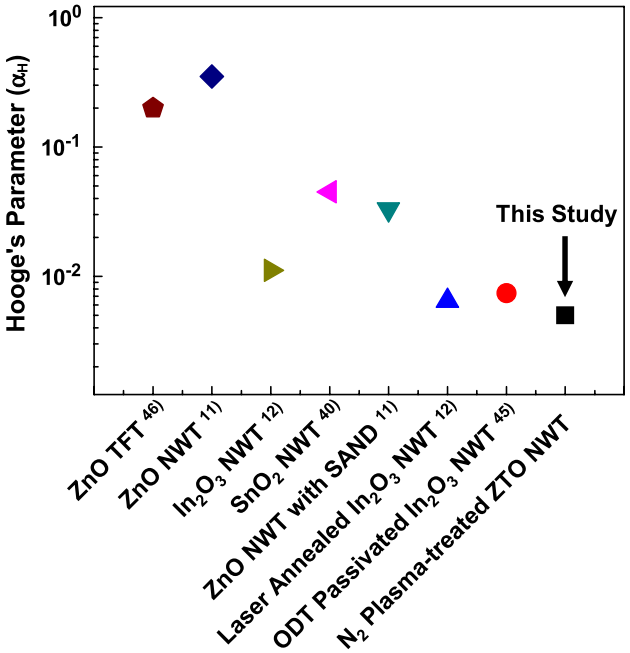

Figure 5. Hooge's parameters of various oxide-based TFTs and NWTs.

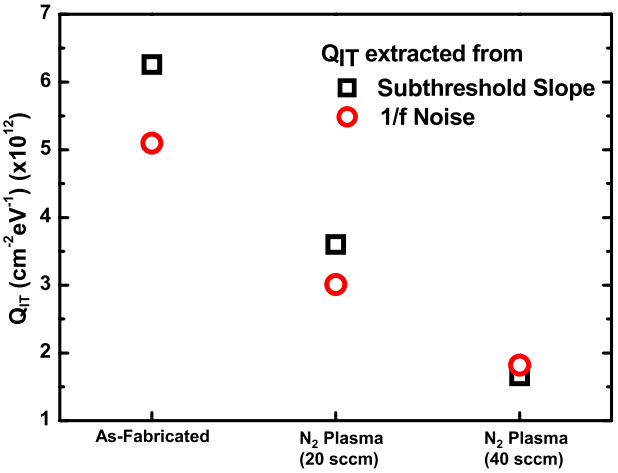

Figure 6. The interface trap density (Q_{IT}) values extracted from the SS and $1/f$ noise spectrum (at 100 Hz) are shown for ZTO NWTs before and after N_2 plasma treatment with different N_2 flow rates (20 and 40 sccm).

the reduction of surface scattering at the nanowire channel region [36, 37]. Note that as the plasma treatment is performed after the source–drain metallization, the metal-to-nanowire contact is expected to be shielded from the effects of the plasma, although the band-bending near the contacts may change. It has been reported in previous literature that plasma treatment removes surface organic layers and contaminants, increasing the adhesion between layers and improving the interface quality [41, 42]. To investigate the shift in the interface trap densities (Q_{IT}) upon N_2 plasma treatment, we calculated the Q_{IT} from the measured $1/f$ noise amplitude and SS. When carrier number fluctuation is the dominant mechanism in $1/f$ noise, S_I/I_{ds}^2 can be expressed as

$$\frac{S_I}{I_{ds}^2} = \frac{kT}{f\gamma N^2 r_{nw} L_{ch}} N_{IT}(E_F) \tag{4}$$

from the unified model for flicker noise reported by Hung *et al* [43]. Here, k is the Boltzmann constant, T the temperature, $N_{IT}(E_F)$ the interface trap density at the Fermi level (E_F) (in units of cm^{-3} eV^{-1}), and $\gamma = 4\pi\sqrt{2m^*\Phi_{TB}}/h$ the attenuation coefficient of the electron wavefunction in the oxide where h is the Planck's constant, m^* is the effective mass of the carrier in oxide, and Φ_{TB} is the tunneling barrier height seen by the carriers at the interface [43]. From equation (4) and S_I/I_{ds}^2 values ($f = 100$ Hz) at fixed $(V_{gs}–V_{th}) = 1.5$ V, Q_{IT} values of 5.10×10^{12} cm^{-2} eV^{-1} and 1.82×10^{12} cm^2 eV^{-1} (3.01×10^{12} cm^{-12} eV^{-1}) are extracted for as-fabricated and 40 sccm (20 sccm) N_2-plasma-treated ZTO NWTs, respectively (figure 6).

While $1/f$ noise is well known to provide information about the Q_{IT} near the Fermi level, SS is more related to the Q_{IT} in the subthreshold region [43]. The SS can be calculated from the equation [44]

$$SS = (\ln 10)\left(\frac{kT}{q}\right)\left(1 + \frac{C_{dep} + C_{IT}}{C_{ox}}\right). \tag{5}$$

In fully depleted nanowires, C_{dep}, the depletion-layer capacitance is negligible, while $C_{IT} = q^2 Q_{IT}$, the interface trap capacitance, and C_{ox}, the oxide capacitance (in units of F cm^{-2}), play a major role in determining the SS values. From equation (5) and the measured SS values, Q_{IT} of 5.10×10^{12} cm^{-2} eV^{-1} and 1.82×10^{12} cm^{-2} eV^{-1} (3.01×10^{12} cm^{-2} eV^{-1}) are estimated for as-fabricated and 40 (20) sccm N_2 plasma-treated devices, respectively (figure 6). We have reported that in the case of back-gated devices where the cylindrical nanowires are placed on top of a large plane of gate dielectric, the Q_{IT} extracted from $1/f$ noise spectrum is closely related to the traps located at the nanowire-to-dielectric interface, while Q_{IT} from SS is more related to the quality of the nanowire surface exposed to ambient [45]. Note that the Q_{IT} values extracted from both $1/f$ noise and SS decreased upon N_2 plasma treatment with increased N_2 gas flow rate, indicating that the decreased SS, lowered noise power and lowered α_H upon plasma treatment is presumably related to the improvement in the quality of the nanowire surface as well as the interface at the nanowire-to-dielectric. Therefore, the decreased Q_{IT} upon plasma treatment is expected to reduce the surface scattering and improve the ZTO NWT performance in terms of SS, μ_{eff}, I_{on}, I_{on}/I_{off} and V_{th}. Also, the slight increase of oxygen vacancies, donor-like traps, after N_2 plasma exposure (evidenced from the XPS data) further increases the conductivity of the nanowire and hence increases I_{on} [3, 14, 45].

4. Conclusions

In summary, the interface quality of high-performance ZTO NWTs after the N_2 plasma treatment was investigated by the

current–voltage characteristics and $1/f$ noise as a function of gate bias. The N_2 plasma treatment was employed in order to reduce the interface state densities, to improve the device performance metrics in terms of SS, μ_{eff}, $I_{\text{on}}/I_{\text{off}}$, and I_{on}, and to achieve low-noise densities. The S_I/I_{ds}^2 values of the N_2 plasma-treated ZTO NWTs with N_2 flow rates of 20 and 40 sccm were 41% and 65% less than that of as-fabricated ZTO NWTs. The low α_{H} value of $\sim 4.99 \times 10^{-3}$ for the N_2 plasma-treated (40 sccm) ZTO NWTs indicated that the ZTO nanowire interface had higher quality than the as-fabricated ZTO nanowire interface. These results suggest opportunities for the fabrication of robust and high-quality ZTO NWTs that can be applied to low-power, high-performance, and low-noise nano-electronic devices.

Acknowledgments

We thank C J Delker at Purdue University for discussions on $1/f$ noise physics. This research was partially supported by the National Research Foundation of Korea (NRF) funded by the Ministry of Education, Science and Technology (2012K001317 and 2012R1A2A2A01013734), and also supported by the National Science Foundation (ECCS-1118934 and ECCS-1202281).

References

[1] Cui Y and Lieber C M 2001 *Science* **291** 851
[2] Hochbaum A I, Chen R, Delgado R D, Liang W, Garnett E C, Najarian M, Majumdar A and Yang P 2008 *Nature* **451** 163
[3] Ju S, Facchetti A, Xuan Y, Liu J, Ishikawa F, Ye P, Zhou C, Marks T J and Janes D B 2007 *Nature Nanotechnol.* **2** 378
[4] Kolmakov A, Zhang Y, Cheng G and Moskovits M 2003 *Adv. Mater.* **15** 997
[5] Park W I, Kim J S, Yi G-C and Lee H-J 2005 *Adv. Mater.* **17** 1393
[6] Ju S *et al* 2008 *Nano Lett.* **8** 997
[7] Dattoli E N, Wan Q, Guo W, Chen Y, Pan X and Lu W 2007 *Nano Lett.* **8** 2463
[8] Ju S, Ishikawa F, Chen P, Chang H-K, Zhou C, Ha Y, Liu J, Facchetti A, Marks T J and Janes D B 2008 *Appl. Phys. Lett.* **92** 222105
[9] Lim T, Kim H, Meyyappan M and Ju S 2012 *ACS Nano* **6** 4912
[10] Zhuge J, Wang R, Hunag R, Tian Y, Zhang L, Kim D-W, Park D and Wang Y 2009 *IEEE Electron Device Lett.* **30** 57
[11] Ju S, Kim S, Mohammadi S, Janes D B, Ha Y-G, Facchetti A and Marks T 2008 *J. Appl. Phys. Lett.* **92** 022104
[12] Kim S *et al* 2011 *J. Phys. Chem.* C **115** 17147
[13] Wang J, Polizzi E, Ghosh A, Datta S and Lundstrom M 2005 *Appl. Phys. Lett.* **87** 043101
[14] Kim S, Delker C, Chen P, Zhou C, Ju S and Janes D B 2010 *Nanotechnology* **21** 145207
[15] Kim S, Lim T and Ju S 2011 *Nanotechnology* **22** 305704
[16] Law J B K and Thong J T L 2008 *Nanotechnology* **19** 205502
[17] Greene L E, Law M, Goldberger J, Kim F, Johnson J C, Zhang Y, Saykally R J and Yang P 2003 *Angew. Chem. Int. Edn* **42** 3031
[18] Wan Q, Dattoli E N and Lu W 2007 *Appl. Phys. Lett.* **90** 222107
[19] Chen P-C *et al* 2009 *ACS Nano* **3** 3383
[20] Shen Y, Yamazaki T, Liu Z, Meng D, Kikuta T, Nakatani N, Saito M and Mori M 2009 *Sensors Actuators* B **135** 524
[21] He H Jr, Lao C S, Chen L J, Davidovic D and Wang Z L 2005 *J. Am. Chem. Soc.* **127** 16376
[22] Bae S Y, Na C W, Kang J H and Park J 2005 *J. Phys. Chem.* B **109** 2526
[23] Li S Y, Lin P, Lee C Y, Tseng T Y and Huang C J 2004 *J. Phys. D: Appl. Phys.* **37** 2274
[24] Bid A, Bora A and Raychaudhuri A K 2006 *Nanotechnology* **17** 152
[25] Scholten A J, Tiemeijer L F, van Langevelde R, Havens R J, Zegers-van Duijnhoven A T A and Venezia V C 2003 *IEEE Trans. Eelectron Devices* **50** 618
[26] Rumyantsev S L, Shur M S, Levinshtein M E, Motayed A and Davydov A V 2008 *J. Appl. Phys.* **103** 064501
[27] Ishigami M, Chen J H, Williams E D, Tobias D, Chen Y F and Fuhrer M S 2006 *Appl. Phys. Lett.* **88** 203116
[28] Fan Z, Wang D, Chang P, Tseng W and Lu J G 2004 *Appl. Phys. Lett.* **85** 5923
[29] Remashan K, Hwang D K, Park S D, Bae J W, Yeom G Y, Park S J and Janga J H 2008 *Electrochem. Solid-State Lett.* **11** H55
[30] Zhang Y, Du G, Wang X, Li W, Yang X, Ma Y, Zhao B, Yang H, Liu D and Yang S 2003 *J. Cryst. Growth* **252** 180
[31] Jing L, Fu H, Wang B, Wang D, Xin B, Li S and Sun J 2006 *Appl. Catal.* B **62** 282
[32] Themlin J-M, Chtaib M, Henrard L, Lambin P, Darville J and Gilles J-M 1992 *Phys. Rev.* B **46** 2460
[33] von Haartman M and Östling M 2007 *Low-Frequency Noise in Advanced MOS Devices* (New York: Springer)
[34] Kim S, Kim S, Janes D B, Mohammadi S, Baek J and Shim M 2010 *Nanotechnology* **21** 385203
[35] Wang W, Xiong H D, Edelstein M D, Gundlach D, Suehle H S, Richter C A, Hong W K and Lee T 2007 *J. Appl. Phys.* **101** 044313
[36] Vandamme L K J 1994 *IEEE Trans. Electron Devices* **41** 2176
[37] Delker C, Kim S, Borg M, Wernersson L and Janes D B 2012 *IEEE Trans. Electron Devices* **59** 1980
[38] Claeys C, Simoen E, Mercha A, Pantisano L and Young E 2005 *J. Electrochem. Soc.* **152** F115
[39] Min B, Devireddy S P, Çelik-Butler Z, Wang F, Zlotnicka A, Tseng H-H and Tobin P J 2004 *IEEE Trans. Electron Devices* **51** 1315
[40] Ju S, Chen P, Zhou C, Ha Y-G, Facchetti A, Marks T J, Kim S, Mohammadi S and Janes D B 2008 *Appl. Phys. Lett.* **92** 243120
[41] Shenton M J and Stevens G C 2001 *J. Phys. D: Appl. Phys.* **34** 2761
[42] Shenton M J, Lovell-Hoare M C and Stevens G C 2001 *J. Phys. D: Appl. Phys.* **34** 2754
[43] Hung K K, Ko P K, Hu C and Cheng Y C 1990 *IEEE Trans. Electron Devices* **37** 654
[44] Sze S M and Ng K K 2007 *Physics of Semiconductor Devices* 3rd edn (Hoboken, NJ: Wiley)
[45] Kim S, Carpenter P D, Jean R K, Chen H, Zhou C, Ju S and Janes D B 2012 *ACS Nano* **6** 7352
[46] Jeong K S, Kim Y M, Park J G, Yang S D, Kim Y S and Lee G W 2011 *AIP Conf. Proc.* **1399** 891