7-2013

Engineering Nanowire n-MOSFETs at L-g < 8 nm

Saumitra Mehrotra
Birck Nanotechnology Center, Network for Computational Nanotechnology, Purdue University, smehrotr@purdue.edu

SungGeun Kim
Birck Nanotechnology Center, Network for Computational Nanotechnology, Purdue University, kim568@purdue.edu

Tillmann Kubis
Birck Nanotechnology Center, Network for Computational Nanotechnology, Purdue University, tkubis@purdue.edu

Michael Povolotskyi
Birck Nanotechnology Center, Network for Computational Nanotechnology, Purdue University, mpovolot@purdue.edu

Mark S. Lundstrom
Birck Nanotechnology Center, Network for Computational Nanotechnology, Purdue University, lundstro@purdue.edu

See next page for additional authors

Follow this and additional works at: http://docs.lib.purdue.edu/nanopub

Part of the Nanoscience and Nanotechnology Commons

Authors

Saumitra Mehrotra, SungGeun Kim, Tillmann Kubis, Michael Povolotskyi, Mark S. Lundstrom, and Gerhard Klimeck

Engineering Nanowire n-MOSFETs at $L_g < 8$ nm

Saumitra R. Mehrotra, *Student Member, IEEE*, SungGeun Kim, *Student Member, IEEE*, Tillmann Kubis, Michael Povolotskyi, Mark S. Lundstrom, and Gerhard Klimeck, *Fellow, IEEE*

Abstract—As metal-oxide-semiconductor field-effect transistors (MOSFETs) channel lengths (L_g) are scaled to lengths shorter than $L_g < 8$ nm source-drain tunneling starts to become a major performance limiting factor. In this scenario, a heavier transport mass can be used to limit source-drain (S-D) tunneling. Taking InAs and Si as examples, it is shown that different heavier transport masses can be engineered using strain and crystal-orientation engineering. Full-band extended device atomistic quantum transport simulations are performed for nanowire MOSFETs at $L_g < 8$ nm in both ballistic and incoherent scattering regimes. In conclusion, a heavier transport mass can indeed be advantageous in improving ON-state currents in ultrascaled nanowire MOSFETs.

Index Terms—InAs, nanowire, quantum transport, Si, source-drain tunneling, strain, tight-binding (TB) approach.

I. INTRODUCTION

SCALING of complementary metal-oxide-semiconductor (CMOS) technology for the past 40 years has led to the current device technology with channel lengths ≤ 30 nm [1]. The international technology roadmap for semiconductors (ITRS) predicts metal-oxide-semiconductor field-effect transistor (MOSFET) channel lengths to be < 8 nm in ten years [2]. In this extremely scaled regime, MOSFETs will suffer from excessive source-drain (S-D) tunneling, making it hard to turn off the device [3], [4]. Nanowire-based MOSFETs have emerged as promising candidates for future scaling as they offer the best electrostatic gate control over the channel [5]. Nanowire MOSFETs made from high-mobility III-V materials are being projected as the future of microelectronics [6]. However, it remains an open question as how practical it would be to scale MOSFETs to channel lengths below 8 nm. In such extremely scaled regime of operation, it becomes clear that the most critical aspect is to maintain good subthreshold characteristics.

The typical transistor approach prefers a light transport mass corresponding to high carrier velocities and a heavy confinement mass for higher quantum capacitance (C_q) [7]. A light transport mass, however, leads to an increased source drain tunneling and can lead to degraded OFF-state characteristics [8]–[10]. A heavy transport mass can limit S-D tunneling

but it also means lower channel mobility or degraded ON-state characteristics. This situation naturally leads to a tradeoff and begs the question: what transport mass will work the best for ultrascaled channel MOSFETs and can it be engineered?

This paper shows that different conduction band (CB) minima masses can be obtained in nanowire channels using strain and orientation engineering and how these changes will affect the transistor performance. In a Si nanowire, due to quantum confinement, the six bulk Δ values rearrange themselves in energy, with each equivalent set of Δ values forming its own separate energy ladder. Furthermore, the different sets of energy ladders can be rearranged in energy space using uniaxial strain leading to different band edge transport masses (Fig. 1). InAs as a channel material is also considered in this paper as a candidate for high-mobility material. Full-band quantum transport calculations are used to assess the ON-state ballistic and electron-phonon scattering limited device performance for the different CB minima mass nanowire devices. The simulation results suggest that for scaling of the channel lengths < 8 nm, increasing the transport mass leads to better device performance.

II. SIMULATION APPROACH

A. Nanowire Cases Considered in This Paper

Five different nanowire MOSFET cases are studied in this paper. At sub-8 nm channel lengths, a smaller diameter is critical for an increased gate control. At the same time, however, a smaller diameter leads to increased threshold voltage fluctuation due to process variations. Considering these issues, an optimal diameter, D = 3.8 nm, is used for all the simulations [11]. As a first step, the different CB minima mass conditions that can be achieved in Si and InAs nanowires are discussed. The applied stress values were chosen to be high enough such that the bottom-most band is energetically at least 2 kT lower than the next higher sub-band, while at the same time ensuring the stress values are experimentally achievable [12].

1) Unstrained Si <100>: Fig. 2(a) shows the case for an unstrained <100> oriented Si nanowire where the Δ_4 set of valleys form the CB minima. The CB minima mass here is the Si bulk projected transverse valley mass (m_t) of $\sim 0.19 m_o$. A slightly higher CB minima mass equal to $0.259 m_o$ is calculated using the tight-binding model. This increase can be attributed to quantum confinement effect [13], [14].

2) Compressive Stressed Si <100>: Unstrained Si <100> nanowire exhibits Δ_2 valleys that have a heavy transport mass but lie higher in energy due to its lighter confinement mass. On application of compressive stress, the heavy Δ_2 valleys are pulled down in energy. The CB minima mass in this case
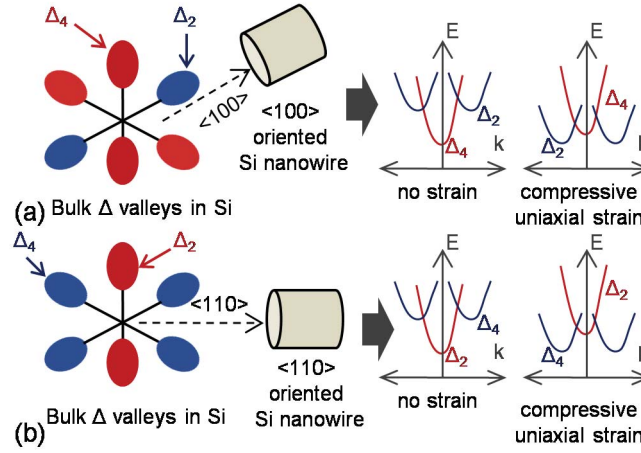
Fig. 1.   Schematic description of the formation of energy ladders or sub-bands in (a) <100> and (b) <110> oriented Si nanowire under no-strain and compressive-strain conditions.
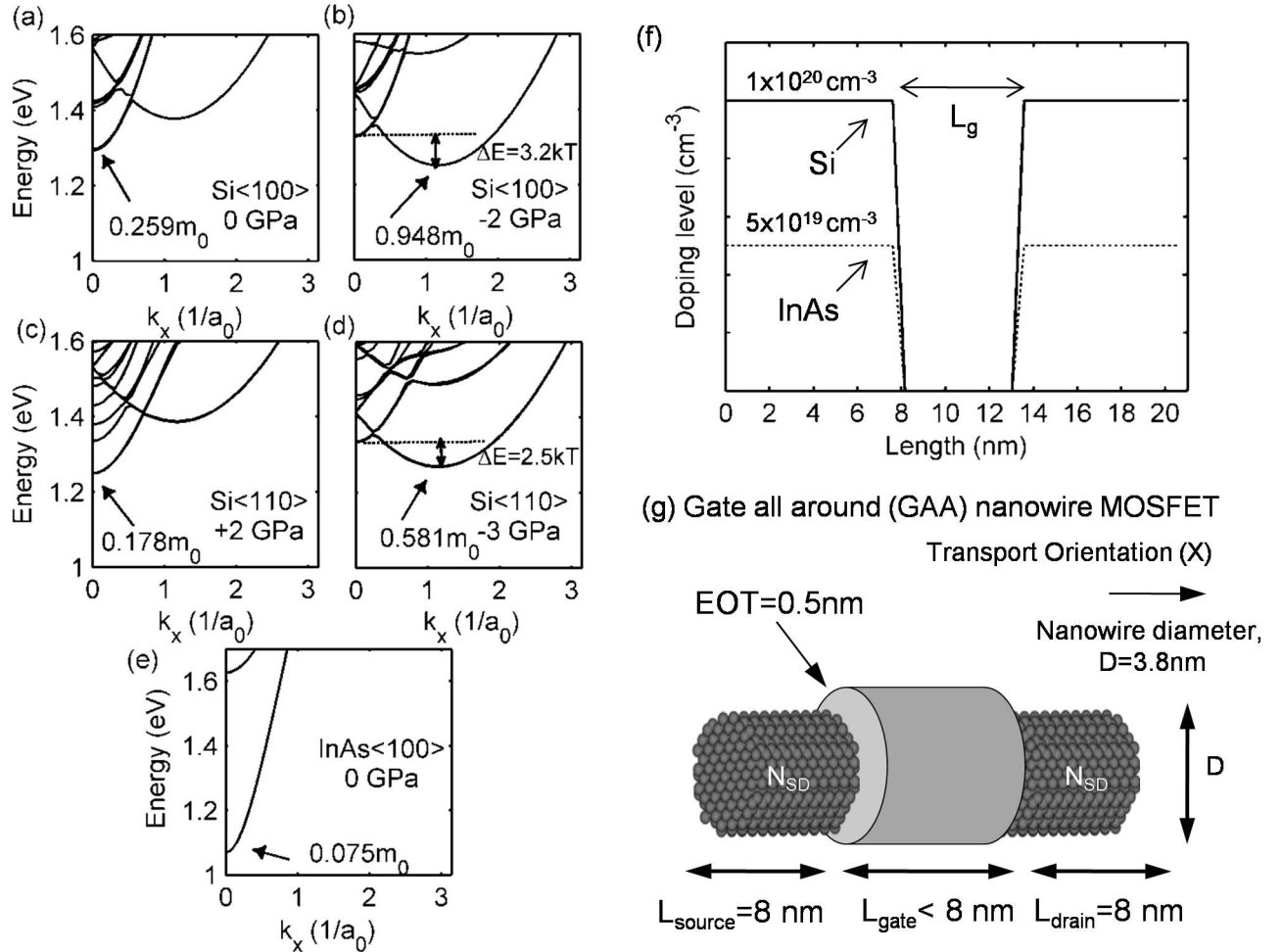

Fig. 2.   Calculated bandstructure for (a) <100> oriented Si, (b) compressively strained <100> oriented Si, (c) tensile strained <110> oriented Si, (d) compressively strained <110> oriented Si, and (e) <100> oriented InAs nanowire with 3.8 nm diameter. (f) Doping profile of Si and InAs nanowire MOSFETs. (g) Schematic view of the simulated device structure.

corresponds to the longitudinal valley mass (m_l) of $\sim 0.91m_o$ in bulk Si. The value of the CB minima is calculated to be $0.948m_o$ as shown in Fig. 2(b) [13], [15].

3) Tensile Stressed Si <110>*:* Fig. 2(c) shows the E-k relation for a tensile stressed <110> oriented Si nanowire. This case is close to current n-MOS technology where tensile

stress is used to reduce CB minima mass and increase the energy difference between the lighter Δ_2 and heavier Δ_4 valleys [1], [12]. The CB minima mass for a $<110>$ oriented nanowire with an applied tensile stress of 2 GPa is calculated to be $0.178m_0$. The calculated CB minima mass is slightly smaller than the expected transverse mass (m_t) of $\sim 0.19m_o$ essentially due to the effect of tensile stress [15].

4) Compressive Stressed Si $<110>$*:* On applying a compressive stress along Si $<110>$ transport direction, heavier Δ_4 valleys are pulled down increasing the CB minima mass. As the stress type is reversed to compressive 3 GPa, the CB minima mass increases to $0.581m_o$ from $0.178m_o$ as shown in Fig. 2(d). The bulk projected CB minima mass in this case can be analytically shown to be equal to $(m_l + m_t)/2$ or $\sim 0.55m_o$, which is close to the calculated value of $0.581m_o$ [13], [15].

5) Unstrained InAs $< 100 >$*:* High-mobility materials like $In_xGa_{1-x}As$ with high in percentage are being actively researched as a post-Si channel material [6]. In light of this fact, a $< 100 >$ oriented InAs channel is also considered in this paper. Fig. 2(e) shows the E-k, with a calculated band edge mass of $0.075m_0$. Due to quantum confinement, the CB minima mass increases significantly from the bulk Γ valley mass of $\sim 0.023\ m_o$ [16].

B. Transport Simulation

Transport simulations are performed using a full-band quantum transport simulator based on the $sp^3d^5s^*$ tight-binding model in the nearest neighbor approximation (without spin-orbit coupling). The atomistic Schrodinger–Poisson equations are solved self-consistently in the nonequilibrium Green function formalism at room temperature [17]–[20]. The electron-phonon scattering is computed in the self-consistent Born approximation that couples the confined electron and phonon spectra [21]. The phonon population has been assumed to be in equilibrium at room temperature. Including the effect of hot phonons can further degrade the performance [22]. The phonon spectra is calculated using a modified Keating model that was benchmarked against bulk phonon dispersion [21]. While calculating the phonon bandstructure the surface atoms are assumed to be free to move. It should be pointed that a different surface boundary condition can lead to a different result [23]. The electron-phonon self energy matrix is further simplified to be local in space because of the heavy computational burden [21]. The dielectric material wrapped around the channel is assumed to have a relative permittivity equal to 3.9 and a thickness of 0.5 nm. This leads to an effective oxide thickness (EOT) of 0.5 nm for all the simulations [2]. It should be pointed out that this represents the best case EOT. A thick, high-K dielectric with EOT = 0.5 nm will have slightly degraded electrostatics [24]. At the same time, a thicker dielectric will also suppress the gate-dielectric leakage current [25]. The dielectric layer is treated as perfect insulator and hard wall boundary conditions are applied to the surface Si or InAs atoms. The gate-dielectric tunneling is not included in our simulations. In light of a recent demonstration of EOT = 0.3 nm, using a material with $K = 40$, the assumptions in this paper can be considered reasonable [25]. A source-drain

doping level of $1 \times 10^{20}/cm^3$ is assumed for Si nanowires while $5 \times 10^{19}/cm^3$ is the doping level for the InAs nanowire. The charge due to the doping concentration is assumed to be uniformly distributed in the source and drain regions. The channel region is assumed to be undoped with an abrupt doping profile as shown in Fig. 2(f).

Nanowire gate all around (GAA) n-MOSFETs are simulated for the five different CB minima mass cases [Figs. 2(a)–(e)] at channel lengths of $L_g = 3$, 5, and 7 nm as shown in Fig. 2(g). The OFF-state current (I_{OFF}) is set to 0.1 $\mu A/\mu m$ ($I_{OFF} = I_{DS}$ at $V_{GS} = 0$ V and $V_{DS} = 0.5$ V), where the current has been normalized by the diameter [2]. Transfer characteristics of the different nanowire MOSFETs are compared at a supply voltage $V_{DS} = 0.5$ V.

III. S-D TUNNELING AND SUBTHRESHOLD CHARACTERISTICS

The S-D tunneling is a quantum mechanical phenomenon that is fundamental and cannot be avoided. Fig. 3 illustrates the OFF-state current profile for the different CB minima cases at $L_g = 5$ nm simulated in the ballistic regime. For the heaviest mass case, it can be seen that most of the current flows over the barrier as opposed to the lightest mass case where most of the current quantum-mechanically tunnels through the barrier. The amount of current flowing below the potential barrier height (E_b) is the tunneling current (I_{DS}^{tunnel}). The ratio of I_{DS}^{tunnel} to the total current I_{DS}^{total} or the tunnel percent increases as the CB minima mass becomes lighter. As a consequence of increased S-D tunneling, to achieve the desired OFF-state current, the barrier height needs to be raised much more for a light transport mass as compared to a heavy transport mass case. This leads to an increased SS in presence of S-D tunneling.

Fig. 4(a) shows the tunnel component (I_{DS}^{tunnel}) along with the current flowing over the barrier or the thermionic component ($I_{DS}^{thermionic}$) during a MOSFET operation. Bias-dependent current components for a light transport mass case (equivalent to Fig. 2(c)) is shown in Fig. 4(b) and for heavy transport mass case (equivalent to Fig. 2(b)) is shown in Fig. 4(c), both at $L_g = 5$ nm. The adverse effect of S-D tunneling in the presence of a light CB minima mass becomes clear as the subthreshold current is totally dominated by I_{DS}^{tunnel}. On the other hand, subthreshold slope is controlled by $I_{DS}^{thermionic}$ current for the heavy CB minima mass case, bringing it closer to the classical MOSFET operation, where the electrostatic gate control determines the subthreshold characteristics.

The calculated subthreshold characteristics for the different CB minima cases at different channel lengths are shown in Fig. 5. The subthreshold slope calculated from $I_{DS}^{thermionic}$ is labeled as $SS^{therm.}$ while SS^{device} is the actual subthreshold slope of the nanowire MOSFET calculated in presence of S-D tunneling. It can be readily observed that for light CB minima mass cases, the $SS^{therm.}$ and SS^{device} show a huge difference. As the CB minima mass increases, the $SS^{therm.}$ and SS^{device} values begin to merge. This can be understood from the fact that with a heavy CB minima mass, the electrostatic gate control determines the subthreshold slope. As the CB
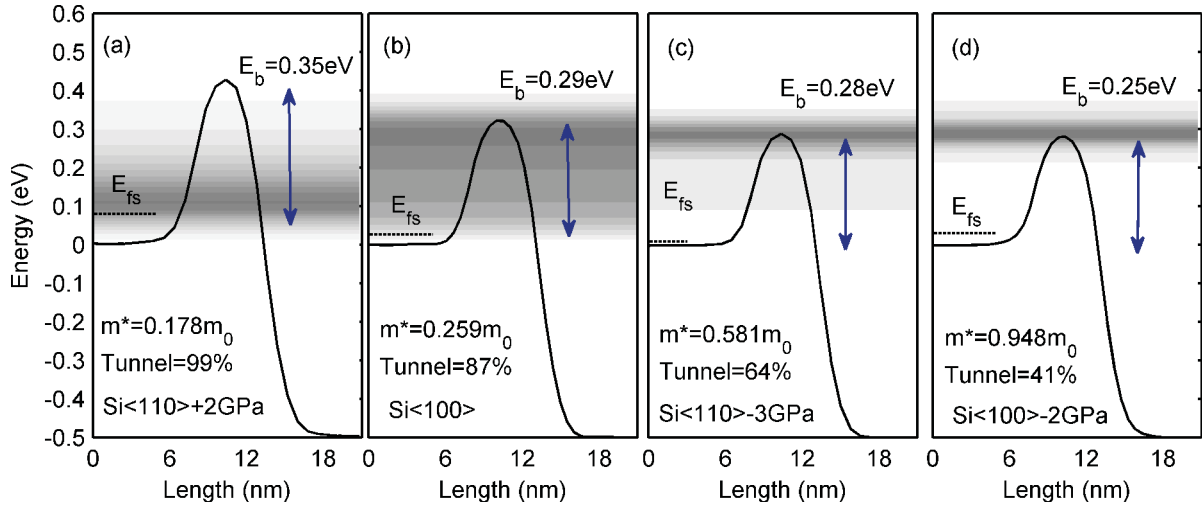
Fig. 3.   Illustration of the leakage current at OFF state ($I_{ds} = 0.1$ μA/μm) at $L_g = 5$ nm. Normalized energy current spectrum is plotted for (a) Si <110> +2 GPa, (b) Si <100>, (c) Si <110> 3 GPa, and (d) Si <100> 2 GPa nanowire cases. Due to S-D tunneling, the barrier height needs to be much higher to achieve the desired I_{OFF}.
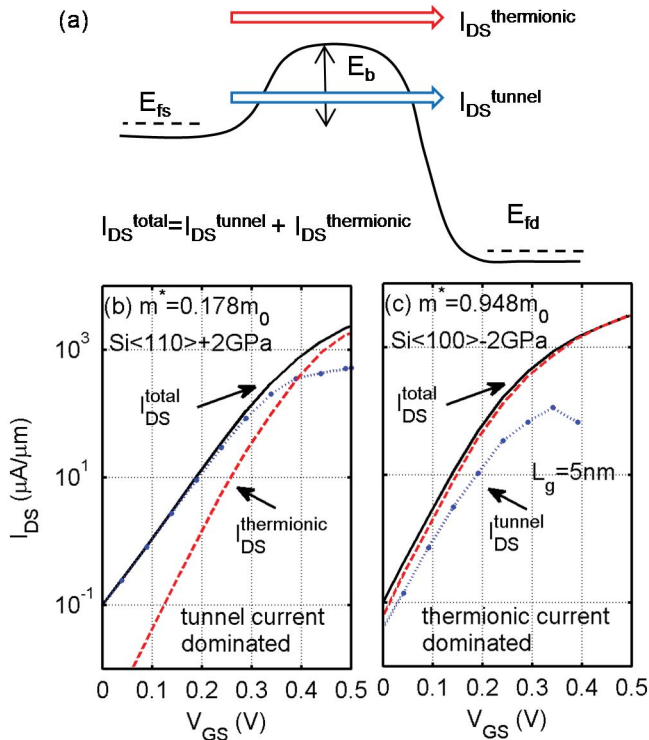

Fig. 4.   Calculated thermionic $I_{DS}^{\text{thermionic}}$ and tunnel component I_{DS}^{tunnel} of the total current I_{DS}^{total} for (a) Si <110> +2 GPa and (b) Si <100> 2GPa nanowire cases.
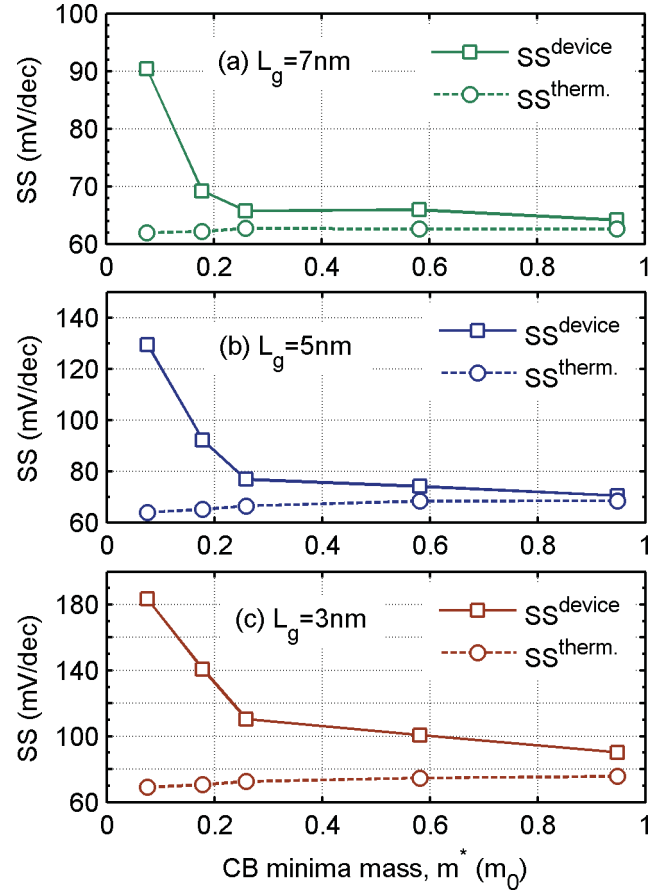

Fig. 5.   Subthreshold slope calculated from the total current (SS$^{\text{device}}$) and the thermionic current component (SS$^{\text{therm.}}$) for the different CB minima nanowire cases at (a) 7 nm, (b) 5 nm, and (c) 3 nm channel lengths.

minima mass becomes lighter, the S-D tunneling component begins to dominate. This fact also underlines another important understanding that the lower limit of SS = 60 mV/dec at room temperature does not hold anymore in presence of S-D tunneling. With the best of gate control, the amount of S-D tunneling will set the lower limit on the achievable SS and that will be more than 60 mV/dec.

It should be noted that for different channel lengths, the SS$^{\text{therm.}}$ is calculated to be $\sim$62 mV/dec at $L_g = 7$ nm to $\sim$75 mV/dec at $L_g = 3$ nm. This fact highlights the strong

electrostatic gate-control that can be achieved using a nanowire geometry. A light transport mass, however, cancels out any advantage because of increased S-D tunneling. This is a crucial understanding that even with the best of gate electrostatics, the so called high-mobility or low-mass materials may fail to perform as channel lengths are scaled to sub-8 nm dimensions.
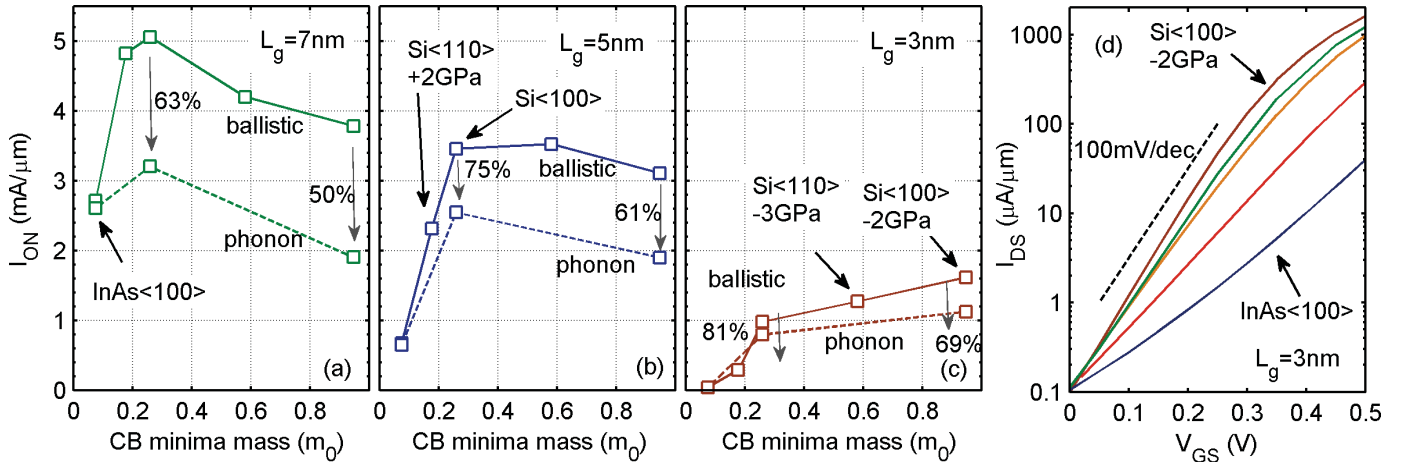
Fig. 6. ON-state currents in ballistic and phonon scattering limited regime for (a) $L_g = 7$ nm, (b) $L_g = 5$ nm, and (c) $L_g = 3$ nm channel lengths. Also, the ballisticity ratio is computed for phonon scattering limited ON-state current values. (d) I_{DS} vs. V_{GS} plot for the different nanowire cases at $L_g = 3$ nm in the ballistic limit.

IV. ON-STATE PERFORMANCE

The calculated ballistic I_{ON} currents ($I_{ON} = I_{DS}$ at $V_{GS} = 0.5$ V and $V_{DS} = 0.5$ V) are plotted in Fig. 6 for the different nanowire cases at different channel lengths. It can be clearly seen that the optimum device performance in the ballistic limit happens at a relatively heavier CB minima mass. This emanates from the tradeoff condition of utilizing a heavy transport mass. A light transport mass (m_t) will lead to a high injection velocity or mobility ($\propto 1/\sqrt{m_t}$). However, at the same time, due to the degraded SS, the threshold voltage increases, reducing the gate-overdrive impacting the final ON-state current. Along the same arguments, a heavy transport mass can lead to gains in term of SS, but the gains do not translate into an improved ON-state performance due to a lower injection velocity. It is also expected for a heavy transport mass to lend some advantage in improving the inversion layer charge because of higher density of states or improved C_q [7]. A proper definiton of the inversion charge, however, becomes a debatable topic at these ultrascaled channel lengths; hence this is not discussed in detail.

It is observed that as the channel length (L_g) is scaled from 7–3 nm [Fig. 6(a)–(c)], the CB minima mass at which the peak performance is obtained also increases. This happens because of degraded SS due to reducing gate control with channel length scaling. This means that an even heavier CB minima mass is required to offset the loss of gate control and to improve device performance. The advantage of a heavy effective mass is highlighted for the shortest channel length of $L_g = 3$ nm . The ON-state current continues to improve monotonically with increasing CB minima mass, owing to improving SS [Fig. 6(d)]. Engineering a channel material with a transport mass heavier than $\sim 0.95\, m_0$ could possibly further enhance the performance at $L_g = 3$ nm.

After computing the $I_{DS} - V_{GS}$ in the ballistic, the ON-state current is recalculated in the presence of electron-phonon scattering [21]. The ON-state current limited by electron-phonon scattering is computed for Si<100> under the condition of no-stress and a compressive uniaxial stress of 2GPa.
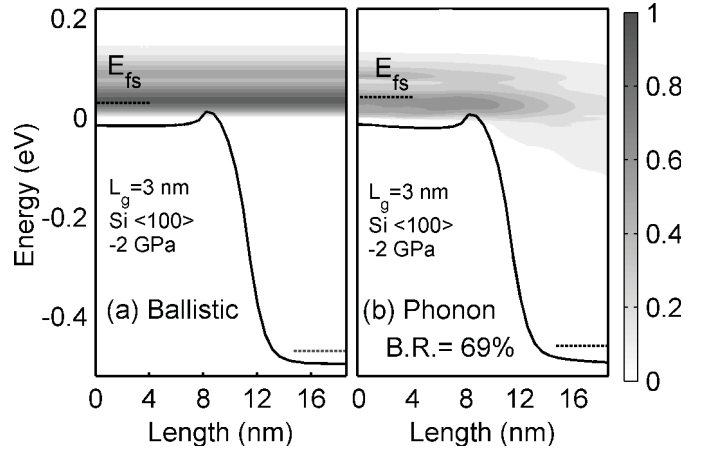

Fig. 7. Normalized energy current spectrum for Si<100> 2 GPa case at $L_g = 3$ nm in (a) ballistic and (b) phonon scattering limited regime at the ON state.

It should be noted Si<100> are also the best performing nanowire cases in the ballistic limit at the different channel lengths. The phonon limited ON current for InAs is assumed to be 96% of the ballistic ON current [26]. Phonon scattering lowers the I_{ON} with Si<100> operating at 63% and compressively stresses Si<100> operating at 50% of the ballistic limit. It is expected for the compressively stressed Si<100> to have a lower ballisticity ratio because of increased density of states for scattering owing to its heavier CB minima mass. However, with reducing channel length, the ballistic ratio (B.R.) improves as the distance over which a carrier can backscatter reduces [27]. At $L_g = 3$ nm, Si<100> begins to operate at 81% while compressively stresses Si<100> operates at nearly 69% of the ballistic limit [Fig. 6(c)].

Interestingly, InAs <100>, which is currently an actively researched material for future MOSFET scaling, and the tensile strained Si <110>, which is the current industry standard, both lag behind in performance at $L_g < 8$ nm.

This is a critical understanding that as the channel lengths scale < 8 nm, we enter a new regime of device operation where the device performance is severely limited by S-D tunneling. However, at the same time, engineering a relatively heavier transport mass can still lead to performance improvements. It is still encouraging to see that the compressively stressed $Si < 100 >$ nanowire with the channel length scaled to 3 nm, even in the presence of phonon scattering, is still able to deliver a respectable $I_{ON}/I_{OFF} > 10^4$ at supply voltage of $V_{DD} = 0.5$ V (Fig. 7).

Although, the ON-state currents are shown to reduce with channel lengths, the design solution to scaling MOSFETs at $L_g < 8$ nm could lie in vertically stacked multiple nanowire MOSFETs that increase the final I_{ON} without compromising on subthreshold characteristics [28].

V. CONCLUSION

In this paper, the deleterious effects of S-D tunneling in nanowire n-MOSFETs at $L_g < 8$ nm were highlighted in realistically gated and extended devices. As S-D tunneling depends on the transport mass, as a first step, the different CB minima masses that can be engineered in Si and InAs were shown. Next, using full-band quantum simulations, based on $sp^3 d^5 s^*$ tight-binding model, the subthreshold and ON-state performances were analyzed. The monotonic improvement in subthreshold slope with heavier CB minima mass was clearly observed as a heavy mass limits S-D tunneling. At the same time, the ON-state performance did not improve monotonically but shows a peak-like nature. This is due to the tradeoff condition that a heavy (or light) mass offers in terms of OFF-state and ON-state properties. The present results showed that the optimal device performance at $L_g < 8$ nm lie in heavier ($> 0.25 m_0$) transport mass channel designs. A realistic scenario of scaling MOSFETs well below $L_g < 8$ nm could lie in channel designs with a heavy transport mass to improve subthreshold characteristics and multiple vertically stacked nanowires to boost the ON-state current.

The effect of surface roughness and random dopant fluctuation has not been taken into account in this paper. The tunneling rate is expected to depend significantly on the variations in the potential barrier caused due to surface roughness or discrete random dopants. Furthermore, trap assisted tunneling due to stray dopant atoms in the channel might further degrade the performance.

REFERENCES

[1] C. Auth, C. Allen, A. Blattner, D. Bergstrom, M. Brazier, M. Bost, M. Buehler, V. Chikarmane, T. Ghani, T. Glassman, R. Grover, W. Han, D. Hanken, M. Hattendorf, P. Hentges, R. Heussner, J. Hicks, D. Ingerly, P. Jain, S. Jaloviar, R. James, D. Jones, J. Jopling, S. Joshi, C. Kenyon, H. Liu, R. McFadden, B. McIntyre, J. Neirynck, C. Parker, L. Pipes, I. Post, S. Pradhan, M. Prince, S. Ramey, T. Reynolds, J. Roesler, J. Sandford, J. Seiple, P. Smith, C. Thomas, D. Towner, T. Troeger, C. Weber, P. Yashar, K. Zawadzki, and K. Mistry, "A 22 nm high performance and low-power CMOS technology featuring fully-depleted trigate transistors, self-aligned contacts and high density MIM capacitors," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 131–132.

[2] (2012, Apr. 10). *International Technology Roadmap for Semiconductors* [Online]. Available: http://www.itrs.net/links/2011itrs/home2011.htm

[3] M. Luisier, M. Lundstrom, D. Antoniadis, and J. Bokor, "Ultimate device scaling: Intrinsic performance comparisons of carbon-based, InGaAs, and Si field-effect transistors for 5 nm gate length," in *Proc. IEDM*, Dec. 2011, pp. 11.2.1–11.2.4.

[4] J. Wang and M. Lundstrom, "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?" in *Proc. IEDM*, 2002, pp. 707–710.

[5] J. Appenzeller, J. Knoch, M. Bjork, H. Riel, H. Schmid, and W. Riess, "Toward nanowire electronics," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 2827–2845, Nov. 2008.

[6] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," *Nature*, vol. 479, pp. 317–323, Nov. 2011.

[7] M. Fischetti, L. Wangt, B. Yut, C. Sachs, P. Asbeck, Y. Taur, and M. Rodwell, "Simulation of electron transport in high-mobility MOSFETs: Density of states bottleneck and source starvation," in *Proc. IEEE IEDM*, Dec. 2007, pp. 109–112.

[8] S. Sylvia, H.-H. Park, M. Khayer, K. Alam, G. Klimeck, and R. Lake, "Material selection for minimizing direct tunneling in nanowire transistors," *IEEE Trans. Electron Devices*, vol. 59, no. 8, pp. 2064–2069, Aug. 2012.

[9] M. Bescond, N. Cavassilas, and M. Lannoo, "Effective-mass approach for n-type semiconductor nanowire MOSFETs arbitrarily oriented," *Nanotechnology*, vol. 18, no. 25, p. 255201, 2007.

[10] P. Solomon, D. Frank, J. Jopling, C. D'Emic, O. Dokumaci, P. Ronsheim, and W. Haensch, "Tunnel current measurements on P/N junction diodes and implications for future device design," in *IEEE IEDM Tech. Dig.*, Dec. 2003, pp. 9.3.1–9.3.4.

[11] T. Yu, R. Wang, R. Huang, J. Chen, J. Zhuge, and Y. Wang, "Investigation of nanowire line-edge roughness in gate-all-around silicon nanowire MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 11, pp. 2864–2871, Nov. 2010.

[12] S. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial-process-induced strained-Si: Extending the CMOS roadmap," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1010–1020, May 2006.

[13] F. Stern and W. Howard, "Properties of semiconductor surface inversion layers in the electric quantum limit," *Phys. Rev.*, vol. 163, no. 3, pp. 816–835, 1967.

[14] Y. Liu, N. Neophytou, T. Low, G. Klimeck, and M. Lundstrom, "A tight-binding study of the ballistic injection velocity for ultrathin-body SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 3, pp. 866–871, Mar. 2008.

[15] J.-L. van der Steen, D. Esseni, P. Palestri, L. Selmi, and R. J. E. Hueting, "Validity of the parabolic effective mass approximation in silicon and germanium n-MOSFETs with different crystal orientations," *IEEE Trans. Electron Devices*, vol. 54, no. 8, pp. 1843–1851, Aug. 2007.

[16] N. Kharche, G. Klimeck, D. Kim, J. A. Del Alamo, and M. Luisier, "Multiscale metrology and optimization of ultra-scaled inas quantum well FETs," *IEEE Trans. Electron Devices*, vol. 58, no. 7, pp. 1963–1971, Jul. 2011.

[17] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the $sp^3 d^5 s^*$ tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B*, vol. 74, no. 20, pp. 205323-1–205323-12, 2006.

[18] T. B. Boykin, G. Klimeck, and F. Oyafuso, "Valence band effective-mass expressions in the $sp^3 d^5 s^*$ empirical tight-binding model applied to a Si and Ge parametrization," *Phys. Rev. B*, vol. 69, pp. 115201-1–115201-10, Mar. 2004.

[19] T. B. Boykin, G. Klimeck, R. C. Bowen, and F. Oyafuso, "Diagonal parameter shifts due to nearest-neighbor displacements in empirical tight-binding theory," *Phys. Rev. B*, vol. 66, no. 12, p. 125207, Sep. 2002.

[20] T. B. Boykin, M. Luisier, M. Salmani-Jelodar, and G. Klimeck, "Strain-induced, off-diagonal, same-atom parameters in empirical tight-binding theory suitable for [110] uniaxial strain applied to a silicon parametrization," *Phys. Rev. B*, vol. 81, p. 125202, Mar. 2010.

[21] M. Luisier and G. Klimeck, "Atomistic full-band simulations of silicon nanowire transistors: Effects of electron-phonon scattering," *Phys. Rev. B*, vol. 80, no. 15, pp. 155430-1–155430-11, 2009.

[22] S. Hasan, M. A. Alam, and M. S. Lundstrom, "Simulation of carbon nanotube FETs including hot-phonon and self-heating effects," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2352–2361, Sep. 2007.

[23] L. Donetti, F. Gámiz, N. Rodriguez, F. Jimenez, and C. Sampedro, "Influence of acoustic phonon confinement on electron mobility in ultrathin silicon on insulator layers," *Appl. Phys. Lett.*, vol. 88, no. 12, pp. 122108-1–122108-3, 2006.

[24] Q. Xie, J. Xu, and Y. Taur, "Review and critique of analytic models of MOSFET short-channel effects in subthreshold," *IEEE Trans. Electron Devices*, vol. 59, no. 6, pp. 1569–1579, Jun. 2012.

[25] Y. Morita, S. Migita, W. Mizubayashi, M. Masahara, and H. Ota, "Two-step annealing effects on ultrathin EOT higher-k (k = 40) ALD-HFO$_2$ gate stacks," in *Proc. Eur. Solid-State Device Res. Conf.*, Sep. 2012, pp. 81–84.

[26] N. Luisier and G. Klimeck, "Phonon-limited mobility and injection velocity in n- and p-doped ultrascaled nanowire field-effect transistors with different crystal orientations," in *Proc. IEEE IEDM*, Dec. 2010, pp. 8.6.1–8.6.4.

[27] C. Jeong, D. Antoniadis, and M. Lundstrom, "On backscattering and mobility in nanoscale silicon MOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 11, pp. 2762–2769, Nov. 2009.

[28] E. Bernard, T. Ernst, B. Guillaumot, N. Vulliet, P. Coronel, T. Skotnicki, S. Deleonibus, and O. Faynot, "Multi-channel field-effect transistor (MCFET)—Part I: Electrical performance and current gain analysis," *IEEE Trans. Electron Devices*, vol. 56, no. 6, pp. 1243–1251, Jun. 2009.

Tillmann Kubis received the Ph.D. degree in physics from the Technical University of Munich, Garching, Germany, in 2009.

His current research interests include the modeling of realistic charge, spin and heat transport in semiconductor nanodevices, and optoelectronics.

Michael Povolotskyi received the the Ph.D. degree in electric engineering from the University of Rome Tor Vergata, Rome, Italy, in 2004.

His current research interests include the modeling of semiconductor nanostructures, devices, and high-power computing.

Saumitra R. Mehrotra (S'10) is currently pursuing the Ph.D. degree in electrical engineering with Purdue University, West Lafayette, IN, USA.

His current research interests include the device physics, modeling and simulation of transport in nanoscale devices.

Mark S. Lundstrom received the Ph.D. degree in electrical engineering from Purdue University, West Lafayette, IN, USA, in 1980.

His current research interests include the physics of small electronic devices, especially nanoscale transistors, on carrier transport in semiconductor devices.

SungGeun Kim (S'10) is currently pursuing the Ph.D. Degree with the School of Electrical and Computer Engineering and Network for Computational Nanotechnology, Purdue University, West Lafayette, IN, USA.

His current research interests include quantum transport in nanoscale electronic devices.

Gerhard Klimeck (S'91–M'95–SM'04–F'13) received the Ph.D. degree from Purdue University, West Lafayette, IN, USA, in 1994.

His current research interests include the modeling of nanoelectronic devices, parallel cluster computing, and genetic algorithms.