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Statistical Study of Deep Submicron Dual-Gated Field-Effect Transistors on Monolayer Chemical Vapor Deposition Molybdenum Disulfide Films

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Statistical Study of Deep Submicron Dual-Gated Field-Effect Transistors on Monolayer Chemical Vapor Deposition Molybdenum Disulfide Films

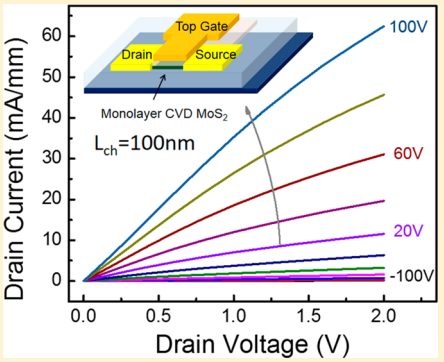
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Supporting Information

ABSTRACT: Monolayer molybdenum disulfide (MoS_2) with a direct band gap of 1.8 eV is a promising two-dimensional material with a potential to surpass graphene in next generation nanoelectronic applications. In this Letter, we synthesize monolayer MoS_2 on Si/SiO_2 substrate via chemical vapor deposition (CVD) method and comprehensively study the device performance based on dual-gated MoS_2 field-effect transistors. Over 100 devices are studied to obtain a statistical description of device performance in CVD MoS_2. We examine and scale down the channel length of the transistors to 100 nm and achieve record high drain current of 62.5 mA/mm in CVD monolayer MoS_2 film ever reported. We further extract the intrinsic contact resistance of low work function metal Ti on monolayer CVD MoS_2 with an expectation value of 175 Ω·mm, which can be significantly decreased to 10 Ω·mm by appropriate gating. Finally, field-effect mobilities (μ_{FE}) of the carriers at various channel lengths are obtained. By taking the impact of contact resistance into account, an average and maximum intrinsic μ_{FE} is estimated to be 13.0 and 21.6 $cm^2/(V\ s)$ in monolayer CVD MoS_2 films, respectively.



KEYWORDS: *Monolayer MoS_2, CVD, transistors, drain current, contact resistance, field-effect mobility*

Two-dimensional (2D) layered crystals have attracted great attention since the advent of graphene.[1−6] These materials are made of individual layers bonded by van der Waals forces and can be easily exfoliated to obtain atomically thin crystals.[7] Despite its ultrahigh charge carrier mobility due to its linear energy dispersion in momentum space, graphene's gapless electronic structure restrains its applications in digital circuits.[8] In comparison, some members of transition metal dichalcogenides (TMDs), another family of layered materials, provide semiconducting substitutes to graphene. Bulk MoS_2 with an indirect band gap of 1.2 eV and a direct band gap of 1.8 eV in monolayers is a promising member of this group.[9] Applications such as field-effect transistors, chemical sensors, photonic detectors, and integrated circuits have been explored.[10−14] These studies were mostly done on single or multilayer MoS_2 flakes peeled from bulk via scotch tape technique.[7] Though mechanical exfoliation offers an easy and feasible way to obtain MoS_2 thin flakes with various thicknesses for fundamental research, the low yield and nonuniformity limits its practical applications.

Chemical vapor deposition (CVD) has been proved to be a good method for 2D crystal growth. Typically, this synthetic route provides a low cost path to high-quality, large-area and thin films. A variety of 2D crystals, such as graphene, boron nitride, topological insulators, and MoS_2 have been successfully synthesized by CVD methods.[15−17] The early attempts to obtain large area MoS_2 have relied on the solid state sulfurization of molybdenum and molybdenum compounds, such as $(NH_4)_2MoS_4$.[18,19] However, they suffer from nonuniformity in thickness, small grain-sizes, and difficulty in precursor preparation. In addition, the reported lower charge carrier mobility in these CVD films is not favorable for device applications. Additionally, the sulfurization of MoO_3 has been comprehensively studied and is a main approach in MoS_2 synthesis, as MoO_3 has a lower melting and evaporation temperature. Several studies have shown the feasibility of CVD MoS_2 synthesis from sulfurization of MoO_3 on Si/SiO_2 or sapphire.[20,21] However, the electrical properties of these CVD films have not been comprehensively studied. In this work, highly crystalline monolayer MoS_2 crystals were obtained from a CVD-based procedure on which we fabricated over 100 transistors with channel lengths scaled down to deep submicrometer region. Previous studies on MoS_2 transistors and other devices were mostly done with the exfoliated single

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crystals. This gives a glimpse of the transport properties of MoS_2 and device characteristics, however, due to a large flake to flake variation, they suffer from a large performance deviation. In order to solve this issue, we introduce a statistical study in this work by quantitatively measuring a large number of transistors. From the statistical view, we are able to unveil the fundamental properties of this novel electronic material and show the average values, distributions, and maximum values of the material and devices, including on-current, field-effect mobility, contact resistance, and so forth. These parameters reflect the general information about the carrier transport of the synthesized material, the uniformity of the material, as well as the best device performance. The information is equally important for the understanding of the potential and limitation of CVD MoS_2 films and transistors.

The synthesis of MoS_2 thin films was carried out in a vapor phase deposition process. As shown in Figure 1a, the precursors, MoO_3 nanoribbons, and sublimated sulfur were placed separately in a quartz tube. MoO_3-covered silicon substrates, along with several clean substrates designated for the growth of MoS_2, were placed close to each other at the center of the furnace, flushed with nitrogen at a constant flow of 200 sccm. Clean heavily doped silicon substrates coated with 285 nm of SiO_2 were used, which also facilitate the direct device fabrication. A container with 0.8−1.2 g of sublimated sulfur was placed at a location reaching an approximate maximum temperature of 600 °C at the opening of the furnace. The center of the furnace was gradually heated from room temperature to 550 °C at a ramping rate of ∼20 °C/min. At 550 °C, the sulfur slowly evaporated and the chamber was then heated to 850 °C at a slower ramping rate of ∼5 °C/min. The temperature of chamber was then maintained at this temperature for 10−15 min, and then the chamber was naturally cooled back to room temperature. The chamber pressure and the closely related sulfur concentration in the chamber were monitored using the guidelines described in ref 21 to optimize the growth of large triangular single crystals. These materials are convenient for device fabrication and allow us to avoid complexities in transport caused by grain boundaries. A more detailed description of the synthesis process and growth kinetics can be found in our previous work.[21] Figure 1b represents an image of these single crystalline monolayer MoS_2 samples under optical microscope. Typical triangular domain side lengths vary between 10 to 20 μm. The atomic force microscope (AFM) image of the CVD MoS_2 is shown in Figure 1c. The thickness of the flake is measured to be 0.85 nm, showing monolayer MoS_2 with a good thickness uniformity.

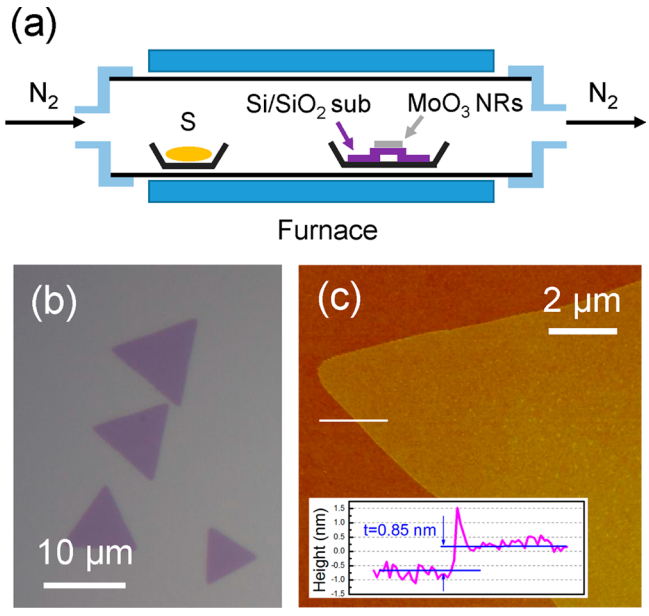


Figure 1. (a) Schematic view of CVD synthesis of monolayer MoS_2 in a furnace. (b) Optical micrograph of single crystalline monolayer CVD MoS_2. Scale bar is 10 μm. (c) AFM image of a synthesized MoS_2 crystal showing good single layer thickness uniformity. Scale bar is 2 μm.

The monolayer CVD MoS_2 samples were then used for device fabrication. To start, source/drain regions were defined by e-beam lithography. The contact width of source and drain was 2 μm. The source and drain spacing, or the channel lengths, were chosen as 100, 200, 500 nm, and 1 μm so that they cover the ranges from long channel to short channel. Ti/Au of 20/60 nm was then deposited by e-beam evaporator as the metal contacts. After the lift-off process, a 0.8−1 nm Al seeding layer was deposited at the rate of 0.1 Å/s on the whole sample to facilitate dielectric growth.[22−24] The samples were then aged overnight in atmosphere to secure a complete oxidation of ∼1 nm Al_2O_3 as the seeding layer. After that, a 15 nm Al_2O_3 was deposited by atomic layer deposition (ALD) at 200 °C using trimethylaluminum (TMA) and water. Pulse times were 0.8 and 1.2 s for TMA and water, and purge times were 6 and 8 s, respectively. Previously, we had a temperature-dependent study on direct ALD growth on 2D crystals.[22] However, we noticed that the insertion of the seeding layer would significantly enhance the yield of devices and minimize the leakage currents. The AFM images of Al_2O_3 growth on monolayer CVD MoS_2 crystals are shown in Supporting Information Figure S1. Finally, the top gate regions were defined by e-beam lithography again. The length of the top gate was chosen to be similar to the channel length, that is, $L_g = L_{ch}$, which reduces the access resistance of the top-gated devices. E-beam evaporated Ni/Au of 20/60 nm was deposited as the top gate metal. A total of 120 devices were fabricated and a statistical study of their transport properties was performed using a Keithley 4200 Semiconductor Characterization Systems.

Figure 2a shows a schematic configuration of the device structures and the dual-gated MoS_2 field-effect transistors. Heavily doped silicon and 285 nm SiO_2 serve as the back gate and gate dielectric, while Ni/Au and 16 nm Al_2O_3 serve as the top gate and gate dielectric materials. By using the dual-gate structure, carrier density in the channel can be modulated by either gate. Figure 2b shows typical output characteristics of a 100 nm channel length device from back-gate modulation. The top-gate is grounded during the measurement to eliminate the capacitance coupling effect. The linear current−voltage relationship at low drain bias indicates good "ohmic" contact at source/drain regions. At 2 V drain voltage, we achieve the highest drain current of 62.5 mA/mm at 100 V back gate voltage, which is equivalent to a vertical field of 3.5 MV/cm. To our best knowledge, this is the highest drain current for CVD MoS_2 based transistors ever reported.[25] However, suffering from the thick back gate dielectric and a large interface trap density ($\sim 1.6 \times 10^{13}$ /cm^2·eV) at the SiO_2/MoS_2 interface, the transconductance is only 0.83 mS/mm. A full scale characterization and the estimation of interface trap density are described in the Supporting Information and Figure S2. The higher interface trap density than devices based on exfoliated

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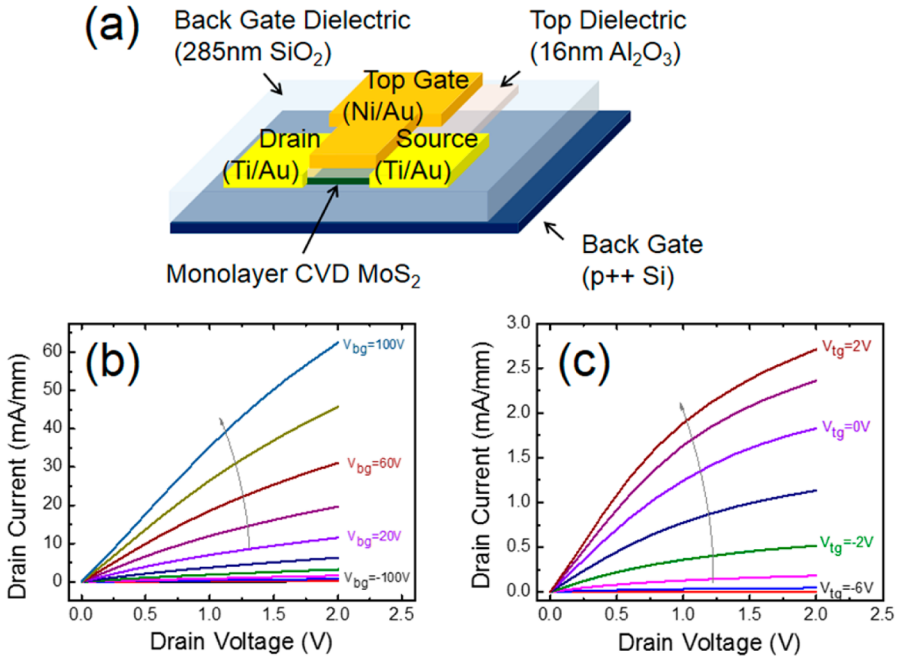


Figure 2. (a) Schematic view of a dual-gate field-effect transistor based on monolayer CVD MoS_2. Heavily doped Si and 285 nm SiO_2 are used as back-gate and dielectric; Ni/Au and 16 nm Al_2O_3 are used as top gate and dielectric. Ti/Au are the contacts for both source and drain. (b) Output curves for a 100 nm channel length device under different back-gate bias showing maximum drain current to be over 60 mA/mm. (c) Output curves of a 1 μm channel length device under top-gate bias.

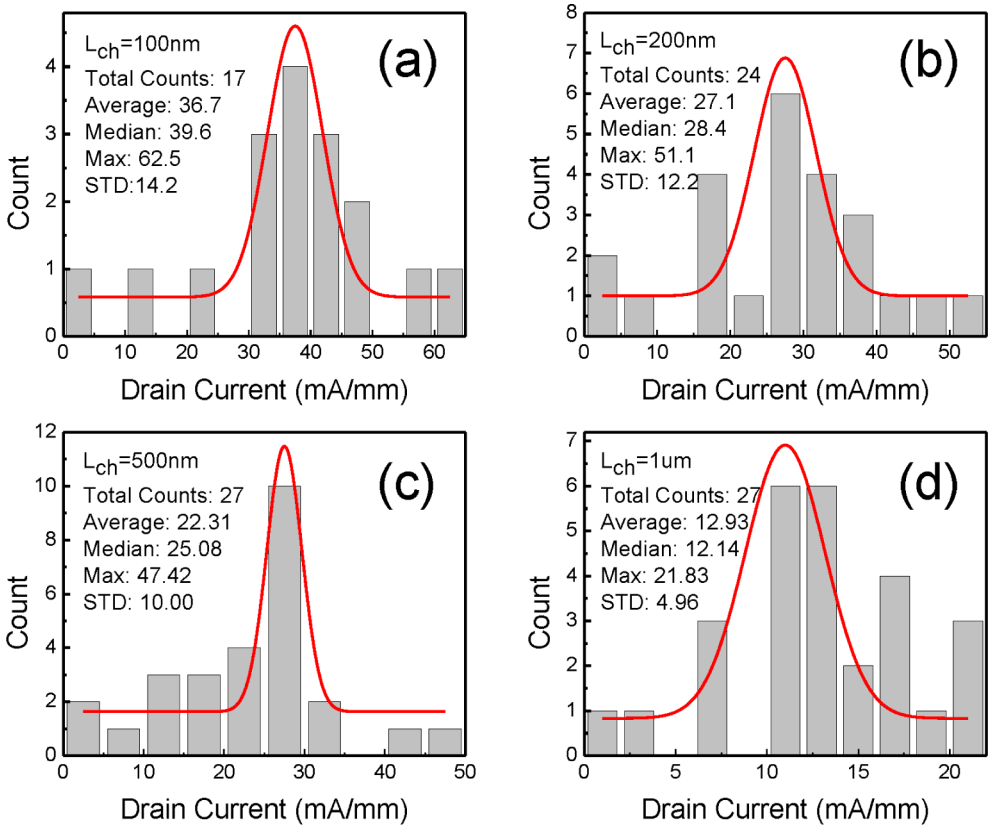


Figure 3. Maximum drain current distributions of (a) 100 nm, (b) 200 nm, (c) 500 nm, and (d) 1 μm devices extracted from back-gate modulation. Average values of 36.7 ± 14.2, 27.1 ± 12.2, 22.3 ± 10.0, and 12.9 ± 5.0 mA/mm for 100 nm, 200 nm, 500 nm, and 1 μm channel lengths are acquired, respectively.

samples is possibly introduced from the synthesis process.[5,10,12] In our material growth, due to the absence of proper seeding particles, the as-grown MoS_2 films are randomly bonded with the amorphous SiO_2 substrate.[26] This not only results in

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difficulty in film transfer to other substrates but also resulting in a large interface trap density. This significantly jeopardizes the interface quality between the semiconducting 2D crystal and dielectric and possible transport mobility. Previous optimism on interface properties due to the nature of 2D crystal without dangling bonds needs to be investigated experimentally. With a better control of interface quality, an enhanced switching behavior in transistors can be expected. Remarkably, unlike transistors based on bulk semiconductors, which have only one semiconductor-to-oxide interface, the transistor based on layered semiconductors has two: one with top dielectric and the other with the substrate. The environment with two interfaces separated by an atomic layer thick semiconductor is expected to impose a strong impact to transport properties of MoS_2. We also notice the big difference between top-gate and back-gate modulations in the same dual-gate device here. The family of output curves of a top-gated device is shown in Figure 2c. During this measurement, the back-gate is grounded.[27] Channel length of this device is 1 μm. Long-channel device is compared here where the device is operated in the diffusive regime and carrier velocity saturation can be ignored so that we can neglect the nonideal factors. We achieve the highest on-current of 2.71 mA/mm only for the top-gate modulation where top gate bias and drain bias are 2 V. The highest drain current of this device under the same 2 V drain bias at 100 V back-gate bias is 14.9 mA/mm, 5 times larger than the drain current from top-gating. Since the channel region is fully gated by either top or back gates, this current difference is mostly originated from the variance in contact resistance. For back-gated devices, the carrier density in MoS_2 under source/drain metal contacts will be increased at higher positive gate bias. Since the source/drain regions are not heavily doped, as in conventional semiconductors, the contact resistance is mainly determined by the effective Schottky barrier height at metal/semiconductor interface.[28,29] With large gate bias, the conduction band bends downward at the metal/semiconductor interface to enhance tunneling current thus reduce contact resistance. Therefore, it facilitates carrier injection from metal contacts to MoS_2. It also can be easily understood by electrostatic doping of MoS_2 underneath source/drain contacts to reduce contact resistance with positive back-gate bias. On the contrary, the top gate has no effect on the carrier density of MoS_2 under the source/drain thus the contact resistance remains constant even at large positive bias. The contact resistance issue would be further discussed in later parts.

Compared to molecular beam epitaxial (MBE) grown crystals, devices made on CVD samples are usually with larger performance variance. Usually, CVD samples have small domain size, random crystal orientation, the existence of grain boundaries and large defect density. These nonideal phenomena have been observed in both graphene and MoS_2 CVD films.[21,30] Therefore, a statistical study of the key parameters of devices is necessary in order to gain a comprehensive understanding of the electrical properties of the CVD grown samples. Figure 3a–d shows the distributions of the maximum drain currents at different channel lengths. All values are extracted at 2 V drain bias and back-gate voltage of 100 V. The variance in device threshold voltages is ignored in the context of this statistical study. A total of 17–27 devices are studied for each channel length. As expected, these figures show a broad distribution for the maximum drain current at all channel lengths. This can be attributed to the nonuniformity of material synthesis and device fabrication; however they show a normal distribution in all sets of data. The average and standard deviation of the measured drain currents are 36.7 ± 14.2, 27.1 ± 12.2, 22.3 ± 10.0, and 12.9 ± 5.0 mA/mm for 100, 200, 500 nm and 1 μm channel lengths, respectively. The channel-length dependent average value with standard deviation and the maximum value measured are plotted in Figure 4. From long

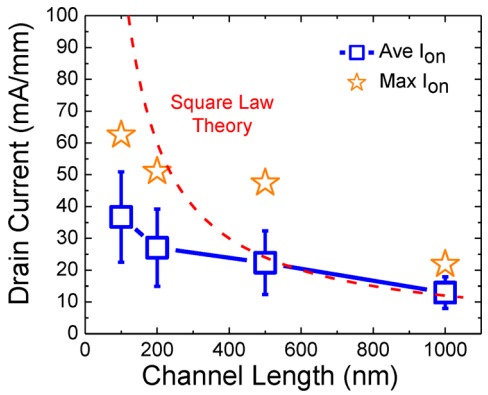


Figure 4. Averaged values of maximum drain current at all channel lengths. Maximum values in measurement are also plotted. Red dashed line shows Square Law Model prediction of channel length-dependent drain current that fits long channel device performance. The deviation at short channel regions is due to contact resistance and velocity saturation.

channel to short channel devices, the increase in drain current indicates the scaling properties in CVD MoS_2 transistors. If we assume the carriers follow the diffusive transport in all channel lengths, the saturated drain current exhibits $I_{ds,sat} = (1/2)\mu_{FE}C_{ox}(W/L)(V_{gs} - V_{th})^2$ by Square Law Theory, where μ_{FE} is the field-effect mobility, C_{ox} is the gate oxide capacitance, W and L are the width and length of the channel, and V_{gs} and V_{th} are the gate bias and threshold voltage.[31] This shows that drain current is inversely proportional to the channel length, and this trend is drawn by the red dashed line in Figure 4. The deviation of drain current at shorter channel lengths is associated with two factors. One is that contact resistance does not scale with channel length, and the impact of this factor is magnified in transistors with ultrathin body semiconductor due to the larger contact resistance.[28] Another reason is the velocity saturation in CVD MoS_2 transistors, where carriers have been approaching the maximum drift velocity in short channel devices, as observed in most conventional semiconductor transistors.

As we have stated before, the major issue for 2D semiconductor based transistors is the existence of a large contact resistance (R_c), which drastically restrains the drain current.[29] The fundamental reason for the large R_c is that the Fermi level pinning at the metal/semiconductor interface that results in a notable Schottky barrier height. However, their atomically thin body makes it difficult for the realization of source/drain engineering such as ion implantation, as a common approach to dope the source/drain regions and reduce contact resistance in traditional semiconductor devices. Thus, it is important to study the contact properties, especially in transistors based on monolayer MoS_2. Here, we develop a simple and effective method to extract the intrinsic contact resistance, or the contact resistance without electrostatic doping, in CVD MoS_2 transistors. The total resistance of the transistor, R_{tot}, is the sum of the contact resistance and channel

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resistance, that is, $R_{tot} = 2R_c + R_{ch}$. Here $2R_c$ represents the contact resistance of both source and drain leads. For each dual-gated device, the on-current from back-gate modulation and top-gate modulation is very different, even though they cover the same area of channel region. This is mostly due to the difference in contact resistance. The global back gate is able to modulate the carrier density of MoS_2 under source/drain metal contacts, thus reducing the contact resistance by electrostatic doping. However, this effect from top gate is screened by source/drain contact metals thus the carrier density in MoS_2 at source/drain regions and the contact resistance remain constant during top-gate sweeping. The observed current ratio between back-gate and top-gate modulation is around 10 (see Supporting Information Figure S3). This means that for top-gate modulation, the contact resistance is over 10 times larger than the channel resistance, that is, $2R_c \gg R_{ch}$. Statistical values and detailed calculations are provided in Supporting Information and Figure S3. This clearly explains a quick saturation in transfer curves of top-gated devices shown in the inset of Figure 5. In top-gated devices, R_c is fixed at a large and

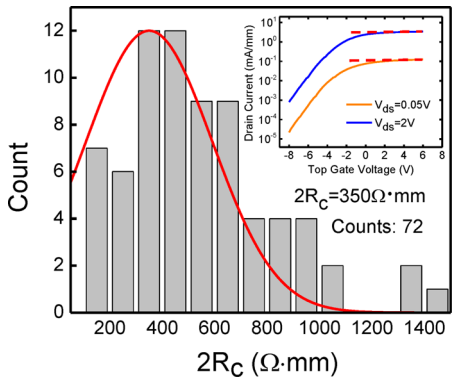


Figure 5. Intrinsic contact resistance distributions in all top-gated devices. An expectation of 350 Ω·mm is predicted by normal distribution. Inset: Typical transfer curves from a top-gated device showing early current saturation.

constant value; once the R_{ch} is much smaller than $2R_c$ during top-gate sweep, R_{tot} does not change much anymore even if we increase the top-gate bias. Beyond this point, we can assume $R_{tot} \approx 2R_c$. We extract the total resistance in all top-gated devices and plot the distributions in Figure 5. We achieve the expectation value of $2R_c$ to be about 350 Ω·mm at zero back-gate bias or without electrostatic doping from back-gate. This huge number is almost two to three orders larger than the desired value in conventional semiconductor devices. Besides the Schottky barrier issue stated before, the single layer nature also has a remarkable contribution to the large contact resistance. Previous study about metal contacts on graphene has revealed that the contact resistivity (ρ_c) is determined by contact width instead of the contact area, that is, $\rho_c = R_cW$.[32] This means that in the case of graphene, the current flows mainly along the edge of the graphene/metal contact. In other words, the current crowding takes place at the edge of the contact metal. We believe this also applies to monolayer MoS_2 since it is more resistive with lower mobility than graphene. The contact resistance R_c could be reduced to 10 Ω·mm at 100 V back-gate bias, which would be discussed in later parts. The consequence of the large contact resistance can be reflected in two ways. First, the on-current is significantly limited, and this effect is significantly magnified for short channel devices, where the portion of channel resistance over total resistance shrinks with scaling down. On the other hand, large transfer length is expected, which barricades high-density device integration. Although the contact resistance can be greatly decreased by applying a large bias on the global back gate, it is not a practical method for real device applications. Previous studies have proposed different approaches to realize doping on 2D semiconductors, such as gaseous and potassium doping.[6,33] However, these methods could be hard to be implemented in real integrated circuits. We are still on the way to work for better solutions, such as formation of MoS_2 based alloy, or contact engineering for Fermi-level depinning at metal to 2D semiconductor interface. This is possible from fundamental physics due to a reduced material dimension and a perfect 2D surface without the termination of a periodic crystal structure.[34] It also requires for defect-free material to eliminate disorder induced gap-states, which has been recognized as a major factor to cause Fermi-level pinning.[35] It is obvious that transport mobility and contact study provides the right information on defect level in CVD MoS_2 films. A comprehensive study on the metal/monolayer MoS_2 contact is required in the future to elucidate these issues.

Next, we study the carrier mobility in monolayer CVD MoS_2 field-effect transistors. In classical theories, the carrier mobility in the bulk and at the interface is different, thus the field-effect mobility is dependent on the gate voltage, which can be written as $\mu_{FE} = (\mu_{FE}^0)/(1 + \theta(V_{gs} - V_{th}))$, where μ_{FE}^0 and θ are two constants. Since increasing the gate bias would push the carriers to the boundary of semiconductor and gate oxide, the carrier mobility would be lowered due to surface scattering. However, in our case the channel material is only atomic layer thick and this effect would have a much smaller impact, hence we assume the mobility is nearly a constant value during gate sweep or $\theta = 0$. As a common approach, the field-effect mobility is extracted from the maximum transconductance on the transfer characteristics, which follows $g_m = (\partial I_{ds})/(\partial V_{gs}) = \mu_{FE}C_{ox}(W/L)V_{ds}$. Field-effect mobility at various lengths is calculated and the distributions are plotted in Figure 6a–d. We achieve the average values of extrinsic field-effect mobility to be 2.67 ± 0.91, 4.58 ± 1.71, 8.52 ± 2.97, and 10.52 ± 3.41 $cm^2/V{\cdot}s$ for 100 nm, 200 nm, 500 nm, and 1 μm channel lengths, respectively. The decrease in mobility at shorter channel lengths is mostly because we assume the drift velocity v_d increases linearly with drain bias by applying $v_d = -\mu E$ this equation. However, because of velocity saturation the product of carrier mobility and lateral electric field is fixed at a constant number. The electric field in the channel increases with channel length down scaling, thus the calculated mobility decreases. This is consistent with our observation of drain current saturation even when we push the channel length to smaller values.

Finally, we estimate the intrinsic carrier mobility in monolayer CVD MoS_2 transistors by subtracting the influence of the significant contact resistance. Because of the large contact resistance we have stated, the intrinsic mobility could be very different from the extrinsic values. Therefore, it is necessary to give a reasonable estimation of the contact resistance under gate bias and correctly estimate the intrinsic field-effect mobility. The back-gated maximum transconductance achieved in our measurement range is at 100 V gate bias. We assume there is no velocity saturation in devices channel length of 500 nm or above so as to ignore the difference in mobility between 500 nm and 1 μm channel length devices. For back-gated

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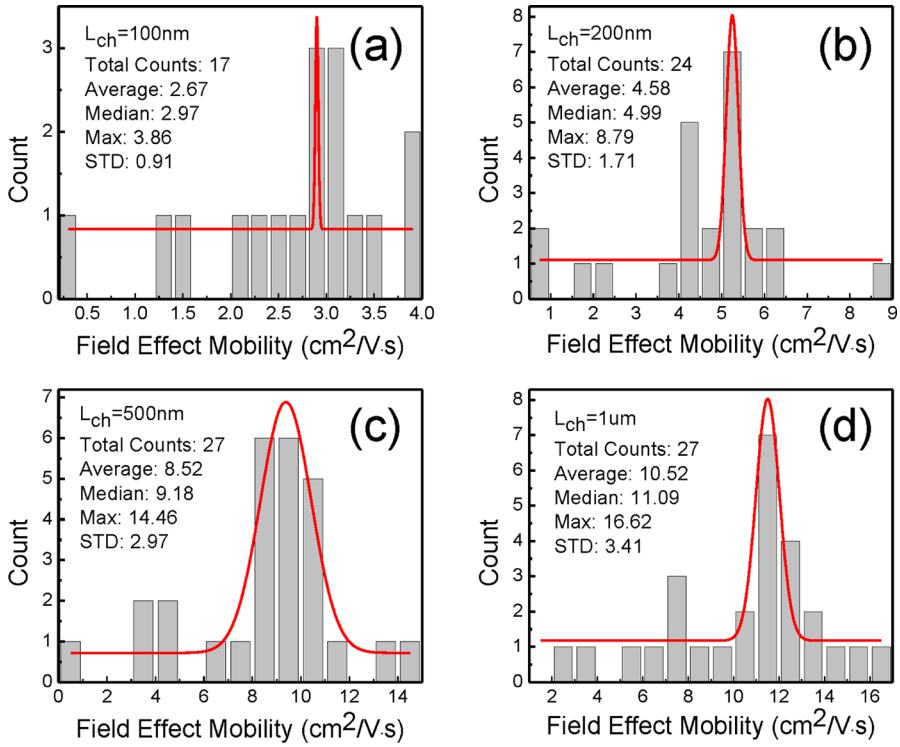


Figure 6. Extrinsic field-effect mobility distributions of (a) 100 nm, (b) 200 nm, (c) 500 nm, and (d) 1 μm devices from back-gate modulation. Carrier mobilities are extracted from transconductance at low drain bias (V_{ds} = 0.05 V). Average values of 2.67 ± 0.91, 4.58 ± 1.71, 8.52 ± 2.97, and 10.52 ± 3.41 cm^2/V·s for 100 nm, 200 nm, 500 nm, and 1 μm channel length are calculated.

devices, the contact resistance is a function of gate bias, and the channel resistance is a function of both gate bias and channel length, that is, $R_{tot} = 2R_c(V_{gs}) + R_{ch}(V_g,L)$. Because $R_{ch}(V_{gs},L)|_{L=1\mu m} \approx 2R_{ch}(V_{gs},L)|_{L=500nm}$ at fixed V_{gs}, therefore R_c can be extracted at a certain V_{gs}. A detailed statistical estimation of the R_c is provided in the Supporting Information. By applying this method, we get an expectation value of $2R_c$ to be 20 Ω·mm. Therefore, the intrinsic carrier mobility is estimated by dividing the ratio between total resistances over channel resistance, that is, $\mu' = \mu(R_{ch}/R_{tot})^{-1} = \mu\{1 - [(2R_c)/(R_{tot})]\}^{-1}$. We get averaged values of 6.11 ± 2.07, 7.72 ± 2.89, 12.59 ± 4.38 and 13.02 ± 4.22 cm^2/V·s for 100 nm, 200 nm, 500 nm, and 1 μm channel length and a maximum value of ~21.6 cm^2/V·s at long channel regions of the CVD monolayer MoS_2 transistors, as plotted in Figure 7. These mobility values provide the low limit for our CVD MoS_2 films. The significant interface trap density, which degrades the measured g_m, has not been considered in this estimation.

In summary, we have synthesized monolayer MoS_2 films by CVD method and have statistically studied their electrical properties. Devices with channel length down to deep submicron region were fabricated. We achieve a maximum drain current of 62.5 mA/mm at 2 V drain bias for 100 nm channel length device. We also revealed the existence of large contact resistance for metal contacts on CVD monolayer MoS_2 films up to R_c = 175 Ω·mm, which could be reduced to 10 Ω·mm under 3.5 MV/cm vertical field. We also extract the field-effect mobility and acquire its intrinsic values by subtracting the contact resistance. The maximum value of intrinsic field effect mobility in CVD monolayer MoS_2 is calculated to be 21.6 cm^2/V·s. We demonstrate the importance to understand metal/MoS_2 interface and significantly reduce the contact resistance for the real device applications of CVD MoS_2 films.

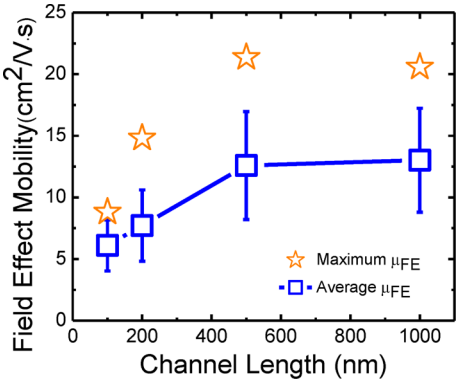


Figure 7. Average and maximum values of intrinsic carrier mobility at all channel lengths. The impact of contact resistance is subtracted from the data. The maximum values are 8.8, 14.8, 21.4, and 20.6 cm^2/V·s for 100 nm, 200 nm, 500 nm, and 1 μm channel length devices.

■ ASSOCIATED CONTENT

Supporting Information

AFM images of ALD integration on monolayer CVD MoS_2 with and without Al seeding layers (Figure S1), device performance from top-gate modulation and back-gate modulation on the same device (Figure S2), method of estimating intrinsic contact resistance and distributions (Figure S3), method of estimating contact resistance under gate bias (Figure S4), and method for mobility correction (Figure S5) are provided. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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