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Utilizing the Unique Properties of Nanowire MOSFETs for RF Applications

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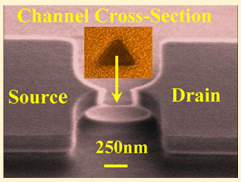
ABSTRACT: Nanostructures have attracted a great deal of attention because of their potential usefulness for high density applications. More importantly, they offer excellent avenues for improved scaling beyond conventional approaches. Less attention has been paid to their intrinsic potential for distinct circuit applications. Here we discuss how a combination of 1-D transport, operation in the quantum capacitance limit, and ballistic transport can be utilized for certain RF applications. In particular this work explores how the above transport properties can provide a high degree of transconductance linearity at the device level. The article also discusses how device characteristics can be interpreted and analyzed in terms of device linearity if the above conditions are not ideally fulfilled. Using aggressively scaled silicon nanowire field-effect transistors as an example device in this work provides new insights toward the proper choice of channel material to improve linearity through the above-mentioned transport conditions. According to this study, a high degree of linearity occurs feasible while operating at low supply voltages making low-dimensional systems, and here in particular nanowires, an interesting candidate for portable RF applications.



KEYWORDS: *Ballistic transport, linearity, nanowire transistor, 1-D transport, quantum capacitance, RF CMOS, transconductance*

In recent years, the rapid transition of the communication systems toward wireless technologies resulted in operation of numerous standards within a small frequency window. More traffic, in adjacent frequency ranges, requires complex circuit and system level linearization techniques to prevent intermodulation and harmonic distortion.[1−5] These constraints turn more focus toward the improvement of linearity at the device level.[6−12] If high transconductance can be achieved in a field-effect transistor, which offers high linearity at the same time, simpler circuit design solutions and lower power consumption are achievable at the same performance specs. This is in line with goals for future generations of wireless and mobile communication systems in which high linearity performance and low power consumption are the key requirements. Recently we discussed the possibility of employing nanostructures to achieve improved linearity in devices with small transconductance variations in the on-state.[13] If three criteria: (i) operation in the quantum capacitance limit (QCL), (ii) one-dimensional (1-D) transport, and (iii) operation in the ballistic transport regime are met, a FET will exhibit ideal linear I_d−V_{ds} characteristics with a constant transconductance which is independent of the actual choice of channel material when operated under high enough drain voltage conditions. These three conditions ensure that: (i) both the conduction and valence band in the gated region of the device follow the applied gate voltage one-to-one (1:1) even in the on-state of the device. Different from a conventional metal−oxide−semiconductor field-effect transistor (MOSFET) where the entire voltage drop is assumed to occur across the gate oxide above threshold, operation in the QCL implies that the gate oxide capacitance C_{OX} is much larger than the so-called quantum capacitance C_Q[14] and the voltage drop across the gate oxide becomes negligible; (ii) only one 1-D mode contributes to the current flow, which ensures that the product of density of states and group velocity[15] cancels out; and (iii) velocity in the channel is determined by the energy dispersion $E(k)$ and that the transmission probability is unity. Under these conditions one can show that eq 1[6,16] holds true in the saturation region of the I_d−V_{ds} characteristics.

$$I_d = \frac{2q^2}{h}(V_{gs} - V_{th}) \tag{1}$$

Note that I_d is independent of V_{ds} in the saturation regime of this ideal device, corresponding to a drain conductance (g_d) of zero. Unlike the conventional RF systems in which sufficiently high supply voltages are needed to improve linearity, operation under the bias and transport conditions discussed here improves linearity at very low supply voltages. This article discusses how a nonideal device, one that approaches but does not perfectly fulfill criteria (i) through (iii), can be analyzed in terms of its linearity performance. Using experiments on silicon devices with small channel diameters (to provide 1-D confinement) and associated analysis, we evaluate the suitability of achieving these requirements in silicon-based devices and

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estimate the degree of linearity that can be achieved as function of channel length over the quasi-ballistic regime.

Device Structure. Figure 1 shows the different physical and geometrical aspects of the silicon nanowire (SiNW) gate-all-around (GAA) n-MOS transistors,[17] which are used for linearity performance analysis in this experiment. These transistors satisfy the 1-D operation condition at low-temperatures over a certain gate voltage range due to the aggressively scaled channel diameters (~6 nm) as shown below. Because of this fact, devices can be quantitatively evaluated in terms of their quantum capacitance contribution to the total gate capacitance. Moreover, their channel length in the 250−400 nm range allows for quasi-ballistic transport at low temperatures. Due to a relatively large effective mass and channel lengths of these transistors compared to the requirements for 1-D and ballistic transport, respectively, most of the measurements were performed at 77 K to satisfy the above conditions. Channel materials with smaller effective masses and larger carrier mean-free-paths (mfp) such as InAs and InSb have the potential to satify the above transport conditions at room temperature.

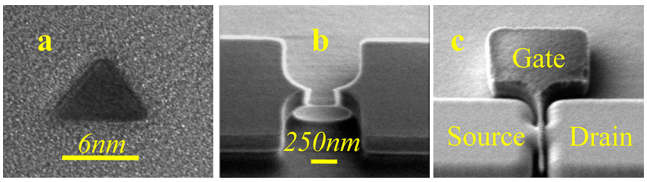

Figure 1. (a) Cross-sectional TEM image of the nanowire channel with triangular cross-section and diameter of ~6 nm, (b) tilted top view SEM image of the released 250 nm nanowire, and (c) GAA Si NWT after gate patterning. The gate dielectric is a 4 nm thermally grown silicon dioxide which wraps the entire channel. Channel and source/drain doping levels are 10^{15} cm^{-3} and 10^{20} cm^{-3}, respectively.

Operating Modes of Current Devices. The following subsections explain how operation of the GAA silicon nanowire transistors (NWT) in the 1-D, quasi-ballistic transport regime in the QCL is evaluated and analyzed within the context of the device linearity.

A. DC Bias Range. While device-level linearity can be achieved via biasing in the velocity saturation regime, operation in this regime results in relatively high power dissipation. In our experiments the velocity saturation regime has been explicitly avoided by keeping the channel electric field below 1 V/μm. This approach ensures that optical phonon scattering is not the cause of linearity in the investigated devices. Figure 2 shows output characteristics for a device with a channel length of 250 nm which limits V_{ds} to below 250 mV according to the above argument. Also, to achieve a large voltage gain and a steady output current, which is not sensitive to the amplitude of the input signal, transistors need to be biased at the maximum transconductance and minimum output conductance points. To accomplish this, devices can be biased in the overdrive voltage range of $V_{gs}-V_{th}$ = 0 V to 250 mV. The following subsection explains how this overdrive voltage range also satisfies the condition of 1-D transport in the channel, since a gate voltage range of 250 mV translates into a channel potential which is smaller than 85 meV, the requirement for 1-D transport in the transistors under investigation. Note that the chosen supply voltage range is around four times smaller than the requirements for today's RF circuits,[18] indicating that low power RF applications may become possible through this approach.

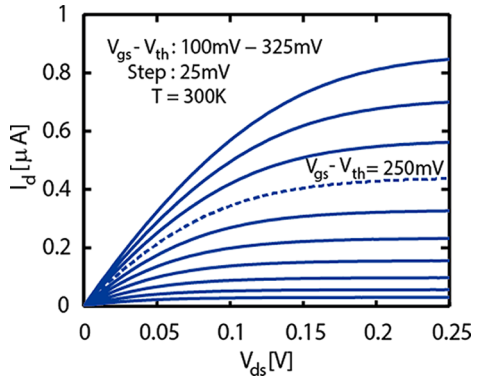

Figure 2. Output characteristic of a transistor with channel length of 250 nm. The dashed curve corresponds to the maximum gate overdrive that guarantees the operation of the device in current saturation to satisfy high transconductance and small output conductance requirements.

B. 1-D Transport. To establish that device operation with just one 1-D mode contributing to conductance is indeed possible with the devices under investigation, low-temperature properties have been explored first. Figure 3 shows a clear step in the transistor conductance as is typically observed in low-dimensional systems when 1-D transport prevails. This has been interpreted as evidence for one 1-D mode contributing to current transport over a certain gate voltage range before the threshold voltage for the second 1-D sub-band is reached (see G_d increase at around 1.8 V).[19,20] The above measurement also reveals that the threshold voltage for this device is around 0.7 V. When comparing the observations from Figure 3 with a simulated 1-D mode spectrum[21−23] for these nanowires one can conclude that a gate voltage range of about 700 mV—the plateau in Figure 3—corresponds to an effective band movement of ~85 meV. 85 meV is in this case the energetic spacing between the first and second 1-D sub-band found from simulations taking into account the actual device geometry.

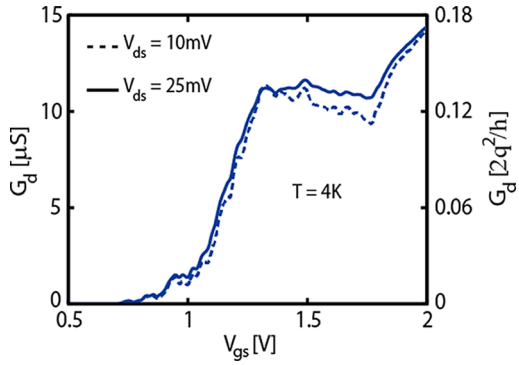

Figure 3. Conductance vs gate voltage for a device with a channel length of 250 nm. Clear 1-D transport effects are noticeable in the characteristics for 10 and 25 mV drain voltages.

C. Quantum Capacitance Limit. To confirm the above gate voltage-to-energy conversion statement, and to simulate the operation of the device in the QCL, the response of the conduction and valence band to the applied gate voltage has been calculated (see Figure 4). The inset of Figure 4 illustrates the simplified capacitance model governed by eq 2.

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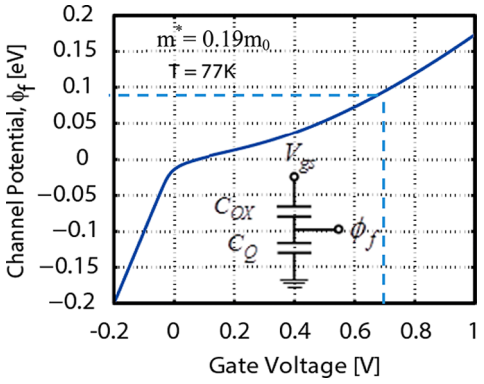

Figure 4. Simulated conduction and valence band movements for a single 1-D sub-band transistor.[25] Gate voltage and channel potential thresholds are adjusted to zero.

$$d\Phi_f = \frac{qC_{OX}}{C_{OX} + C_Q} dV_{GS} \tag{2}$$

C_{OX} denotes the gate oxide capacitance of the device and has been estimated by finite element analysis using COMSOL.[24] C_Q is the gate dependent quantum capacitance of the device which is calculated assuming a single parabolic 1-D sub-band density of states. Negative voltages in Figure 4 correspond to the device off-state showing the expected 1:1 band movement with the gate voltage. Due to the fact that $C_Q > C_{OX}$ in the device on-state, nanowire transistors do not operate in the ideal QCL. In fact, in the early on-state bands move slowly in response to the gate voltage because of the high DOS close to the onset of the first 1-D sub-band. Knowing the band movement of the transistors, one can translate the gate voltages in the experiment into the channel potential to back-calculate the operation of the device in the QCL and also to evaluate the above made linearity statement (see also Figure 6). In particular, one can confirm that the above claimed 1-D aspect, namely, the population of only one 1-D sub-band, holds true over a gate voltage range of ~700 mV (see the dashed line in Figure 4). While the input capacitance of the device will be a function of channel potential in the QCL, the specific impact of CQ on linearity will depend on the circuit topology. The current study is focused on transconductance linearity, which is expected to have an impact on circuit linearity regardless of circuit topology.

D. Quasi-Ballistic Transport and Scattering Approximation. Experiments have shown that ballistic effects become visible in the electrical characteristics when channel lengths are shrunk to about 46 nm for GAA Si NW MOSFETs.[26] With the channel length of 250 nm, scattering effects are expected to dominate the transport through the silicon channel at room temperature. To alleviate this effect, all of the analysis performed below has been carried out at 77 K, noting that in particular phonon scattering is substantially suppressed at this temperature. As mentioned at the beginning of this Letter, ballistic transport is one of the three critical requirements to achieve high linearity. Similar to the argument from above about operation in the QCL that allowed translating the nonideal device behavior in terms of gate voltage into the expected band movement, the linearity analysis is extended here to include the impact of scattering (see Linearity section). The following part of this section explains how backscattering in the channel is approximated to extract the mean-free-path (mfp) of the electrons from the experimental data. Next, the mfp values are used to calculate the 1-D current in the QCL using Landauer formalism. Through this approach we believe to properly account for the nonidealities of our silicon nanowires in terms of QCL and ballisticity allowing us to extract reliable information about the device linearity. To quantify the scattering in the channel, the measured transfer characteristics of the device is analyzed by employing the following approach: First, the current expected in the ballistic limit, $I_{ON\text{-}BALLISTIC}$, is calculated using Landauer's model:[15]

$$I_{ON} = -\frac{2q}{h}\int_{\varepsilon_1}^{\infty} T(E)\cdot M(E)\cdot(f_S - f_D)\cdot dE \tag{3}$$

$$M(E) \propto v(E)\cdot DOS_{1D}(E) \tag{4}$$

where q, h, and ε_1 are the charge of electron, Plank's constant, and bottom of the first transport energy sub-band respectively. $T(E)$ is the transmission coefficient, and $f_{S,D}$ are the Fermi distribution functions at the source and drain. $M(E)$ represents the number of modes which is directly proportional to the multiplication of carrier velocity $v(E)$ and the density of states $DOS_{1D}(E)$, see eq 4. In a 1-D ballistic channel $T(E)$ is equal to 1, and the carrier velocity and density of states have opposite energy dependencies resulting $v(E)\cdot DOS_{1D}(E)$ to be a constant. In the measured current, $I_{ON\text{-}MEASURED}$, the presence of scattering in the quasi-ballistic channel provides (i) a transmission coefficient which is smaller than one and (ii) a carrier velocity which has a different energy dependency compared to the ballistic carriers which causes the quasi-ballistic current to be nonlinear.

Next, the energy dependent mfp $\lambda(E)$ is determined by comparing the measured current, $I_{on\text{-}measured}$, to the calculated $I_{on\text{-}ballistic}$ at each channel potential (see Figure 5). Using eq 5

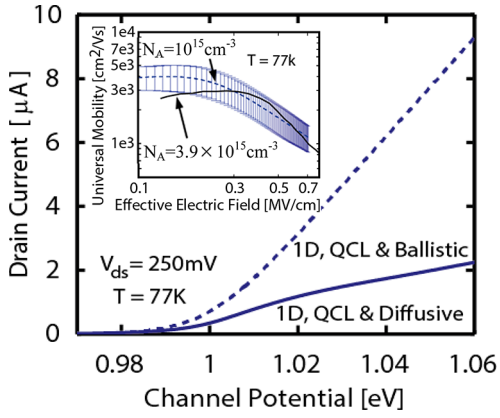

Figure 5. Solid, and dashed lines in the figure are the experimental and the ideal 1-D, transfer characteristics of the device under investigation in the QCL, respectively. Solid and dashed lines in the inset are the universal mobility vs gate field[27−29] and the extracted mobility from our data (with error bars), respectively.

the transmission coefficient in the current saturation regime, T_{sat}, can be calculated.[27]

$$\frac{T_{sat}}{2 - T_{sat}} = \frac{I_{on\text{-}measured}}{I_{on\text{-}ballistic}} \tag{5}$$

$$T_{sat} = \frac{\lambda_0}{\lambda_0 + L_{eff}} \tag{6}$$

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Equation 6 relates the transmission coefficient to λ_0 and the effective channel length of the device (L_{eff}). The effective channel length was assumed to be 6−8% of the actual channel length.[27] To evaluate the correctness of the above calculation, the averaged mfp values for different devices are converted into an effective gate field-dependent mobility.[28,29] Considering the various assumptions that enter into the conversion between the current data and the extracted mobility μ, the obtained μ vs effective electrical field data are in fair agreement with the expected universal mobility curve[30−32] (inset of Figure 5). Note that the deviation for small electric fields, where impurity scattering is the dominant scattering mechanism in the channel, is mainly a consequence of different channel doping.

Linearity. In this section the experimental findings on the nanowire device linearity after employing the conversion scheme between gate voltage and channel potential as described in the Operating Modes section, part C are discussed first. Then these findings are utilized to project the expected device linearity for aggressively scaled silicon nanowire devices including the impact of scattering.

A. Actual Device. By applying the findings from the Operating Modes section the device linearity of a nanowire transistor operating in the 1-D quasi-ballistic regime in the QCL can be evaluated. As apparent from Figure 6, the

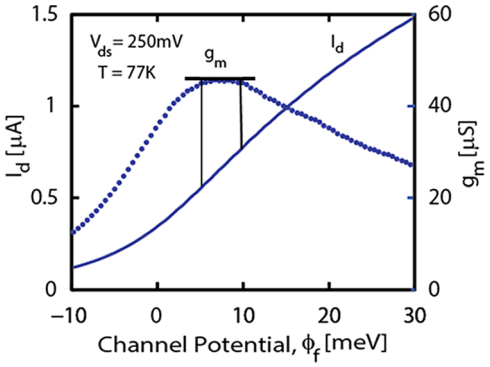

Figure 6. Transfer characteristics vs channel potential. The transconductance shows small variations over a certain channel potential range as a result of operation in the 1-D quasi-ballistic transport regime in the QCL. (The threshold voltage has been adjusted to zero.)

transconductance has small variations over a certain channel potential range, a signature of current linearity. The rather small channel potential range is a direct consequence of the nonballistic transport in the channel.

IIP3 is a standard figure of merit to measure RF linearity and is an indication of how well a system/device can "distinguish" between two adjacent frequencies.[33] Expressions for estimating the IIP3 from DC current−voltage characteristics have been derived[8] and applied in a number of previous studies, refs 7, 9 and 10. An overall expression considering nonlinearities in transconductance is given by eq 7:

$$\mathrm{IIP3} = \frac{2g_{m3}}{3R_S g_{m1}} = \frac{4(\partial I_d/\partial V_{gs})}{R_S(\partial^3 I_d/\partial {V_{gs}}^3)} \tag{7}$$

$$g_{mn} = \frac{1}{n!}\cdot\frac{\partial^n I_d}{\partial {V_{gs}}^n} \tag{8}$$

R_S is the system impedance, which is assumed to be 50 Ω for the following calculations. Equation 8 is the general definition for the weighted derivatives of transconductance. Note that the focus of this work is on the transconductance linearity due to the small variations of the output conductance (see Figure 2) and its negligible effect on linearity. Figure 7 shows the

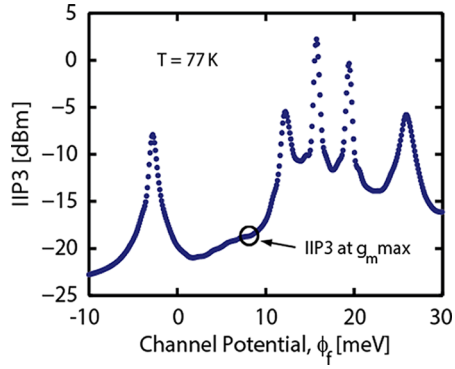

Figure 7. IIP3 for a transistor with 250 nm channel length biased to operate in the 1-D, quasi-ballistic transport regime in the QCL.

calculated IIP3 using eq 7 when the device is biased in the 1-D, quasi-ballistic transport regime in the QCL. The presence of noise in the measured transfer characteristics produces sharp peaks in IIP3 which are the results of high-order derivatives and can be ignored in this analysis due to the fact that they are far from the reference points (maximum transconductance). For a variety of RF applications, circuit designers tend to bias their device to achieve the highest voltage gain and linearity possible at the same time. Depending on the application, it is possible to trade-off between gain and linearity. As one can see from Figure 7 by moving away from the maximum transconductance point toward higher channel potentials one can achieve a higher degree of linearity.[34] At the same time it is apparent from Figure 6 that this higher linearity is achieved at the expense of a smaller transconductance and as a result smaller voltage gain. In a variety of RF receivers, the overall gain of the system is the product of the gains of the cascaded stages, and the trade-off between the gain and linearity in a single stage is affordable.

B. Projected Linearity versus Channel Length. As discussed above, scattering in the nanowire channel is a severe source of nonlinearity—at least when not operating in the velocity saturation regime. To project the performance of silicon nanowire devices with shorter channel lengths, the findings from Operating Modes section part D are employed. Furthermore, the maximum transconductance point is chosen as the point of reference to compare the RF linearity for transistors with different channel lengths. The average extracted λ_0 value at maximum transconductance from devices with different channel lengths was used to calculate the current for nonballistic 1-D transistors operating in the QCL for channel lengths that were not accessible experimentally. Figure 8 shows the extracted linearity for four different nanaowire channels (circles) that were analyzed as described in the Linearity section part A, as well as the projected linearity at maximum transconductance for a wide range of channel lengths assuming that the impact of scattering is independent of L. Linearity data from operation in the classical room temperature velocity saturation regime at the maximum transconductance point are also included for comparison (squares). Figure 8 shows that silicon nanowire transistors, even when operating in the 1-D and QCL, will not likely outperform the classically achievable degree of linearity since transport would have to become ~98%

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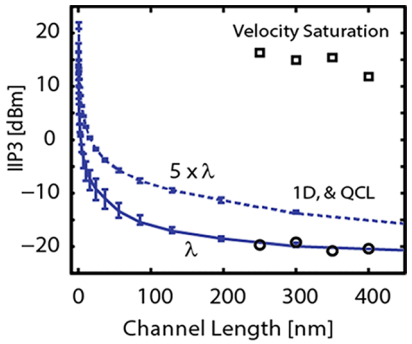

Figure 8. Linearity trend for devices operating in 1-D ballistic transport regime in the QCL is shown for a wide range of channel lengths (circles and solid line). The dashed line shows the effect of increasing the mfp for the same channel material.

ballistic to compete with the respective velocity saturation numbers. However, our analysis also provides valuable insights toward using different channel materials to improve RF linearity. For example, the dashed line in Figure 8 shows how linearity improves for transistors that are identical to the ones explored here but exhibit a larger mean-free-path.

Channel materials such as InAs and InSb, which exhibit longer mean-free-paths than silicon, are better candidates in the context of linearity since they allow for a higher degree of ballisticity at reasonable channel lengths. In addition, these materials also benefit from smaller effective masses, which in turn increase the sub-band splitting and facilitate 1-D transport accordingly. The suggested use of small effective mass materials requires careful evaluation of any scattering mechanism in the system that could impact the ballistic motion of the carriers. Another critical factor to improve linearity that is identified from this study is the rate of change of mfp as a function of channel potential. The smaller the rate of change, the more linear transfer characteristic are attainable. Thus materials that show a high degree of ballisticity while exhibiting a small rate of change of the mfp are expected to result in a linearity trend which can compete with the classical velocity saturation linearity for realistic channel lengths.

Conclusion. The presented work shows that linearity can be improved in 1-D systems that operate in the quantum capacitance limit by transitioning from the diffusive to the ballistic transport regime using silicon nanowires as an example system. The impact of mfp and rate of change of the mfp as a function of channel potential is also discussed qualitatively, and preliminary conclusions have been drawn about the use of other channel materials than silicon in the context of device linearity. Achieving linearity through 1-D, ballistic transport in the QCL is believed to require very low supply voltages if compared to traditional linearization methods. Consuming less power and providing a higher self-gain and linearity level at the same time low noise levels gives low-dimensional MOSFETs a unique advantage for applications such as LNAs at the front-end of transceivers in variety of RF wireless systems.

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Notes

The authors declare no competing financial interest.

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(34) Note that the increasing trend in the IIP3 plot is due to the fact that the rate of decrease of g_{m3} is larger than the rate of decrease of g_{m1} when evaluating IIP3 at a larger supply voltage. If ideal ballistic transport conditions would prevail in the channel g_{m1} would be constant ($2q^2/h$ = 77.46 μS) over a wide range of channel potentials, and g_{m3} would be zero.