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Analytical modeling of surface accumulation behavior of fully depleted SOI four gate transistors (G^4-FETs)

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ABSTRACT

A charge sheet model is proposed to analyze the transistor characteristics of fully depleted SOI four gate field effect transistors (G^4-FETs). The model is derived assuming a parabolic potential variation between the junction-gates and by solving 2-D Poisson's equation. The proposed model facilitates the calculation of surface potential and charge densities as a function of all gate biases. Modifying this charge sheet model for non-equilibrium condition, current–voltage and capacitance–voltage characteristics are also analyzed. Different back surface charge conditions are considered for each analysis. The models are compared with 3-D Silvaco/Atlas simulation results which show good agreement.

1. Introduction

FOUR-GATE-TRANSISTOR (G^4-FET) is an innovative silicon-on-insulator (SOI) device which offers four gate to enhance electrostatic control on the conducting channel [1]. SOI devices are popular for very low parasitic capacitance, better radiation tolerance and better isolation in both horizontal and vertical direction [2,3]. G^4-FET based circuits can be realized with a standard partially or fully depleted SOI process without requiring any additional fabrication processes [4]. The thin-film fully depleted SOI devices exhibit attenuated short channel effects, improved subthreshold slope, high transconductance, reduced hot carrier effects and so on.[5]. The fully-depleted (FD) G^4-FET is defined as an accumulation-mode SOI MOSFET featuring two junction-gates that provide an extra JFET-like control on the conducting channel [6]. G^4-FET features the maximum number of gates which will reduce the number of transistors in circuit design compared to standard CMOS implementations [7]. The efficiency in both analog and digital integrated circuit design depends highly on the accuracy of physics based models involved in the circuit simulation. The subthreshold regime has been studied for both partially and fully depleted G^4-FETs [8,9]. Analytical modeling above the threshold condition has been conducted for partially depleted G^4-FETs [10] but for FD device this region is studied using numerical approach only [6].

Modeling of potential distribution is prerequisite to model the transistor characteristics. An analytical model of 2-D potential distribution has been proposed for a FD G^4-FET previously [11]. This model was derived using full-depletion approximation, hence loses validity when the front or back surfaces are driven into strong accumulation or inversion. To model surface potential from weak inversion/accumulation to strong inversion/accumulation, charge sheet approximation has been used with good accuracy in the past [12,13]. The charge sheet approximation was first applied to thin film SOI devices by Ortiz-Conde et al. for equilibrium condition [14]. Later the model was modified for non-equilibrium condition [15]. Charge sheet model considering different back surface condition has been investigated for thin film SOI device in [16]. In this investigation, the model was derived by solving one dimensional Poisson's equation.

This work is intended to provide a simple and reasonably accurate charge-sheet model to analyze transistor characteristics of FD G^4-FETs. The model is derived by solving 2-D Poisson's equation with the assumption that the potential profile between the junction gates is parabolic in nature. The model is used here to analyze surface potential, accumulation charge and gate capacitance. An

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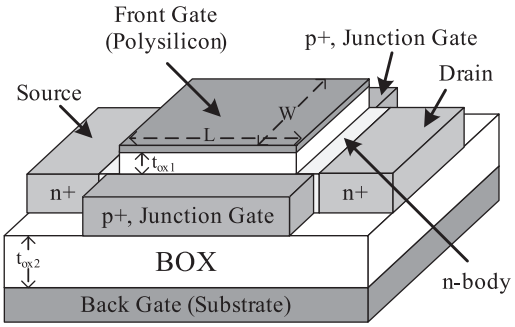

Fig. 1. Structure of an n-channel G⁴-FET.

extension to this model in the non-equilibrium situation is used to analyze drain current and transconductance of the device. Different back-surface charge condition has been taken into account for each analysis. The proposed charge-sheet model shows good agreement with the 3-D Silvaco/Atlas simulation results.

2. Device structure

The n-channel G⁴-FET is actually a p-channel SOI MOSFET with two body contacts located on each side of the channel [1]. In G⁴-FET, the body contacts of the p-channel MOSFET are used as the source and drain while the source and drain of p-channel MOSFET are used as junction-gates as shown in Fig. 1. Drain current comprises of majority carriers and flows in the direction perpendicular to that of a p-channel MOSFET [4]. In a FD G⁴-FET, the full body depletion is enabled just by doping-thickness combination.

3. Charge-sheet model

The device considered here is a long n-channel G⁴-FET. The front-gate voltage V_{G1}, back-gate voltage V_{G2} and junction-gate voltages $V_{JG1,2}$ are such that the body is fully depleted. For simplicity the junction-gates are tied together, i.e. $V_{JG1} = V_{JG2} = V_{JG}$. The potential distribution between the junction-gates shows a parabolic nature [11]. So the channel potential (defined with respect to a hypothetical neutral region) can be expressed as

$$\psi(x,y) = a(y)x^2 + b(y)x + c(y) \tag{1}$$

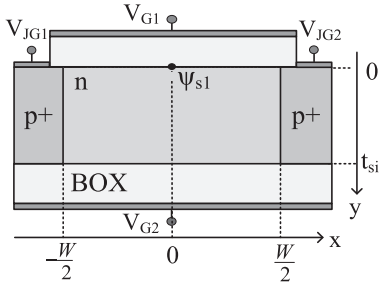

Fig. 2. Cross-section of an n-channel G⁴-FET showing axes and symbols for modeling.

The coefficients of (1) can be evaluated using the boundary conditions $\psi(-\frac{W}{2},y) = \psi(\frac{W}{2},y) = V_{JG} - \phi_b$. Here, W is the channel width and ϕ_b is the potential barrier between junction-gates and the channel. The axes and symbols used for modeling are indicated in Fig. 2. Thus (1) can be expressed in terms of $\psi(0,y) = \psi(y)$ as

$$\psi(x,y) = \left(1 - \frac{4x^2}{W^2}\right)\psi(y) + \frac{4}{W^2}(V_{JG} - \phi_b)x^2 \tag{2}$$

The 2-D Poisson's equation is given by

$$\frac{\partial^2\psi(x,y)}{\partial x^2} + \frac{\partial^2\psi(x,y)}{\partial y^2} = -\frac{\rho(x,y)}{\varepsilon_{si}} \tag{3}$$

where $\rho(x,y)$ is the total charge in the body and ε_{si} is the permittivity of silicon. Considering the charge neutrality condition and assuming complete ionization the total charge can be approximated as [17]

$$\rho(x,y) = qN_D\left[e^{\frac{2\phi_F}{V_t}}\left\{e^{-\frac{\psi(x,y)}{V_t}} - 1\right\} - \left\{e^{\frac{\psi(x,y)}{V_t}} - 1\right\}\right] \tag{4}$$

Here, $V_t = kT/q$ is the thermal voltage, k is the Boltzmann constant and T is the temperature, $\phi_F = -V_t\ln(N_D/n_i)$ is the Fermi potential of the n-type channel, N_D is the donor concentration, n_i is the intrinsic carrier concentration and q is the charge of electron. Putting the parabolic approximation (2) in the 2-D Poisson's equation yields

$$\frac{\partial^2\psi(y)}{\partial y^2} = \frac{8}{W^2}\psi(y) - \frac{8}{W^2}(V_{JG} - \phi_b) - \frac{\rho(x,y)}{\varepsilon_{si}} \tag{5}$$

This differential equation can be re-written as

$$\left(\frac{\partial\psi(y)}{\partial y}\right)d\left(\frac{\partial\psi(y)}{\partial y}\right) = \left[\frac{8}{W^2}\psi(y) - \frac{8}{W^2}(V_{JG} - \phi_b\frac{qN_D}{\varepsilon_{si}}\left\{e^{\frac{2\phi_F}{V_t}}\left\{e^{-\frac{\psi(x,y)}{V_t}} - 1\right\} - \left\{e^{\frac{\psi(x,y)}{V_t}} - 1\right\}\right\}d\psi(y)\right] \tag{6}$$

The front surface accumulation charge can be found as

$$Q_{s1} = \varepsilon_{si}\left.\frac{\partial\psi(y)}{\partial y}\right|_{y=0} \tag{7}$$

$$Q_{s1} = \sqrt{8C_{jg}^2\{\psi_{s1}^2 - 2(V_{JG} - V_P)\psi_{s1}\} + 2qn_i\varepsilon_{si}\left[\psi_{s1}e^{\frac{\phi_F}{V_t}} + 2V_t\left\{\cosh\left(\frac{\psi_{s1} - \phi_F}{V_t}\right) - \cosh\left(\frac{\phi_F}{V_t}\right)\right\}\right]} \tag{8}$$

In the hypothetical neutral region, $\psi = 0$ and $d\psi/dy = 0$ [17]. Integrating (6) from the hypothetical neutral region towards the front surface and solving for $\left.\frac{\partial\psi(y)}{\partial y}\right|_{y=0}$ yields a general expression of total charge (8). Using full depletion approximation, i.e. $\rho(x,y) \approx qN_D$, (5) can be solved to determine the depletion charge as

$$Q_{d1} = \sqrt{8C_{jg}^2\{\psi_{s1}^2 - 2(V_{JG} - V_P)\psi_{s1}\}} \tag{9}$$

The accumulation charge at the front surface can be approximated as $Q_{acc1} = Q_{s1} - Q_{d1}$. The drain current of G⁴-FET is due to the carriers accumulated at the front surface under control of V_{G1}. When V_{G1} is greater than the threshold voltage, the accumulation charge in the channel can be approximated as [18].

$$Q_{acc1} = C_{ox1}(V_{G1} - V_{TH}^* - \psi_{s1}) \tag{10}$$

where V_{TH}^* is the threshold voltage which is a strong function of back surface charge condition [6] and ψ_{s1} is the maximum surface potential at the mid position between the junction-gates for equal junction gate voltages [11].

$$V_{G1} - V_{TH}^{*} = \psi_{s1} + \sqrt{8\left(\frac{C_{jg}}{C_{ox1}}\right)^2\{\psi_{s1}^2 - 2(V_{JG} - V_P)\psi_{s1}\} + \kappa\left[\psi_{s1}e^{\frac{\phi_F}{V_t}} + 2V_t\left\{\cosh\left(\frac{\psi_{s1} - \phi_F}{V_t}\right) - \cosh\left(\frac{\phi_F}{V_t}\right)\right\}\right]} - \sqrt{8\left(\frac{C_{jg}}{C_{ox1}}\right)^2\{\psi_{s1}^2 - 2(V_{JG} - V_P)\psi_{s1}\}} \quad (11)$$

Thus from (8) and (10) a relationship among accumulation surface potential at the front surface and the applied gate biases can be derived as (11). Where, $C_{jg} = \varepsilon_{si}/W$ is the lateral depletion capacitance related to junction-gates, $\kappa = \frac{2qn_i\varepsilon_{si}}{C_{ox1}^2}$ and $V_P = \phi_b - \frac{qN_DW^2}{8\varepsilon_{si}}$ is the pinch-off voltage. The expression of threshold voltage considering different back surface charge conditions reported previously [11] can be used in (11) to calculate the front surface potential.

$$V_{G2}^{acc2} = V_{FB2} + (\gamma - \alpha)\frac{C_{jg}}{C_{ox2}}(V_{JG} - V_P) \quad (12)$$

$$V_{G2}^{inv2} = V_{FB2} + \left(1 + \alpha\frac{C_{jg}}{C_{ox2}}\right)2\phi_F - (\gamma - \alpha)\frac{C_{jg}}{C_{ox2}}V_P + \left(1 + \gamma\frac{C_{jg}}{C_{ox2}}\right)(V_{JG} - V_P) \quad (13)$$

When the back surface is inverted $\left(V_{G2} \leqslant V_{G2}^{inv2}\right)$, the threshold voltage is given by

$$V_{TH}^{*} = V_{FB1} - \gamma\frac{C_{jg}}{C_{ox1}}(2\phi_F + V_P) - \alpha\frac{C_{jg}}{C_{ox1}}(V_{JG} - V_P) \quad (14)$$

When the back surface is depleted $\left(V_{G2}^{acc2} \leqslant V_{G2} \leqslant V_{G2}^{inv2}\right)$, the threshold voltage is given by

$$V_{TH}^{*} = V_{FB1} - \beta(V_{G2} - V_{FB2}) + (\gamma - \alpha)\left(\frac{C_{jg}}{C_{ox1}} + \beta\frac{C_{jg}}{C_{ox2}}\right) \times (V_{JG} - V_P) \quad (15)$$

Here, $\beta = \left(\gamma\frac{C_{jg}}{C_{ox1}}\right) \Big/ \left(1 + \alpha\frac{C_{jg}}{C_{ox2}}\right)$, $\alpha = \frac{2\sqrt{2}}{\tanh\left(2\sqrt{2}\frac{t_{si}}{W}\right)}$, $\gamma = \frac{2\sqrt{2}}{\sinh\left(2\sqrt{2}\frac{t_{si}}{W}\right)}$, $C_{ox1,2} = \varepsilon_{ox}/t_{ox1,2}$ is the front gate and back gate oxide capacitances respectively, $t_{ox1,2}$ are the front and back oxide thickness, t_{si} is the silicon film thickness, ε_{ox} is the permittivity of oxide and $V_{FB1,2}$ are flat-band voltages. The hyperbolic and linear terms inside third bracket in (8) represents the charge accumulated at the mid position at the surface due to the front-gate bias. The remaining parabolic term represents the effect of lateral depletion region induced by junction-gates on the surface accumulation charge. The term $2qn_i\varepsilon_{si}\psi_{s1}e^{\frac{\phi_F}{V_t}}$ in (8) is negligible and can be ignored. The front surface potential and surface accumulation charge as a function of front-gate voltage for different back surface charge conditions provided by (11) and (8) respectively are shown in Figs. 3 and 4. The models are compared with the 3-D Silvaco/Atlas simulation results. The simulation was performed on an n-channel G^4-FET with $N_D = 10^{17}$ cm^{-3}, $t_{si} = 40$ nm, $W = 80$ nm, $t_{ox1} = 5$ nm and $t_{ox2} = 50$ nm.

At the onset of accumulation, the front surface potential $\psi_{s1} = 0$, which is the threshold condition for G^4-FET. The surface potential gradually increases with increasing front-gate voltage and eventually gets 'pinned' to a nearly constant value (0.29–0.35 V) when the front surface gets strongly accumulated. The potential is seen to increase by nV_t with increasing front-gate voltage when strong accumulation is achieved. Here, n is a real number which decreases with increasing front-gate voltage and eventually becomes a value less than unity for sufficiently large front-gate voltage. The model shows good agreement with the potential model of Akarvardar et al. [11] when the surface is in weak accumulation (see Fig. 3). The potential model in [11] keeps on rising linearly in strong accumulation.

It is observed that this 'pinning' of surface potential in strong accumulation almost disables the control abilities of other gates on front-channel potential. Previous studies on fully-depleted G^4-FET [6] showed that the lateral depletion regions induced by the junction-gates cannot significantly modulate the front-surface potential. Hence, junction-gate bias has a little effect on front-surface potential when the back surface is depleted. But when the back surface is inverted, the inversion layer at the back surface acts as a 'third' junction-gate and enables the junction-gates to modulate the back surface potential. In a thin film device, the front and back surface potential are interrelated by coupling [19]. Hence, the junction-gates are supposed to significantly modulate the front surface potential. But when the front surface becomes accumulated, the coupling between two surfaces becomes weaker and eventually vanishes when the front-surface is driven into strong accumulation. Thus only a slight gradual reduction in surface potential (around 5 mV for 1 V change in junction-gate bias) is observed

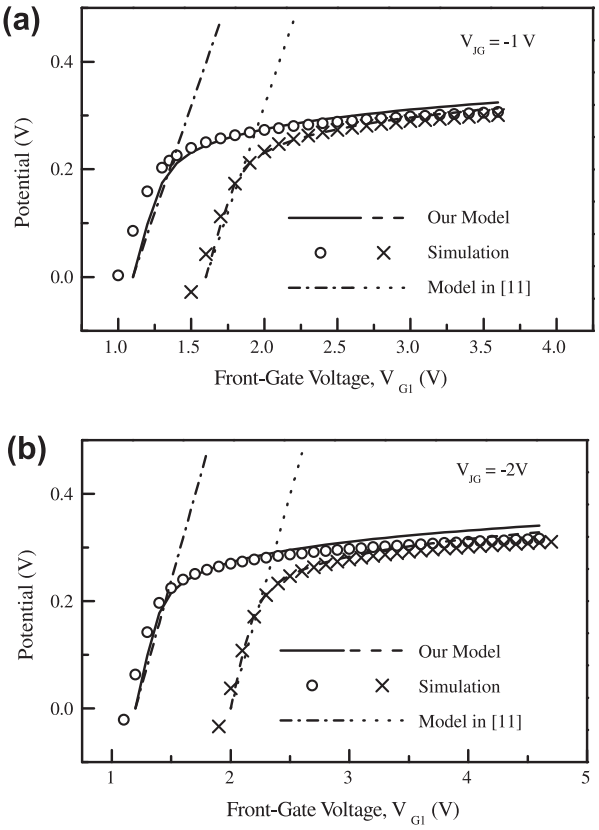

Fig. 3. Surface potential as a function of front-gate voltage for: (a) $V_{JG} = -1$ V and (b) $V_{JG} = -2$ V. The solid lines and circle symbols represent depleted back surface ($V_{G2} = 0$) and dashed lines and cross symbols represent inverted back surface ($V_{G2} = -15$ V).

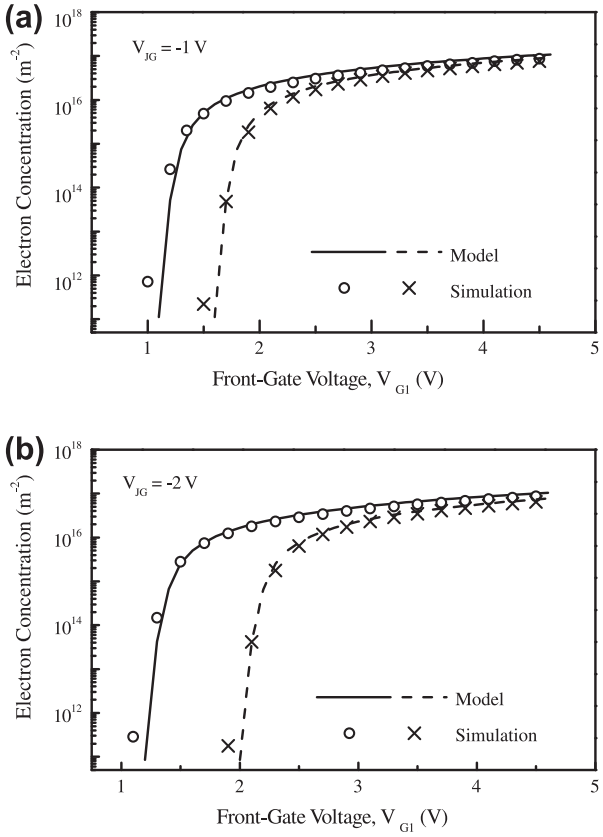

Fig. 4. Surface accumulation charge as a function of front-gate voltage for: (a) $V_{JG} = -1$ V and (b) $V_{JG} = -2$ V. The solid lines and circle symbols represent depleted back surface ($V_{G2} = 0$) and dashed lines and cross symbols represent inverted back surface ($V_{G2} = -15$ V).

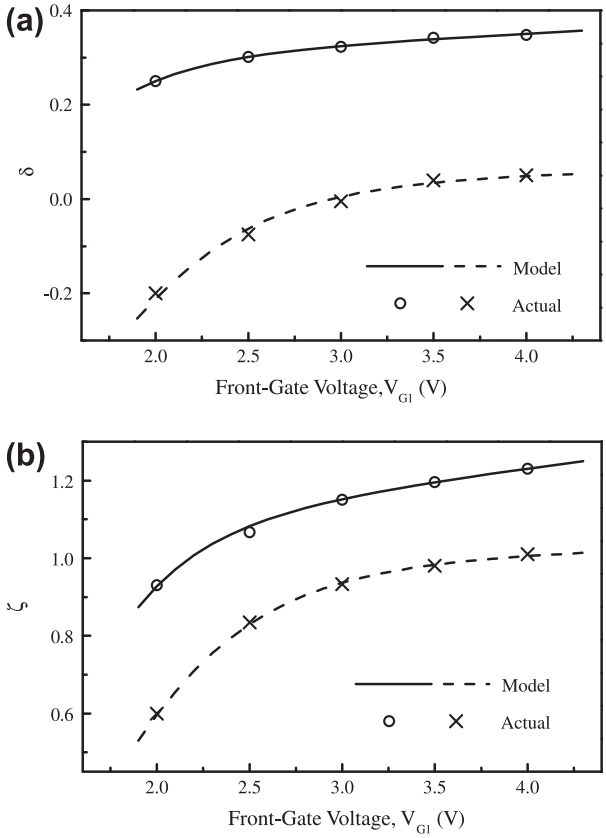

Fig. 5. (a) Fitting parameter δ and (b) fitting parameter ζ as functions of front-gate voltage.

for increase (in magnitude) in junction-gate bias, when the back surface is in inversion.

4. Drain current

The total drain is the summation of drift and diffusion components. Above the threshold condition, drift is the dominant mechanism of conduction. When a positive voltage V_C is placed at the n^+ region (source or drain end), less electron will be accumulated near that region than predicted by (8). Hence, the potential ψ_{s1} needs to be adjusted by $\psi_{s1} - V_C$ in the hyperbolic terms in (8) to consider the voltage at the n^+ region [20]. Thus the expression (11) can be modified as (16) for non-equilibrium condition. It is observed that a fraction of the junction potential (δ) is required to adjust the electron concentration at the surface. This fraction is a function of the vertical electric field induced by the front-gate. The drift current component can be found by integrating the following expression from source to drain.

$$I_{D,drift} = \mu_{eff} W Q_{s1} \frac{d\psi_{s1}}{dz} \tag{17}$$

Here, μ_{eff} is the effective mobility of electron and z is the direction along which the current flows. Using (10) in (17) the expression of current can be found as

$$I_{D,drift} = \mu_{eff} \zeta C_{ox1} \frac{W}{L} \left\{ (V_{G1} - V_{TH}^*)(\psi_{s1,D} - \psi_{s1,S}) - \frac{1}{2}\left(\psi_{s1,D}^2 - \psi_{s1,S}^2\right) \right\} \tag{18}$$

Here, is the potential at the source end, which can be found by placing $V_C = V_S$ in (16), where V_S is the source voltage (in this case, $V_S = 0$). $\psi_{s1,D}$ is the potential at the drain end, which can be found by placing $V_C = V_D$ in (16), where V_D is the applied drain voltage. ζ is used as a fitting parameter here, which is also a function of the vertical electric field. ζ and δ can be approximated by two empirical expressions as

$$V_{G1} - V_{TH}^* = \psi_{s1} + \sqrt{8\left(\frac{C_{jg}}{C_{ox1}}\right)^2 \{\psi_{s1}^2 - 2(V_{JG} - V_P)\psi_{s1}\} + 2\kappa V_t \left[\cosh\left\{\frac{\psi_{s1} - \phi_F - V_C - \delta(V_{JG} - \phi_b)}{V_t}\right\} - \cosh\left(\frac{\phi_F}{V_t}\right)\right]} - \sqrt{8\left(\frac{C_{jg}}{C_{ox1}}\right)^2 \{\psi_{s1}^2 - 2(V_{JG} - V_P)\psi_{s1}\}} \tag{16}$$

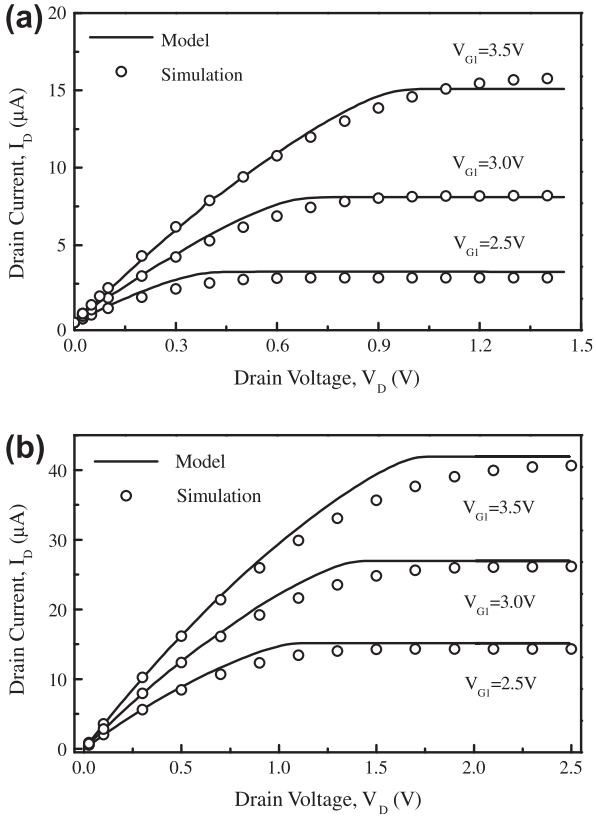

Fig. 6. Drain current as a function of drain voltage for different front-gate biases, $V_{JG} = -1$ V and $V_D = 0.3$ V, when the back surface is: (a) inverted ($V_{G2} = -15$ V) and (b) depleted ($V_{G2} = 0$ V).

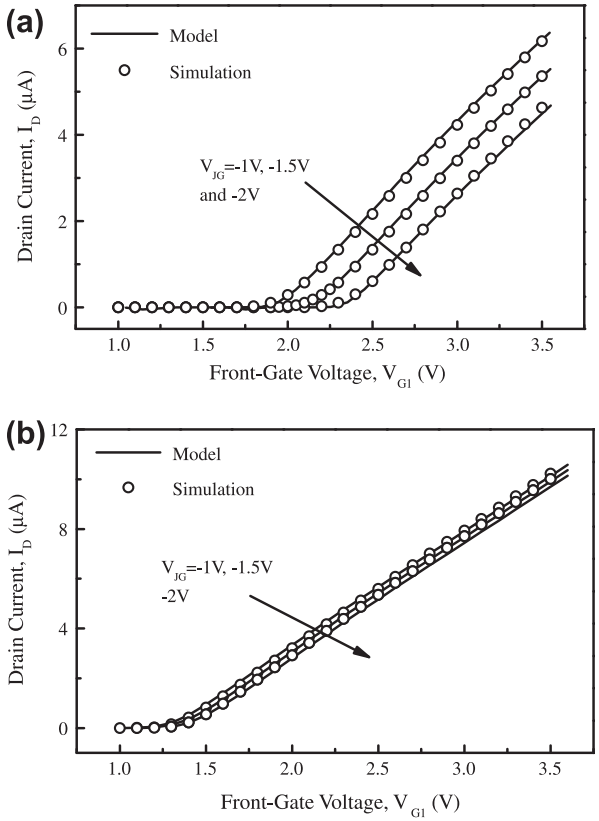

Fig. 7. Drain current as a function of front-gate voltage for different junction-gate biases and $V_D = 0.3$ V, when the back surface is: (a) inverted ($V_{G2} = -15$ V) and (b) depleted ($V_{G2} = 0$ V).

$$\zeta = \frac{1}{1 + \left(\frac{V_0}{V_{G1}}\right)^{\tau}}(1 + \lambda_\mu V_{G1}) \tag{19}$$

$$\delta = \Gamma_\mu \zeta + \Omega_\mu \tag{20}$$

Here, V_0, τ, λ_μ, Γ_μ and Ω_μ are the empirically determined model parameters. In this work $V_0 = 1.5$ V, $\tau = 5.5$,$\lambda_\mu = 0.059$, $\Gamma_\mu = 0.332$ and $\Omega_\mu = -0.058$ for depleted back surface and $V_0 = 1.865$ V, $\tau = 5.1$,$\lambda_\mu = 0.0065$, $\Gamma_\mu = 0.635$ and $\Omega_\mu = -0.59$ for inverted back surface. ζ and δ as a function of front-gate voltage are shown in Fig. 5. The 'actual' values indicated in the figure are calculated using successive trial and error method to fit the simulation results. The 'model' values are given by (19) and (20) .

The effective mobility (μ_{eff}) of electron is taken as the concentration dependent low field mobility, which is around 650 cm^2/V-s [21]. δ and ζ provided by (19) and (20) are shown in Fig. 5. The circles in the figures represent the actual values which were calculated by successive trial method through curve fitting approach for better fit.

In the subthreshold region, the diffusion is the dominant mechanism of conduction. In this region, drain current is related to the front-gate bias via maximum surface potential (ψ_{s1}) [9]. The diffusion current is given by

$$I_{D,diff} = \mu_{eff} W V_t \frac{dQ_n}{dz} \tag{21}$$

Here, Q_n is the surface electron charge. Integrating this equation from source to drain yields

$$I_{D,diff} = \mu_{eff} \frac{W}{L} V_t (Q_{n,D} - Q_{n,S}) \tag{22}$$

$Q_{n,S}$ and $Q_{n,D}$ are surface electron charge at source and drain ends which can be approximated as reported in [21].

$$Q_{n,S} = -\frac{\varepsilon_{si} n_i kT}{C_{ox1}(V_{G1} - \psi_{s1})} e^{\frac{\psi_{s1} - \phi_F}{V_t}} \tag{23}$$

and

$$Q_{n,D} = -\frac{\varepsilon_{si} n_i kT}{C_{ox1}(V_{G1} - \psi_{s1})} e^{\frac{\psi_{s1} - \phi_F - V_D}{V_t}} \tag{24}$$

This front surface potential in the subthreshold region can be found by solving the potential models proposed in [11].

$$V_{G1,2} = V_{FB1,2} + \left(1 + \alpha \frac{C_{jg}}{C_{ox1,2}}\right)\psi_{s1,2} - \gamma \frac{C_{jg}}{C_{ox1,2}}\psi_{s2,1} + (\gamma - \alpha)\frac{C_{jg}}{C_{ox1,2}}(V_{JG} - V_P) \tag{25}$$

For depleted back surface the back surface potential can be found from (25). For inverted back surface, the back surface potential is $\psi_{s2} = V_{JG} + 2\phi_F$. Diffusion current above the threshold can be found by using the models 8, 11 and 22. The total drain current can be found from the following expression

$$I_D = I_{D,drift} + I_{D,diff} \tag{26}$$

The threshold voltage slightly changes with the change in junction-gate bias for depleted back surface. But the threshold voltage is a very sensitive function of junction-gate bias when the back surface is in inversion. An increase in junction-gate bias magnitude causes increase in threshold voltage [11], which leads to a lateral shift in the $I_D - V_{G1}$ curves as shown in Fig. 7. Similar study was

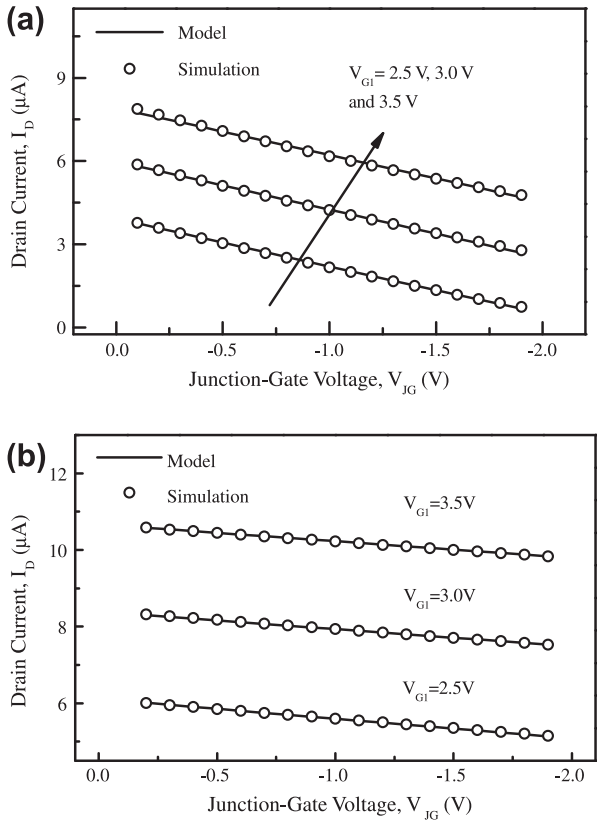

Fig. 8. Drain current as a function of junction-gate voltage for different front-gate biases and V_D = 0.3 V, when the back surface is: (a) inverted (V_{G2} = −15 V) and (b) depleted (V_{G2} = 0 V).

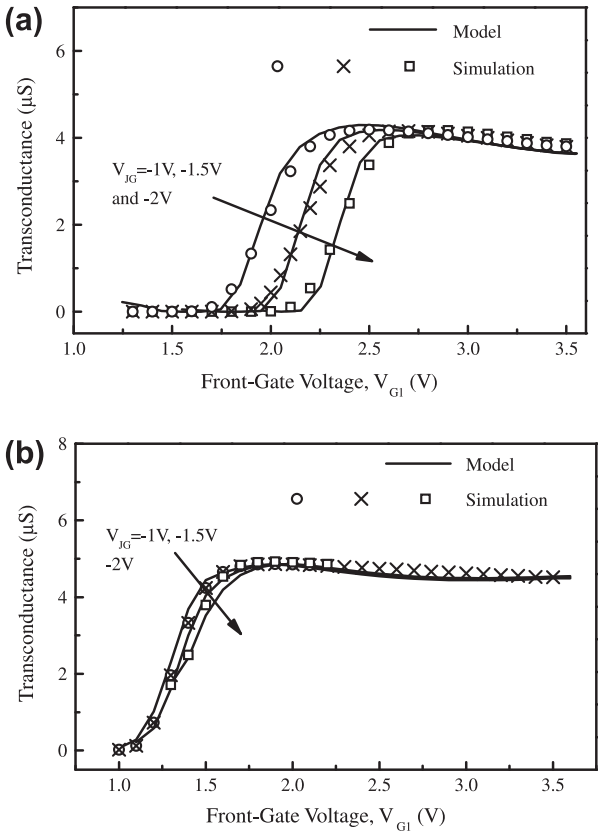

Fig. 9. Front-gate transconductance of the as a function of front-gate voltage for different junction-gate biases and V_D = 0.3 V, when the back surface is: (a) inverted (V_{G2} = −15 V) and (b) depleted (V_{G2} = 0 V).

also reported in [6]. The lateral depletion depth induced by the junction-gates reduces the effective width of the channel which in turn reduces the accumulation charge participating in the channel current. That is why the drain current reduces with increasing junction-gate voltage (see Fig. 8), although the rate of this reduction is lower for depleted back surface.

The drain current saturates for a large drain voltage (see Fig. 6) since the hyperbolic terms in (16) become negligible. Hence, the drain end potential saturates to a constant value given by

$$\psi_{s1,D}^{sat.} = V_{G1} - V_{TH}^{*} \tag{27}$$

The saturation current increases when the back surface is driven to depletion from inversion for the same front-gate voltage. The threshold voltage is seen to be lower for depleted back surface than inverted back surface [11]. Thus the overdrive voltage $V_{G1} - V_{TH}^{*}$ becomes larger causing larger amount of charge to be accumulated at the front surface and hence larger drain current is observed. The saturation point depends on the overdrive voltage related to front-gate $(V_{G1} - V_{TH}^{*})$. The threshold voltage V_{TH}^{*} itself depends on the overdrive voltage related to junction-gate $(V_{JG} - V_P)$. This observation certainly proves the claim that this novel device is a perfect combination of a MOSFET and a JFET [1,6].

The front-gate transconductance ($g_{m1} = \partial I_D / \partial V_{G1}$) can be calculated using the drain current model proposed here. Transconductance as a function of front-gate bias is shown in Fig. 9. When the back surface is driven to inversion, the transconductance value decreases, but the dependence on junction-gate bias increases. This effect can be explained by the degradation of the mobility in front accumulation channel due to increased vertical electric field [6,22].

5. Capacitance model

The per unit area capacitance in the accumulation region related to the front-gate can be written as

$$C_{G1}^{acc} = \frac{dQ_{acc1}}{dV_{G1}} = \frac{dQ_{acc1}}{d\psi_{s1}} \frac{d\psi_{s1}}{dV_{G1}} \tag{28}$$

The derivatives in (28) can be evaluated using the expressions of charge and potential (8) and (11) respectively. The evaluation yields an expression showing a series combination of front oxide capacitance (C_{ox1}) and front channel capacitance in accumulation $(C_{ch1}^{acc.} = \partial Q_{acc1} / \partial \psi_{s1})$.

$$C_{G1}^{acc} = \frac{C_{ox1} C_{ch1}^{acc}}{C_{ox1} + C_{ch1}^{acc}} \tag{29}$$

Using (8), the front-accumulation capacitance is evaluated as (30) shown at the bottom of the page. The gate capacitance provided by (29) and (30) is shown in Fig. 10. For sufficiently large front-gate voltage, the front-gate capacitance becomes nearly equal to the front oxide capacitance. A lateral shift in the front-gate capacitance is observed for increasing (in magnitude) junction-gate bias. But the accumulation capacitance shows almost similar change with front-gate bias for both depleted and inverted back surface.

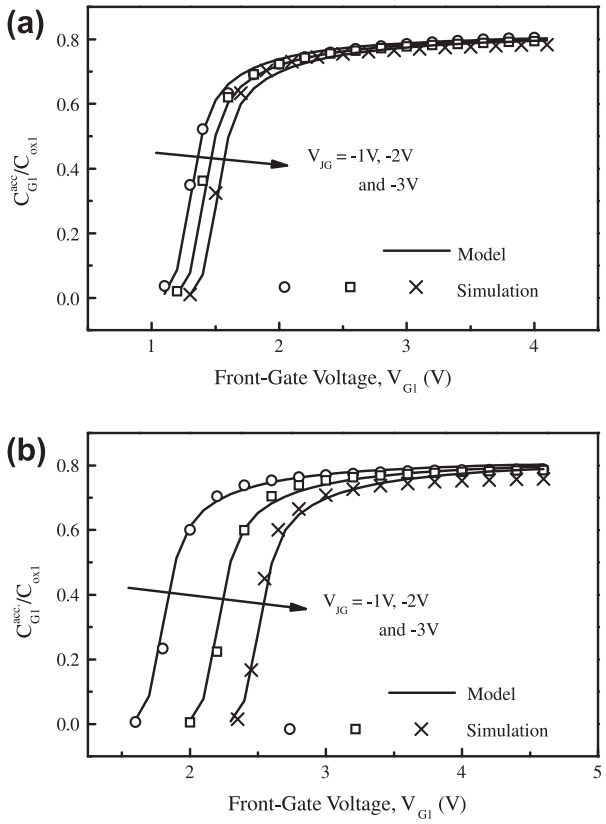

Fig. 10. Normalized gate capacitance as a function of front-gate voltage for different junction-gate biases when the back surface is: (a) inverted (V_{G2} = −15 V) and (b) depleted (V_{G2} = 0 V).

also depends on the junction potential ($V_{JG} - \phi_b$). This dependence is much more complex due to vertical electric fields induced by front and back gates. In order to incorporate the effect of this fraction of junction potential, two fit parameters δ and ζ are introduced. Here, δ denotes the fraction of junction potential which is missing in the model. δ itself is a strong function of vertical fields. The introduction of empirical models as fit parameters was inspired from the previously proposed saturation current model for partially depleted G4-FETs [23]. For similar reason Akarvardar et al. introduced a fit parameter 'α' in their model for partially depleted G^4-FET [10]. Detailed analysis for the fit parameters proposed here and the physics behind will be presented in a future paper.

The effect of channel length modulation was not included in the drain current model. Thus a deviation in the saturation region is observed. Finally, the effect of oxide fixed charge, interface traps and recombination was not included in the model. The models proposed here are non-linear equations, which are to be solved by an iteration technique. The proper choice of a technique and parameters are required to yield less computational time and good accuracy.

Analysis for accumulated back surface is not considered in this work because when the back surface is accumulated, the back channel current acts as a leakage current to the front channel current and in turn shunts the device. This mode of operation is not useful for circuits.

In an earlier work, it has been demonstrated that the subthreshold swing of the device degrades when the back surface is driven from depletion to inversion [9]. The subthreshold swing is seen to stay close to ideal value only for depleted back surface. Moreover, the swing remains close to the ideal value for wide channel devices and ultra-thin film devices. Thin front oxide thickness and thick back oxide thickness is also required to ensure subthreshold swing closer to the ideal value.

$$C_{ch1} = \frac{8C_{jg}^2(\psi_{s1} - V_{JG} + V_P) + qn_i\varepsilon_{si}\left\{e^{\frac{\phi_F}{V_t}} + 2\sinh\left(\frac{\psi_{s1}-\phi_F}{V_t}\right)\right\}}{\sqrt{8C_{jg}^2\{\psi_{s1}^2 - 2(V_{JG}-V_P)\psi_{s1}\} + 2qn_i\varepsilon_{si}\left[\psi_{s1}e^{\frac{\phi_F}{V_t}} + 2V_t\left\{\cosh\left(\frac{\psi_{s1}-\phi_F}{V_t}\right) - \cosh\left(\frac{\phi_F}{V_t}\right)\right\}\right]}} - \frac{8C_{jg}^2(\psi_{s1} - V_{JG} + V_P)}{\sqrt{8C_{jg}^2\{\psi_{s1}^2 - 2(V_{JG}-V_P)\psi_{s1}\}}} \quad (30)$$

6. Discussion

The models proposed here shows a slight deviation from the simulated results. The parabolic change of potential assumed between the junction-gates is not completely accurate. The actual potential variation is much wider than the parabolic approximation, as can be seen in [11]. Moreover, the threshold voltage model used here also shows slight deviation from the numerical results. The deviation in threshold voltage is larger for inverted back surface since the back surface potential was set to the classical value $V_{JG} + 2\phi_F$ and was assumed to be constant while modeling the threshold voltage. But in strong inversion, back surface potential increases beyond this classical value by few thermal voltages [19]. Thus slight deviation is observed in the equilibrium condition.

The situations become much more complicated in non-equilibrium condition. The quasi Fermi levels at the drain end are separated by the drain voltage (qV_D). The reverse bias between the junction gates and the body increases from the source end to drain end. Since the body is fully depleted, quasi Fermi level separation

7. Conclusion

A complete set of simple, yet accurate mathematical models for analyzing surface accumulation behavior is proposed. Comparison with the simulation results show very good accuracy relative to the low computational time required. These models will prove to be very important tools to realize circuit opportunities using FD G^4-FETs. Moreover, these models can be applied to some other FET devices, having structural similarities with G^4-FET.

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