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Design of high-current L-valley GaAs/AlAs_{0.56}Sb_{0.44}/InP (111) ultra-thin-body nMOSFETs

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Abstract— We propose and analyze a high-current III-V transistor design using electron transport in the Γ - and L-valleys of (111) GaAs. Using $sp^3d^5s^*$ empirical tight-binding model for band-structure calculations and the top-of-the-barrier transport model, improved drive current is demonstrated using L-valley transport in a strained GaAs channel grown on an (111) InP substrate. At a body thickness of 2 nm the (111)GaAs/InP MOSFET design outperforms both (100) Si and (100) GaAs/InP for all EOTs larger than 0.3nm.

Index Terms— MOSFET, L-valley, tight-binding, GaAs, InP, top-of-the-barrier

I. INTRODUCTION

III-V nMOSFETs have small transport effective mass that provides high electron velocities and high on-state currents. However, small effective mass also leads to a small semiconductor density of states, and consequently III-V channels provide no benefit over Si for EOT < 0.6 nm [1]. This loss of state density can be compensated by using the highly anisotropic L-valley for electron transport [2]. Confining the channel along the (111) direction leads the L-valley to have a large confinement mass and much smaller in-plane transport mass. At some channel thickness, the Γ - and L-valleys are aligned in energy, increasing the state density and on-current [3]. Simulations in [3] ignored interactions of the channel wavefunction with gate dielectric and the well bottom barrier: here we report practical L-valley GaAs channel designs incorporating AlAs_{0.56}Sb_{0.44} barriers to set the boundary conditions for Γ -L alignment.

II. DEVICE STRUCTURE

Interaction of the channel wavefunction with the amorphous gate dielectric is difficult to compute, hence ideal hydrogen-terminated semiconductor interfaces are often assumed in simulations. To prevent this interaction from changing the Γ -L energy alignment and dispersion, the designs here reported use thin AlAs_{0.56}Sb_{0.44} cladding layers to strongly attenuate the channel wavefunction at the dielectric-semiconductor interface. Fig. 1 shows the device geometries under study in this paper. A single-gate (SG) MOSFET consists of a biaxially strained (3.67% mismatch with InP) GaAs channel grown on a 5nm AlAs_{0.56}Sb_{0.44} barrier layer, lattice matched to InP. Two monolayers of AlAs_{0.56}Sb_{0.44} serve as a cap-layer. Similarly, for a double-gate (DG) MOSFET a biaxial strained GaAs with AlAs_{0.56}Sb_{0.44} cap layer on top and bottom are assumed.

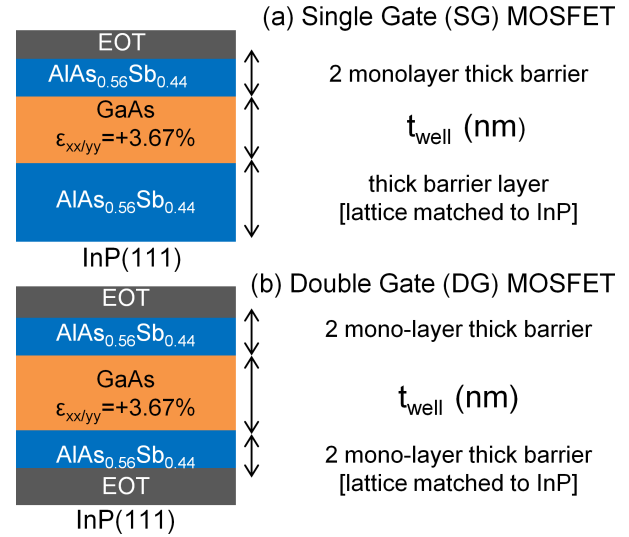


Fig. 1. GaAs/AlAs_{0.56}Sb_{0.44}/InP (111) MOSFETs based on (a) a single gate with strained GaAs channel and AlAs_{0.56}Sb_{0.44} as a capping and barrier layer (b) a double gate structure with strained GaAs channel AlAs_{0.56}Sb_{0.44} capping layer.

Similar designs are used for GaAs/InP (100) and Si (100) (no cap layer) for comparison of device performance.

III. SIMULATION METHODOLOGY

Band structure calculations of the SG/DG structures (Fig. 1) are performed using an $sp^3d^5s^*$ empirical tight-binding model including spin-orbit coupling. GaAs has a smaller lattice constant than InP, leading to an in-plane tensile strain $\simeq 3.67\%$ in GaAs. The biaxial strain is modeled as a homogenous strain tensor that affects the original atomic positions [4]. Strain effects are taken into account according to the Boykin model [5]. Both the channel material, GaAs and the capping layer AlAs_{0.56}Sb_{0.44} are included in the simulation domain. Fig. 2 explicitly shows the effect of including a barrier layer on the band structure calculations. For a 2 nm thick, GaAs thin body structure grown on InP(111) with idealized hydrogen-terminated interfaces, the conduction band minima is formed by the L-valley states. The inclusion of thick AlAs_{0.56}Sb_{0.44} layers on top and bottom reduces effective confinement and the Γ valley becomes the lowest-energy band. It should be noted that, electronic effects due to strain are included only

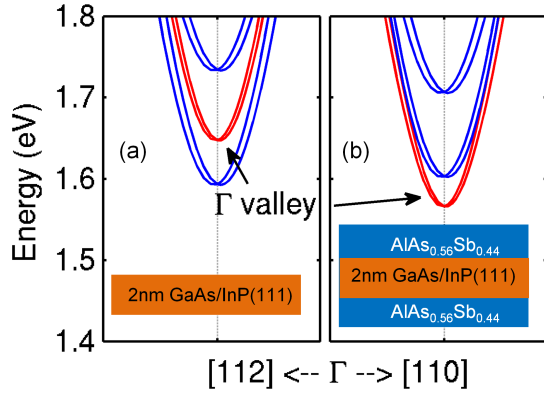


Fig. 2. Bandstructure calculations for 2 nm thick and biaxially strained (a) GaAs/InP(111) and (b) GaAs/InP(111) with 5 nm thick $\text{AlAs}_{0.56}\text{Sb}_{0.44}$ layers.

for the GaAs material [5]. The $\text{AlAs}_{0.56}\text{Sb}_{0.44}$ layer, that is lattice matched to InP is not affected by strain.

To compare the device performance, 2D E-k relations are calculated for different device structures. The energy dependent density of states (DOS) and carrier velocity are then extracted from the band structure information. For GaAs/InP(111) case, $\langle 110 \rangle$ orientation is considered to be the transport orientation while for GaAs/InP(100) and Si(100) cases $\langle 100 \rangle$ is taken as the transport orientation. The DOS(E) and velocity(E) information are then used to calculate the on-state current (I_{on}) using the ballistic top-of-barrier transport model implemented in NEMO5 simulation package [6], [7].

IV. RESULTS

Fig. 3(a) shows the bandstructure calculations for GaAs UTB terminated by 2 - monolayer $\text{AlAs}_{0.56}\text{Sb}_{0.44}$ and lattice matched to InP. From the GaAs body thickness dependent band structure calculations it is revealed that L-valley minima transistor can be reached by confining GaAs to a 2 nm body thickness (marked in Fig. 3(a)). This particular structure

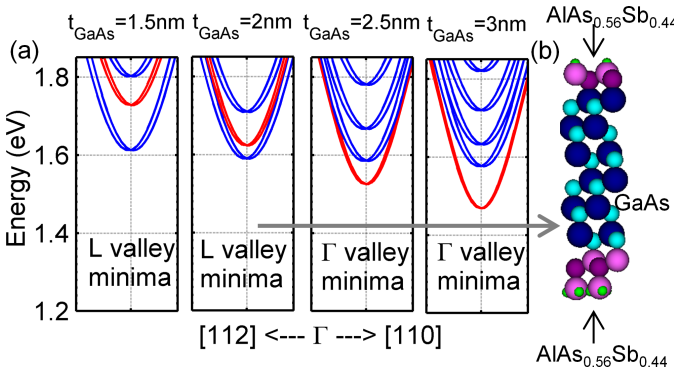


Fig. 3. Tight-binding bandstructure ($sp^3 d^5 s^*$) calculations for (111) oriented GaAs terminated with 1-2 monolayer $\text{Al}_{0.56}\text{As}_{0.44}\text{Sb}$ lattice matched to InP. The blue lines correspond the L valley states, while the red lines correspond to the Γ valley states.

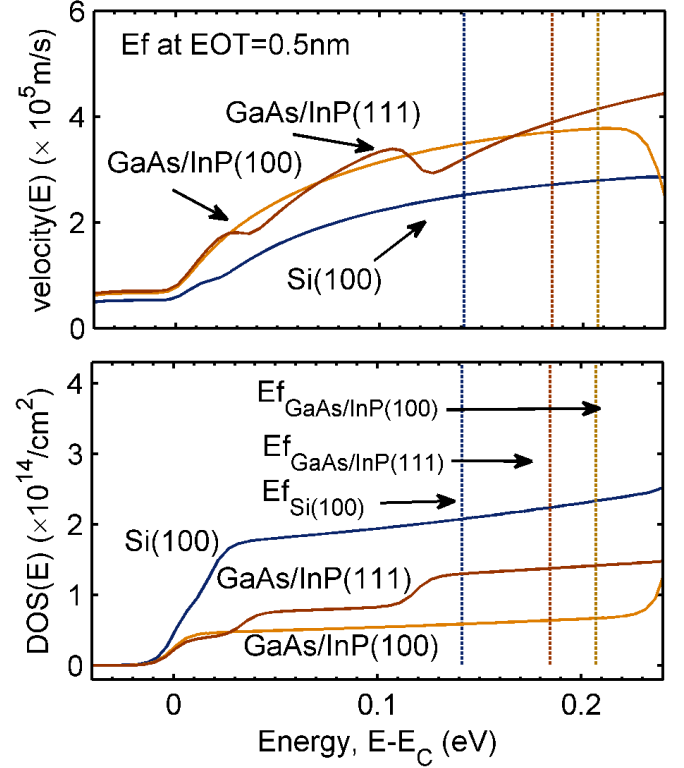


Fig. 4. Density of states and carrier velocity for 2 nm thick GaAs/InP(111), GaAs/InP(100) and Si(100) structures. Fermi level E_f position in the on state for DG MOSFET and EOT=0.5 nm is also shown. Energy axis has been adjusted to the conduction band edge, E_C

is used for GaAs/InP(111) device performance comparison throughout this paper.

Fig. 4 compares state density and carrier velocity for the different channel designs. It is readily observed that Si(100) exhibits higher DOS and lower velocity when compared to GaAs/InP(100) which exhibits a high velocity but suffers from lower DOS. The small state density leads to the condition popularly known as 'DOS bottleneck' associated with low carrier effective mass III-V materials [1]. The GaAs/InP(111) transistor design aims to offset both the issues as will be shown later.

As a next step, ON state currents are calculated for 2 nm body structures with the channel material as GaAs/InP(111), which is the L-valley minima case, GaAs/InP (100) and Si (100). The on-state current is defined as the current at $V_{ds}=V_{gs}=0.5\text{V}$, with threshold voltage V_{th} set so that $I_{off} = 0.1\mu\text{A}/\mu\text{m}$. The on-state currents are calculated for different EOT values ranging from 0.3nm to 1.1nm. The degrading effect of the $\text{AlAs}_{0.56}\text{Sb}_{0.44}$ cap layer on the capacitive coupling of the GaAs channel to the gate is considered by increasing the EOT per gate by 0.1nm.

Fig 5 shows the gate capacitance (C_G) normalized to oxide capacitance (C_{OX}) for the DG MOSFET structures. It can

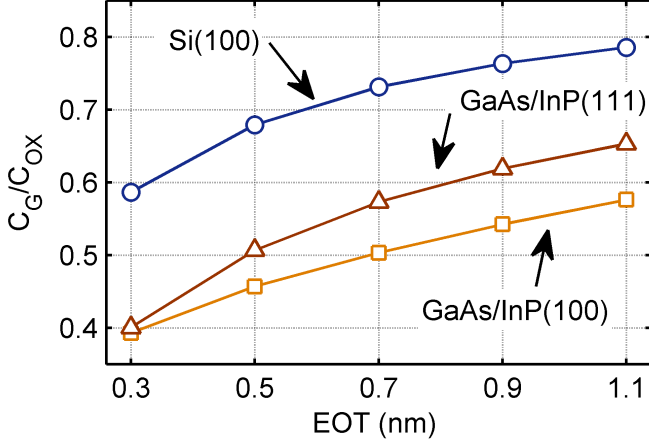


Fig. 5. Gate capacitance normalized with oxide capacitance is shown for DG MOSFET. Gate capacitance calculated $V_{gs}=0.5V$ and $V_{ds}=0.05V$

be deduced from Eq (2) a high C_{DOS} (directly related to $DOS(E)$, Eq (1)) leads to C_G being closer to C_{OX} , or lower a DOS will lead to degraded C_G and ultimately on-state current (Eq 3). In Eq (2) D_{mean} is the mean wavefunction depth in the semiconductor and ϵ_s is the semiconductor permittivity. As expected GaAs/InP(100) which has a small confinement mass or lowest DOS has the smallest C_G . This is the 'DOS bottleneck' effect, which practically nullifies the expected gains from increasing the gate dielectric capacitance. This drawback can be minimized by utilizing L-valley minima transistor designs that allows multiple subbands close to band edge. The L-valley minima design of GaAs/InP(111) exhibits an increased C_G when compared to GaAs/InP(100). However, Si(100) still exhibits the highest gate capacitance owing to its large state density (Fig (4)). It should be noted that the GaAs/InP cases have further degraded capacitance due to the presence of $AlAs_{0.56}Sb_{0.44}$ cap layer.

$$C_{DOS} = q^2 \frac{dn_s}{dE_f} \quad (1)$$

$$C_G = (C_{DOS}^{-1} + C_{OX}^{-1} + D_{mean}/\epsilon_s)^{-1} \quad (2)$$

and,

$$I_{ON} = qC_G(V_{gs} - V_{th}) \cdot v_{avg} \quad (3)$$

The final computed I_{on} values are shown in Fig. 6. GaAs/InP(111) exhibits an improved gate capacitance over GaAs/InP(100) and at the same time shows a higher carrier velocity over Si(100) MOSFET. This fact leads GaAs/InP(111) MOSFET to perform better than both GaAs/InP(100) and

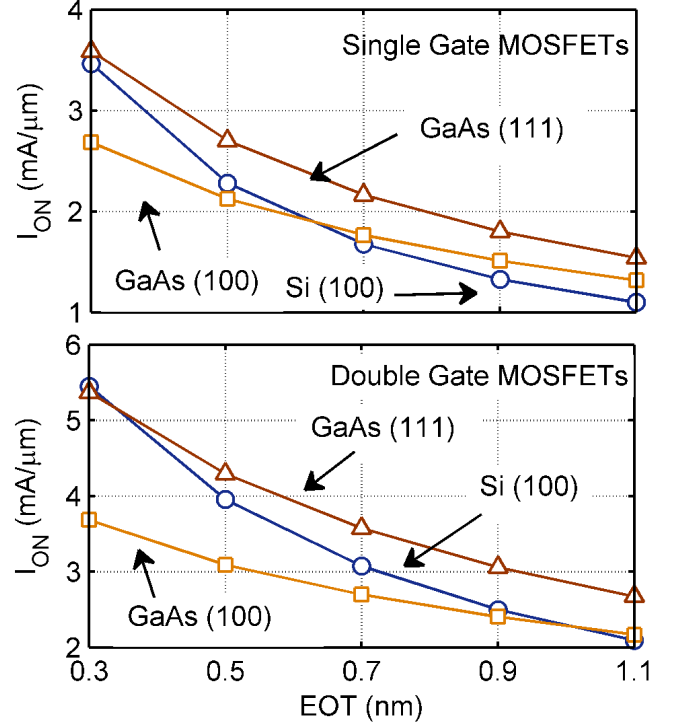


Fig. 6. ON state currents calculated for different EOT values for (a) single gate and (b) double gate structures.

Si(100) MOSFET structures at higher EOT values. For SG and DG MOSFET designs, Si(100) surpasses GaAs/InP(100) in $I_{on} \simeq 1.0$ nm and $\simeq 0.6$ nm EOT, respectively. GaAs/InP(111) has a smaller density of states than Si (100), hence loses its advantage over Si at ultra thin EOT values. GaAs/InP(111) exhibits the highest on-current; only at $\simeq 0.3$ nm EOT is Si comparable. At EOT=0.5 nm, considered feasible for MOSFETs at $L_g=5$ nm, the GaAs/InP(111) design delivers 8.5% higher I_{on} than Si(100) DG MOSFETs and 18% higher than Si(100) SG MOSFETs confirming the efficacy of the Γ -L channel designs (see [8]).

V. CONCLUSIONS

GaAs/ $AlAs_{0.56}Sb_{0.44}$ /InP (111) channel designs are presented for high current MOSFETs. Using $sp^3d^5s^*$ -SO bandstructure calculations it is showed that at $\simeq 2$ nm body thickness L valley minima can be achieved in GaAs/ $AlAs_{0.56}Sb_{0.44}$ /InP (111) quantum wells. Later, using the top-of-the-barrier transport model it is shown that GaAs/ $AlAs_{0.56}Sb_{0.44}$ /InP (111) orientation outperforms both Si(100) and GaAs/ $AlAs_{0.56}Sb_{0.44}$ /InP(100) at similar channel thicknesses for EOT >0.5nm. These results could be useful in design of future nanoscale device applications.

VI. ACKNOWLEDGMENT

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