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Ultrafast Submicron Thermal Characterization of Integrated Circuits

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Abstract- Static and dynamic hot spots limit the performance and reliability of electronic devices and ICs. We show that transient thermoreflectance imaging using a CCD camera can measure temperature distribution in chips with 0.1 °C temperature, 100 nanosecond time, and submicron spatial resolution. It is possible to measure the temperature on metal interconnects in wire-bonded chips and, with through-the-substrate infrared illumination, at the transistor level in flip-chip packages. Recent results in transient thermal imaging of GaN transistors, ESD protection devices, solar cells, and LEDs are presented. We show it is possible to identify non-uniform temperature rise and defects in 200 to 300 nm interconnect vias that have been stressed at high temperatures. Power blurring techniques can be used to obtain transient temperature profiles in packaged IC chips with a calculation time orders of magnitude faster than finite element analysis. The technique is well suited to solve the inverse problem and extract the power dissipation profile from the measured thermal map.

I. SUMMARY

Miniaturization of devices and circuits and the increased operation speeds have exacerbated localized heating problems. Steady-state and transient characterization of temperature distribution in devices and interconnects are important for performance and reliability analysis. In this talk we review recent developments in ultrafast submicron imaging techniques. Many properties of materials depend on temperature and they can be exploited for local temperature measurement. An overview of different thermal measurement techniques is given in [1] (see table 1) and more specifically thermoreflectance imaging is described more in details in [2] and [3].

For the characterization of active devices, thermal maps can provide useful information about the power dissipation profile, hot spots, and manufacturing or material defects before the device completely fails. Transient thermal imaging can show temperature variation in switching devices under pulsed operation. This can be used to identify buried defects or help to extract the thermal resistance/capacitance in 3D packages. For optoelectronic devices such as LEDs and solar cells, an additional scheme is required to separate electro-luminescence and the reflected illumination used for thermoreflectance. The integrated circuits require high spatial resolution. At the same time, the structure of multiple metal layer interconnects makes it difficult to characterize active device junction temperature. When there is optical access, with the through silicon substrate thermal imaging, one can directly measure the active transistor region. The use of solid immersion lens for back-side through substrate imaging can increase the numerical aperture of the optical system and improve the spatial resolution down to microns for IR (3-5 microns wavelength) and couple of hundred nanometers for near IR thermoreflectance (1.1-1.5 microns wavelength).

The challenge in obtaining high quality thermal images arises when one considers the magnitude of the weak temperature dependent reflection coefficient (thermoreflectance effect) in metals and semiconductors. The thermoreflectance coefficient is on the order of 10^-4 to 10^-5 per degree Kelvin for most materials [2]. This coefficient is wavelength, material, and even surface texture dependent, and in-situ calibration (e.g. with a thermocouple) is necessary. To capture the thermoreflectance signal with reasonable signal-to-noise ratio, an active device is thermally cycled at a known frequency and lock-in technique (phase sensitive detection) is used. Images are detected by typically a CCD. The high temperature sensitivity, down to 5-10mK, for steady-state measurements provides the opportunity to study the spatial distribution of current flow (Joule heating) in the device and identify defects before significant hot spots develop. Finally, the ultrafast time resolution is important in high speed devices or in studying transient effects such as Electrostatic Discharge (ESD). Transient thermal imaging with resolution down to 100 nanosecond [4] (800 picoseconds [5]) has been achieved with pulsed LED (semiconductor laser) illumination, respectively.

<table>
<thead>
<tr>
<th>Method</th>
<th>Resolution x(μm)</th>
<th>t(K)</th>
<th>t(sec)</th>
<th>Imaging?</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>μ thermocouple</td>
<td>50</td>
<td>0.01</td>
<td>0.1-1</td>
<td>No</td>
<td>Contact method</td>
</tr>
<tr>
<td>IR Thermography</td>
<td>3-10</td>
<td>0.02-1</td>
<td>1μ</td>
<td>Yes</td>
<td>Emissivity dependent</td>
</tr>
<tr>
<td>Lockin IR Thermography</td>
<td>3-10</td>
<td>10μ</td>
<td>NA</td>
<td>Yes</td>
<td>Need cycling</td>
</tr>
<tr>
<td>Liquid Crystal Thermography</td>
<td>2-5</td>
<td>0.5</td>
<td>100</td>
<td>Yes</td>
<td>Only near phase transition (aging issues)</td>
</tr>
<tr>
<td>Thermoreflectance</td>
<td>0.3-0.5</td>
<td>0.08</td>
<td>800</td>
<td>Yes</td>
<td>Need cycling</td>
</tr>
<tr>
<td>Optical Interferometry</td>
<td>0.5</td>
<td>100μ</td>
<td>6n-0.1μi</td>
<td>Scan</td>
<td>Indirect measurement (expansion)</td>
</tr>
<tr>
<td>Micro Raman</td>
<td>0.5</td>
<td>10n</td>
<td>Scan</td>
<td>3D T-distribution</td>
<td></td>
</tr>
<tr>
<td>Near Field (NSOM)</td>
<td>0.05</td>
<td>0.1-1</td>
<td>0.1μi</td>
<td>Scan</td>
<td>S/N dependent Tip/sample interaction</td>
</tr>
<tr>
<td>Scanning thermal microscopy</td>
<td>0.05</td>
<td>0.1</td>
<td>10-100μi</td>
<td>Scan</td>
<td>Contact method surface morphology</td>
</tr>
</tbody>
</table>
Temperature map measurement of an IC chip is a well-established and powerful technique that allows chip designers and process engineers to identify strong temperature non-uniformity (hot-spot) locations where there are fabrication failures. However, a temperature map, by itself, often fails to provide enough information for IC thermal inspection, due to the fact that the formation of temperature non-uniformities can be highly complex. Note that, even one single hot-spot is often contributed by multiple discrete heat sources, and therefore the power dissipation profile has to be obtained and studied in order to achieve effective thermal management.

Typically, chip designers provide the power map to package engineers to calculate the temperature map of the chip taking into account thermal properties of the die and the package. Since the characteristic length scales of the transistors, various functional units, the die, and the package range from sub-microns to centimeters, accurate thermal analysis is done using sophisticated finite element solvers and multi grid algorithms. To identify fabrication or device failures, the calculated temperature map of the IC chip is compared to a measured one. For a more quantitative analysis of power dissipation and its spatial extent in the hot-spots, a novel iterative method is recently proposed where the temperature map is calculated for a series of power maps and the best match is experimentally identified [6]. However, these methods are accurate and useful only when few heat sources are in the chip. Unfortunately, in the more complex case of commercial ICs composed of numerous heat sources, the number of parameters involved becomes prohibitively large making this problem unsolvable even if the adaptive masking technique [6] is utilized. Also, there have been some attempts to calculate the power map from the measured temperature map by implementing an experimental direct inverse filter [7]. This was done using extensive characterization of the dies by applying point heat sources at various locations and measuring the resulting temperature maps. However, since the measurements are noisy and the problem is ill-posed, the results obtained from such direct inverse filtering technique will always be suboptimal.

Recently, by using an analogy with image processing and restoration, a fast and optimal numerical solution to this inverse problem was proposed, which takes input from the temperature map and outputs the power map [8,9]. Unlike the method in [6,7], this technique is much less sensitive to noise and outliers. This approach is inspired from a recent robust image restoration method. The procedure for applying this new analysis tool requires two simple steps: (1) Estimating the heat point spread function by using an finite element software while using a scaling function to address the boundary problems. This step requires some knowledge about the chip and package dimension and IC’s material thermal properties, which are commonly included in the chip/package design files. (2) Exploiting the estimated temperature map and solving an inverse problem to obtain the power map. The inverse problem was solved through a maximum a posteriori (MAP) estimation framework in which a robust regularizer is used to stabilize the solution.

REFERENCES