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Experimental Investigation of Border Trap Generation in InGaAs nMOSFETs With Al₂O₃ Gate Dielectric Under PBTI Stress

Guangfan Jiao, Chengjun Yao, Yi Xuan, Member, IEEE, Daming Huang, Peide D. Ye, and Ming-Fu Li

Abstract—The reliability performance of InₓGa₁₋ₓAs n-type metal–oxide–semiconductor field-effect transistors with Al₂O₃ gate dielectric under positive-bias temperature instability stress is investigated systematically. A model of stress-induced border traps was proposed to interpret all charge pumping and I–V experimental results excellently. The stress-induced border traps include recoverable donor traps and permanent acceptor traps with respective energy densities \( \Delta D_{\text{Donor}}(E) \) and \( \Delta D_{\text{Acceptor}}(E) \). The shapes of \( \Delta D_{\text{Donor}}(E) \) and \( \Delta D_{\text{Acceptor}}(E) \) have been extracted from experimental data. \( \Delta D_{\text{SOX}}(E) \) mainly distributes in the conduction band of InGaAs with a tail extending to the mid-gap, whereas \( \Delta D_{\text{SOX}}(E) \) has a large distribution inside the energy gap and extends to the conduction band. The high density of \( \Delta D_{\text{Donor}}(E) \) in the energy gap induces large degradation in the off-current, which is particularly serious when the In composition \( x \) is raised to 0.65.

Index Terms—Border traps, InGaAs n-type metal–oxide–semiconductor field-effect transistors (nMOSFETs), off-current, positive-bias temperature instability (PBTI).

I. INTRODUCTION

InGaAs has attracted much attention in the recent years as the channel material in n-type metal–oxide–semiconductor field-effect transistors (nMOSFETs) because of its higher electron mobility than that of silicon [1]–[7]. However, there are only a few studies reporting the reliability of InGaAs nMOSFETs [4], [6], [8]. We have investigated the reliability performance of InGaAs nMOSFETs under positive-bias temperature instability (PBTI) stress [9]. This paper elaborates more details than what was presented in [9].

II. DEVICES AND EXPERIMENTS

InₓGa₁₋ₓAs nMOSFETs with \( x = 0.53 \) and 0.65 are used in this paper. The planar device structures and fabrication processes of these devices were illustrated in [3]. The transistors have channel width \( W = 100 \mu \text{m} \), Al₂O₃ gate dielectric grown by Atomic Layer Deposition with physical thickness of 8 nm, and Ni/Au metal gate. P-type channel doping is about \( 1 - 2 \times 10^{17} \text{ cm}^{-3} \). Channel length \( L \) is 2–40 \( \mu \text{m} \) with specific value being marked in the relevant figure captions.

Current–voltage I–V and charge pumping (CP) measurements are carried out to characterize PBTI using an Agilent 4156C parameter analyzer, a pulse generator 81110A, and a Cascade probe station. In the I–V measurements, \( V_{G} \) is set to 50 mV, whereas the source and substrate are grounded (\( V_{S} = V_{B} = 0 \text{ V} \)). In the conventional CP measurements [10], the source, drain, and substrate are all grounded. The CP current \( I_{cp} \) is measured from the source/drain. During the PBTI stress phase, the gate stress voltage \( V_{G} = 3.0 \text{ V} \), whereas \( V_{S} = V_{D} = V_{B} = 0 \text{ V} \). During the recovery phase, all the electrodes are grounded. All measurements are taken at room temperature. More than 20 devices for \( x = 0.53 \) and 0.65 nMOSFETs were measured, with the typical characteristics presented in this paper.

III. EXPERIMENTAL RESULTS

A. CP Experiments

Fig. 1(a) shows the time evolution of the CP currents \( I_{cp} \) and the areal density of the stress-induced interface traps \( \Delta N_{it} \) for the In₀.65Ga₀.35As nMOSFET during the PBTI stress phase and the following recovery phase. The interface trap density \( N_{it} \) is extracted from \( I_{cp} \) using the following formula [10]:

\[
N_{it} = I_{cp} / (f q A_{G})
\]

(1)

where \( q \) is the proton charge, \( f \) is the pulse frequency, and \( A_{G} \) is the gate area. From the \( I_{cp} \) of the fresh device, the process-induced interface trap density \( N_{it}^{0} \) is derived to be about \( 9 \times 10^{12} \text{ cm}^{-2} \). The stress-induced interface trap density \( \Delta N_{it} \) is only about \( 1.3 \times 10^{11} \text{ cm}^{-2} \) after 500-s stress. It decreases in the recovery phase. The inset in Fig. 1(a) illustrates that the time evolution of \( \Delta N_{it} \) in the stress phase shows a power law \( \Delta N_{it} \propto t^{\gamma} \) with index \( \gamma = 0.22 \), close to the index \( n \) of Si/SiON pMOSFET under negative bias temperature instability stress with similar CP measurement [11], [12].

Fig. 1(b) shows the frequency dependence of \( N_{it}^{0} \) and \( \Delta N_{it} \) estimated by CP experiments. By changing the CP frequency from 100 to 1 kHz, \( N_{it}^{0} \) increases by a factor of 1.3, whereas \( \Delta N_{it} \) increases by a factor of 2.5. The results indicate that the
stress-induced traps contain a major component of slow border traps (oxide traps near the interface) that can exchange electrons with the channel slowly. Therefore, the measured $\Delta N_{it}$ has a strong CP frequency dependence, and the stress-induced traps are seriously underestimated by CP measurement [13]. We would thus denote the stress-induced traps by $\Delta N_{SOX}$ rather than $\Delta N_{it}$. Using the method illustrated in [13], the volume density of the stress-induced border traps can be estimated from Fig. 1(b) to be $\sim 5 \times 10^{18} \text{ cm}^{-3}$.

**B. $I_s-V_g$ Experiments**

Fig. 2 shows the $I_s-V_g$ and $I_d-V_g$ characteristics measured from devices with $x = 0.65$ before stress (initial state, I lines), after 500-s PBTI stress (S lines), and with additional 500-s recovery (R lines). Both $I_s-V_g$ and $I_d-V_g$ show the same characteristics except in the “off-current” region. In this region, $I_d$ is larger than $I_s$ and is confirmed to be the drain leakage flowing to the substrate when a $V_g$ of 50 mV is applied. This leakage is further discussed in Section V. In the following investigation, we will mainly use $I_s-V_g$ as the transfer characteristic.

Fig. 3 shows the $I_s-V_g$ characteristics measured before stress (initial state, I lines), after 500-s PBTI stress (S lines), and with additional 500-s recovery (R lines) for $x = 0.65$ and 0.53 devices. There are two points worth to be noticed. First, by comparing the I and S lines, $\Delta V_g$ extracted at low $I_s$ [subthreshold (SS) region] is negative after stress, accompanied by a degradation in SS swing $S$, as shown in Figs. 3–5(a).

$\Delta V_g$ extracted at high $I_s$ (“ON-current” region) is positive after stress, accompanied by a degradation in transconductance $G_m$, as shown in Figs. 3–5(b). There is a crossing point between the I and S lines, denoted by $C$, at which $\Delta V_g = 0$. Second, by comparing the I and R lines, $\Delta V_g$ extracted at low $I_s$ in the SS region is positive, with a degradation in $S$, as shown in Figs. 3–5(a).

The strange thing is that, at high $I_s$, $\Delta V_g$ increases...
further in the recovery phase, as shown in Figs. 3 and 4, and it saturates gradually toward a constant value.

IV. BORDER TRAP MODEL

At first glance at the $I_s$–$V_g$ curves in Fig. 3, one may consider the stress-induced donor traps to be responsible for the negative $\Delta V_g$ and the degradation in $S$ in the SS region [comparing the I and S lines in Figs. 3 and 11(a) in [7]]. One may also consider the stress-induced acceptor traps or the fixed charge to be responsible for the positive $\Delta V_g$ in the high $I_s$ region and the degradation in transconductance $G_m$, as shown in Figs. 3–5(b). However, there are several conflicting points that have to be considered in the analyses presented in [9]. The key point is that the stress-induced donor traps estimated from $\Delta V_g$ shown in Fig. 3 are in the range of $10^{12}$ cm$^{-2}$ (see Section VI), which is one order of magnitude higher than that estimated from the CP measurement shown in Fig. 1(a). Combining with the results shown in Fig. 1(b), it is obvious that the stress-induced traps are mainly not the conventional interface traps, but the border traps near the interface in the oxide layer. The electron capture or emission from the border traps cannot follow the fast change of the surface potential in the CP measurement. As a result, $\Delta N_{SOX}$ is seriously underestimated by the CP measurement [13]. However, electron trapping (detrapping) can follow the slow change of the surface potential in the $I_s$–$V_g$ measurement and cause the change in $V_g$ and the degradation in $S$ in the SS region, acting as a role similar to conventional interface traps [14].

We now compare the R lines with I lines in Fig. 3 in the SS region. There are two possible cases to be considered after the recovery phase. 1) There are recoverable donor traps and permanent acceptor traps, which can explain the positive $\Delta V_g$ and the S degradation [see the difference between the I and R lines and compare it with Fig. 11(b) in [7]]. 2) There are recoverable donor traps and fixed negative oxide charge. In the case 2, the R lines in Fig. 3 are the combined effect of the fixed charge and the residual donor traps. The fixed charge induces a parallel positive shift in the $I_s$–$V_g$ curve. The residual donor traps induce the degradation in $S$ and the negative $\Delta V_g$. If it is case 2, the residual donor traps must have high enough density to compensate the positive shift induced by the fixed charge. As a result, the net $\Delta V_g$ is close to zero only when $I_s$ is very low ($4 \times 10^{-9}$ A for $x = 0.65$ devices and $3 \times 10^{-10}$ A for $x = 0.53$ devices), as shown in Fig. 3. Case 2 should be ruled out because the recovered OFF-current $I_{off}$ (discussed in Section V) reveals that the stress-induced donor traps mostly recovered in the end of the recovery phase. These results are in conflict with case 2, but in support of case 1.

A unified and natural border trap model has emerged to explain perfectly all the details of the aforementioned experimental results, as shown in Fig. 6. The main points of this model are as follows:

1) The stress-induced slow border traps with density $\Delta D_{SOX}$ include recoverable donor traps with energy density $\Delta D_{SOX}^{Donor}(E)$ and permanent acceptor traps with energy density $\Delta D_{SOX}^{Acceptor}(E)$.

2) The recoverable $\Delta D_{SOX}^{Donor}(E)$ not only distributes within the InGaAs energy gap but also extends to the conduction band. The donor traps within the energy gap induce the negative $\Delta V_g$ and the $S$ degradation in the stress phase and the recovery in the SS region during the recovery phase [Figs. 3–5(a)]. The donor traps in the conduction band induce the strange phenomena of continuous increase of positive $\Delta V_g$ in the recovery phase (Figs. 3 and 4).

3) The permanent $\Delta D_{SOX}^{Acceptor}(E)$ mainly distributes in the conduction band with a tail extending to the energy gap. The acceptor traps in the conduction band induce the positive $\Delta V_g$ and the degradation in $G_m$ in the high $I_s$ region in the stress phase [Figs. 3–5(b)]. The acceptor traps in the energy gap result in the positive $\Delta V_g$ and the small $S$ degradation in the SS region at the end of the recovery phase [Figs. 3–5(a)].

4) All the border traps are seriously underestimated by the CP measurements when they cannot follow the fast change of the surface potential during the CP measurements.

V. OFF-CURRENT DEGRADATION

In this section, we concentrate on the degradation behavior of the OFF-current in the range of $V_g = −0.8$ to $−1.0$ V, denoted by $I_{off}$. As shown in Fig. 3, for $V_g = −0.8$ to $−1.0$ V, $I_{off}$ is nearly independent of $V_g$. Fig. 7 shows the time evolutions of the $I_{off}$ change ($\Delta I_{off}$) at a constant gate voltage $V_g = −0.8$ V in the stress and recovery phases for $x = 0.65$ and 0.53 devices, respectively. As shown in Fig. 3, both $I_{off}$ and $\Delta I_{off}$ show a large quantitative difference between $x = 0.53$ and 0.65 devices. For $x = 0.53$ devices, the $I_{off}$ is in the range of $10^{-10}$ A in the initial state. It increases by a factor of 2–3 after 500-s stress. For $x = 0.65$ devices,
however, the $I_{s}^{\text{off}}$ is in the range of $10^{-9}$ A in the initial state. It increases by two orders of magnitude after 500-s stress.

Fig. 8 illustrates the $\Delta I_{s}^{\text{off}} - V_d$ curves measured after 500-s stress and 500-s recovery for $x = 0.53$ and 0.65 devices. If $\Delta I_{s}^{\text{off}}$ is due to the change of the surface potential pinning [8], [15], $\Delta I_{s}^{\text{off}}$ should be the diffusion current of minority carriers in the SS region and should satisfy the following equation [14]:

$$\Delta I_{s}^{\text{off}} = A \left[ 1 - \exp(-qV_d/kT) \right]$$

(2)

which saturates when $V_d > 3$ kT/q $\approx$ 0.1 V. As shown in Fig. 8(a), for $x = 0.53$ devices with $I_{s}^{\text{off}}$ in the range of $10^{-10}$ A, $\Delta I_{s}^{\text{off}}$ measured after 500-s stress satisfies (2). The results imply that the degradation (recovery) of $\Delta I_{s}^{\text{off}}$ is due to the generation (recovery) of a large density of donor traps in the energy gap, causing the change of the surface potential pinning. However, as shown in Fig. 8(b) for $x = 0.65$ devices with $I_{s}^{\text{off}}$ in the range of $10^{-9} - 10^{-7}$ A, $\Delta I_{s}^{\text{off}}$ measured after 500-s stress does not satisfy (2). In that case, $\Delta I_{s}^{\text{off}}$ is likely due to the drift of electrons in a surface conduction path across the source and drain, and therefore, the $I_{s}^{\text{off}} - V_d$ relationship is similar to the case of an ohmic resistance. Fig. 9 shows the $I_d$ and $I_s$ versus $V_d$ curves ($V_g = -0.8$ V) for the initial state, after 500-s stress, and after 500-s recovery for $x = 0.53$ and 0.65 devices. The $I_d$ in the both kinds of devices are pretty large ($>10^{-7}$ A) when $V_d > 0.8$ V. A major component of the $I_d$ is the pn-junction reverse bias leakage $I_{jl}$. In this paper, the transistor channel length $L_s$ is near 4–8 $\mu$m, with a similar drain size $L_d$ along the channel direction. Since $I_{on}$ and $I_{jl}$ are proportional to $L_s^2$ and $L_d$, respectively, when $L_s$ and $L_d$ are reduced to the nanometer range, $I_{on}/I_{jl}$ can be improved by several orders of magnitude. $I_{jl}$ can be further improved by reducing s/d activation temperature [3] or by using an implant-free 3-D structure [16]. Figs. 8(b) and 9(b) show that for the $x = 0.65$ devices, about one-half of the stress-induced drain current flows to the source through a channel surface conduction path. This surface conduction path could be due to the hopping conduction [17] between the neighboring donor traps induced by the stress. Although a high In mole fraction $x$ can improve the ON-current performance of In$_x$Ga$_{1-x}$As nMOSFETs, the large $\Delta I_{s}^{\text{off}}$ in $x = 0.65$ devices raises a new challenge for developing III–V MOSFET technology for low standby power application. Further improvement in high-$k$/InGaAs interface quality, in particular, reducing the interface trap and border trap densities within the lower half energy gap, is needed to suppress the OFF-current degradation of InGaAs MOSFETs. New passivation techniques and alternative high-$k$ dielectrics are being explored.

VI. Extractions of Border Trap Densities From Experiments

We can use the $I_s - V_g$ curves in Fig. 3 to estimate the energy distribution of stress-induced border traps based on the following assumptions for the trap model described in Section V. 1) At the end of 500-s stress, there are both stress-induced donor traps and acceptor traps in the devices. 2) At the end of 500-s recovery, the stress-induced donor traps fully recover while the acceptor traps are permanent.

A. Method I—Extraction From $\Delta V_g$ in the $I_s - V_g$ Curves

At first, $\Delta V_g$ is extracted from the I and R lines as a function of $I_s$ for all the current ranges shown in Fig. 3. The result is denoted by $\Delta V_g^{\text{III}}(I_s)$. Since only the acceptor traps remain after 500-s recovery, the density $\Delta N_{\text{SOX}}^{\text{Accept}}(I_s)$ of
negatively charged acceptor traps as a function of \( I_s \) can be obtained by

\[
\Delta N_{SOX}^{-\text{Acceptor}}(I_s) = (C_{OX}/q)\Delta V_g^{IR}(I_s) \tag{3}
\]

where \( C_{OX} \) is the gate oxide capacitance per unit area and is near \( 10^{-6} \) F/cm\(^2\) estimated using 8-nm Al\(_2\)O\(_3\) gate dielectric. The density difference of negatively charged acceptor traps and positively charged donor traps \( \Delta N_{SOX}^{-\text{Acceptor}}(I_s) - \Delta N_{SOX}^{+\text{Donor}}(I_s) \) can be extracted from the I and S lines, shown in Fig. 3, by

\[
\Delta N_{SOX}^{+\text{Donor}}(I_s) = (C_{OX}/q)\Delta V_g^{IS}(I_s) \tag{4}
\]

where \( \Delta V_g^{IS}(I_s) \) is the \( V_g \) difference between the S and I lines at the same \( I_s \). From (3) and (4), the density of positively charged donor traps can be obtained from

\[
\Delta N_{SOX}^{+\text{Donor}}(I_s) = (C_{OX}/q)\Delta V_g^{IR}(I_s) - (C_{OX}/q)\Delta V_g^{IS}(I_s). \tag{5}
\]

Next, the surface potential \( \psi_s \) and the energy difference \( E = E_F - E_V \) at the interface as a function of \( I_s \) can be calculated by SILVACO Atlas simulation tool for In\(_x\)Ga\(_{1-x}\)As nMOSFETs. The device structures for simulation are the same as the real devices reported in [3]. From these simulations, the relationship between \( I_s \) and the energy \( E(I_s) \) is obtained. Combining (3), (5), and \( E(I_s) \), we obtain \( \Delta N_{SOX}^{+\text{Donor}}(E) \) and \( \Delta N_{SOX}^{-\text{Acceptor}}(E) \) as functions of \( E \). The energy distribution of donor and acceptor traps can be obtained from

\[
\Delta D_{SOX}^{+\text{Donor}}(E) = -\frac{d\Delta N_{SOX}^{+\text{Donor}}}{dE} \tag{6}
\]

\[
\Delta D_{SOX}^{-\text{Acceptor}}(E) = \frac{d\Delta N_{SOX}^{-\text{Acceptor}}}{dE}. \tag{7}
\]

The results are plotted in Fig. 10.

There are two possible error sources in obtaining the donor and acceptor trap densities using the above derivations. 1) The mobility degradation induced \( \Delta V_g \) in the strong inversion region has been overlooked [18]. Therefore, both donor and acceptor trap densities may be overestimated, giving rise to the distortions of the curves in the horizontal direction in Fig. 10.

B. Method II—Extraction From the Degradation in \( S \) in the SS Region

We can also extract part of the energy distribution of stress-induced traps from the \( S \) in the SS region. On the one hand, since only the acceptor traps remain after 500-s recovery, their energy distribution \( \Delta D_{SOX}^{\text{Acceptor}}(I_s) \) can be obtained from

\[
\Delta D_{SOX}^{\text{Acceptor}}(I_s) = [C_{OX}/(qkT\ln10)]\Delta S^{\text{IR}}(I_s) \tag{8}
\]

where \( \Delta S^{\text{IR}}(I_s) \) is the difference in \( S \) extracted between the R and I lines shown in Fig. 3. From (8) and (9), the energy distribution of donor and acceptor traps \( \Delta D_{SOX}^{\text{Accepter}}(I_s) + \Delta D_{SOX}^{\text{Donor}}(I_s) \) can be extracted from the I and S lines using

\[
\Delta D_{SOX}^{\text{Accepter}}(I_s) + \Delta D_{SOX}^{\text{Donor}}(I_s) = [C_{OX}/(qkT\ln10)]\Delta S^{\text{IS}}(I_s). \tag{9}
\]

By combining (8), (10), and the simulation result \( E(I_s) \) described in Method I, we obtain \( \Delta D_{SOX}^{\text{Donor}} \) and \( \Delta D_{SOX}^{\text{Accepter}} \) as functions of energy \( E \). The results shown in Fig. 11 are only in a narrow energy region corresponding to the SS region in the \( I_s-V_g \) curves. However, the trap energy distributions estimated from Methods I and II are consistent in the same energy range.
VII. CONCLUSION

We have presented CP and $I_s-V_g$ degradations under PBTI stress for In$_{0.65}$Ga$_{0.35}$As nMOSFETs with $x = 0.53$ and 0.65. A model for the slow border traps induced by stress near the Al$_2$O$_3$/InGaAs interface is proposed to perfectly interpret all experimental results in detail. The stress-induced border traps include recoverable donor traps with energy density $\Delta D_{\text{DONOR}}^{\text{SOX}}(E)$ and permanent acceptor traps with energy density $\Delta D_{\text{ACCEP}}^{\text{SOX}}(E)$, which can be estimated from the measured $I_s-V_g$. The permanent $\Delta D_{\text{ACCEP}}^{\text{SOX}}(E)$ distributes mainly in the conduction band of InGaAs with a tail extending to the mid-gap. It is responsible for the positive $\Delta V_g$ in the ON-current region of the $I_s-V_g$ curve after stress. The recoverable $\Delta D_{\text{DONOR}}^{\text{SOX}}(E)$ has a large distribution in the InGaAs energy gap and extends to the conduction band. It is responsible for the negative $\Delta V_g$ in the SS region, the $S$ degradation, the $I_{\text{OFF}}$ degradation of the $I_s-V_g$ curve in the stress phase, and continuous degradation of positive $\Delta V_g$ in the ON-current region in the recovery phase. The $\Delta D_{\text{DONOR}}^{\text{SOX}}(E)$ is completely recoverable in the recovery phase. The large $I_{\text{OFF}}$ degradation under stress for In$_{0.65}$Ga$_{0.35}$As nMOSFETs exposes new challenges in the technology development of InGaAs nMOSFETs.

REFERENCES


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Ming-Fu Li received the degree from Fudan University, Shanghai, China, in 1960. After graduation, he was with the Department of Technical Physics, University of Science and Technology, Hefei, China. He joined the Graduate School, Chinese Academy of Sciences, Beijing, China, in 1978 and became a Professor in 1986. He was a Visiting Scholar with the University of Illinois, Urbana, from 1979 to 1981, and a Visiting Scientist with the University of California, Berkeley, from 1986 to 1987 and from 1990 to 1991. In 1991, he joined the National University of Singapore (NUS), Singapore, where he became a Professor in the ECE Department. He was a founding member of the Silicon Nano-Device Laboratory at NUS. He joined Fudan University, Shanghai, in 2006 as a Professor in the Microelectronics Department. He has published over 400 research papers and three books, including Modern Semiconductor Quantum Physics (World Scientific, 1994) and Selected Semiconductor Research (Imperial College Press, 2011). He has served on numerous committees in international conferences worldwide, including the premier International Conference on the Physics of Semiconductors and premier electron device conferences IEDM and IRPS.