Tunable, Dual-Gate, Silicon-on-Insulator (SOI) Nanoelectromechanical Resonators

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Yu, Lin; Pajouhi, Hossein; Nelis, Molly R.; Rhoads, Jeffrey F.; and Mohammadi, Saeed, "Tunable, Dual-Gate, Silicon-on-Insulator (SOI) Nanoelectromechanical Resonators" (2012). Birck and NCN Publications. Paper 1109.
http://dx.doi.org/10.1109/TNANO.2012.2212028

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Tunable, Dual-Gate, Silicon-on-Insulator (SOI) Nanoelectromechanical Resonators
Lin Yu, Hossein Pajouhi, Molly R. Nelis, Member, IEEE, Jeffrey F. Rhoads, and Saeed Mohammadi, Senior Member, IEEE

Abstract—Resonant nanoelectromechanical systems (NEMS) have the potential to have significant impact in mass sensing, signal processing, and field detection applications, if the challenges associated with processing, material, and geometric variability can be mitigated. The research presented here details a breakthrough in the design and development of resonant NEMS aimed at addressing these challenges. Specifically, this study details the fabrication, characterization, and tuning of dual-gate silicon nanoelectromechanical resonators, which are transduced electrostatically and realized with close to 100% yield. These devices are fabricated on a silicon-on-insulator (SOI) substrate using only top-down microfabrication techniques and can be easily integrated with SOI-CMOS transistors, enabling the development of fully integrated CMOS-NEMS with highly tunable nonlinear frequency response characteristics.

Index Terms—Dual-gate nanoresonators, electrostatic tuning, nonlinear tuning, silicon nanowire.

I. INTRODUCTION

NAOLOCMECHANICAL systems (NEMS) are elicitting great interest because they allow access to microwave frequencies and nanosecond response times, amongst other pertinent metrics [1]–[5]. These unprecedented properties are fueling the potentially ground-breaking application of NEMS in analog and RF signal processing [6]–[9], nanomechanical electrometry [10], and chemical and biological sensing [11]–[22]. To date, most NEMS resonators have been fabricated using bottom-up carbon nanotube or nanowire (NW) synthesis, followed by low-temperature top-down microfabrication [2]–[4], [22]–[28]. While this approach can be adopted for post-CMOS device fabrication, it is quite susceptible to processing, material, and geometric variability [29], which leads to irreproducible near-resonant response characteristics and, ultimately, prohibits predictive device design.

Resonant NEMS devices fabricated using only a top-down approach have also been reported [10], [30]–[34]. However, with perhaps one exception [34], these devices cannot be fabricated and integrated as a single-chip solution in mass sensing or signal processing applications, as technologies that are not based on Si resonators (including piezoelectric NEMS devices) are generally incompatible with CMOS processing, and devices which rely on magnetomotive or optical transduction typically require additional hardware to fully characterize their near-resonant response.

This study describes the design, development, and characterization of electrostatically transduced nanoelectromechanical resonators which are aimed at addressing the aforementioned constraints and are fabricated using only top-down microfabrication, as realized via a silicon-on-insulator (SOI) process flow. SOI-CMOS technology is widely employed in the development of low-power digital microprocessors, such as those used in mobile computing and communication platforms. The selective nature of silicon/silicon dioxide (Si/SiO$_2$) etching which enables the fabrication of these devices also allows for the development, implementation, and on-chip integration of SOI-NEMS. The dual-gate silicon devices detailed here are reproducible and reliable, have been fabricated with near 100% yield (excluding the outer perimeter of the chip), and can be easily integrated with SOI-CMOS transistors, enabling the development of fully integrated CMOS-NEMS with highly tunable in-plane and out-of-plane, nonlinear frequency response characteristics.

II. DEVICE FABRICATION

SOI wafers with a 110 nm device layer and 144 nm buried oxide layer are used in this study. The wafers are slightly doped with boron ($\rho = 14–20 \, \Omega \cdot \text{cm}$). Prior to device fabrication, the SOI wafers are implanted with phosphorous. An impurity dose of $1 \times 10^{13} \, \text{cm}^{-2}$ and an implantation energy of 40 keV are employed to ensure that the peak concentration (with an estimated doping density of $10^{18} \, \text{cm}^{-3}$) appears in the middle of the device layer. After ion implantation, the wafers are annealed at 1050 °C in a nitrogen ambient for 60 s using a rapid thermal annealing (RTA) furnace. The RTA anneal allows the dopant, namely phosphorous, to diffuse into the substitutional lattice sites where they are electrically active.

The silicon nanoresonators are fabricated following the dopant activation. First, a layer of hydrogen silsesquioxane (HSQ) is spin-coated on top of the device layer. The silicon nanoresonators are then patterned with e-beam lithography.
using HSQ as a high-resolution, negative-tone inorganic electron-beam resist. After development, the exposed HSQ remains on the wafer, which is then introduced into a reactive ion process. After plasma etching, the wafer is dipped in buffered oxide etchant (BOE) for 30 s to remove the HSQ. Another e-beam lithography process is then performed to define the source, drain, and side-gate electrodes. This is followed by metal deposition and a lift-off process. The thick metal contacts are realized with 30 nm chrome and 200 nm gold in order to achieve good step coverage of the silicon nanoresonators.

Note that a small window is patterned between source and drain with another e-beam lithography process and the SiO$_2$ beneath the resonators is etched in BOE. Finally, the suspended resonators are released through the use of a critical point drying (CPD) process. Fig. 1 shows the device fabrication process (a)–(f) and a typical atomic force microscopic image of a suspended silicon nanoresonator (g) fabricated with this process.

A scanning electron micrograph of a representative SOI-NEMS device is shown in Fig. 2. This nanoresonator features a near-rectangular cross section, measuring approximately 110 nm high and 120 nm wide, and is suspended approximately 144 nm above the bottom gate. Note that phosphorus implantation is used to enhance the conductance of the Si nanoresonators and reduce their contact resistance—key factors in reducing the thermoelectric noise floor of SOI-NEMS. Also of note is the unique dual-gate nature of this system, which allows in-plane and out-of-plane modes of vibration to be selectively actuated by mechanical motion and attributable to the conductance and piezoresistive changes caused by this motion [4], [38]. Mathematically, this results in a detectable mixing current given by

$$ I_{\Delta \omega} (\omega) = \frac{dG}{dV_g} \left[ V_{ds}^2 + \frac{C'_g(z(\omega))}{C_g} V_g V_{ds} \right] $$

where $z(\omega)$ denotes the deflection of the center of the nanoresonator with respect to its equilibrium position, $G$ is the nanoresonator’s conductance, $C'_g$ and $C_g$ are the differential and absolute capacitances between the gate and device, respectively, and $V_g$ and $V_{ds}$ are the amplitudes of the gate bias and ac voltage applied to the drain, respectively. Note that the piezoresistive strain varies at twice of the resonant frequency of the device and two distinct dc biases are applied on the side gate and back gate, and two ac signals, a pure sinusoid with frequency $\omega$ and another with carrier frequency $\omega$ and sinusoidal amplitude modulation at $\Delta \omega$, are applied to the drain electrode, facilitating motion and measurement readout. Due to the capacitance change induced by mechanical motion, the two ac signals mix together when their frequencies approach the natural frequency of the nanoresonator, enabling the vibration of the nanoresonator to be directly measured via the down-mixed current at the intermediate frequency $\Delta \omega$ using a lock-in amplifier at the source port. The lock-in amplifier is locked at frequency $\Delta \omega$ (1 kHz) and a Labview-based automated measurement setup is used to collect data and graph the results. As noted in subsequent sections, the detectable mixing current at frequency $\Delta \omega$, which is related to the physical displacement of the device, has two dominant components: a background response induced by the ac voltage applied to the drain and attributable to electrostatic field induced current modulation and a resonant response induced by mechanical motion and attributable to the conductance and piezoresistive changes caused by this motion [4], [38].

III. MEASUREMENT SETUP

To recover the near-resonant response of the dual-gate SOI devices, the measurement setup shown in Fig. 2(c) is employed. This system utilizes a high-vacuum chamber (ambient pressure $<10^{-3}$ torr) and an electrostatic measurement technique similar to that previously described in [4]. For this particular research, the measurement setup is used to enhance the conductance of the Si nanoresonators and ultimately enable planar, nonplanar, and combination (e.g., whirling) motions [35]–[37].
The dual-gate nanoresonator structure detailed herein represents a highly tunable device platform as it facilitates planar, nonplanar, and combined (e.g., whirling) near-resonant motions, which can be tuned bidirectionally.

Fig. 4 depicts a representative near-resonant response of the nanoresonator at different side-gate biases when the back-gate bias is fixed, as acquired by incrementing the side-gate bias. The upper panels specifically highlight the magnitude of the detected mixing current, as a function of both the excitation frequency $\omega$ and the side-gate bias voltage $V_{\text{side}}$ for three distinct back-gate biases $V_{\text{back}}$. Note that a 15-mV$_{\text{rms}}$ source–drain voltage was selected for actuation purposes here, as it is just strong enough to drive the near-resonant response above the noise floor (as set by thermomechanical effects and the employed measurement
phenomena are observed when the bias voltage is changed. As previously noted, the amplitude of the measured currents increases with increasing side-gate bias—a phenomenon consistent with the previously defined stiffening mechanism. In contrast, the peak frequency associated with out-of-plane motion decreases with increasing side-gate bias.

Fig. 4. Resonant response of a representative dual-gate nanoresonator at different side-gate bias voltages with a fixed bias on the back gate. The amplitude of the ac source–drain voltage excitation is 15 mVrms. The side-gate bias is changed from −6 V to 6 V in 0.1 V steps. The upper panels highlight the magnitude of the detected mixing current (in pA) as a function of both the excitation frequency \( \omega \) and the side-gate bias voltage \( V_{\text{side}} \) for back-gate bias voltages \( V_{\text{back}} \) of 0, 3, and −3 V, respectively. The lower panels highlight the corresponding phase for \( V_{\text{back}} = 0, 3, -3 \) V.

Fig. 5. Resonant response of a representative dual-gate nanoresonator at different back-gate bias voltages with a fixed bias on the side gate. The amplitude of the ac source–drain voltage excitation is 15 mVrms. The back-gate bias is changed from −6 V to 6 V in 0.1 V steps. The upper panels highlight the magnitude of the detected mixing current (in pA) as a function of both the excitation frequency \( \omega \) and the back-gate bias voltage \( V_{\text{back}} \). The lower panels highlight the corresponding phase for \( V_{\text{side}} = 0, 3, -3 \) V.

Fig. 6. (Top row) Near-resonant, planar response and (bottom row) nonplanar response of a representative silicon nanoresonator obtained by exciting the system with various ac source–drain voltages \( V_{\text{ds}} \), while sweeping the excitation frequency \( \omega \) up and down. The left column highlights the corresponding mixing current versus frequency trajectories at different source–drain excitation amplitudes by sweeping the excitation frequency up and down, respectively. The solid lines correspond to frequency sweeping up and the dashed lines correspond to frequency sweeping down. The center column highlights the corresponding phase change versus frequency trajectories at different source–drain excitation amplitudes. The right column shows the extracted peak amplitude as a function of the source–drain voltage amplitude (subtracting the background amplitude) as obtained by sweeping the frequency. One can see all of the response characteristics noted in planar response remain qualitatively unchanged with the nonplanar bias configuration.

However, one noticeable difference exists—capacitive softening mechanisms appear to dominate in all tuning scenarios.

Given the hysteretic nature of the nonlinear response of nanoresonators, a series of frequency sweeps were also initiated to characterize the devices’ bifurcation structure and demonstrate how the structures can be tuned by varying the voltage biases applied to the back and side gates. This capability is essential for the development of small-scale resonators which actively exploit nonlinear effects in applications such as resonant mass sensing and signal processing, as previously demonstrated at the microscale [40], [50]–[52].

Fig. 6 (top row) Near-resonant, planar response and (bottom row) nonplanar response of a representative dual-gate nanoresonator by fixing the side-gate bias and incrementing the back-gate bias. In general, the results recovered through this experimental analysis, mirror those described in Fig. 4, which were recovered by incrementing the side-gate bias.
resonator as recovered by incrementing the applied source–drain voltage $V_{\text{ds}}$ and sweeping the excitation frequency up and down. Note that the gate biases are fixed such that $V_{\text{back}} = 0$ V and $V_{\text{side}} = 5$ V to ensure that the back-gate bias does not affect the in-plane motion. As evident, the system exhibits a Duffing-like [53] response characteristic, bistability over a finite frequency bandwidth, and hysteresis with respect to the direction of the frequency sweep. The left and center panels highlight the detected mixing current and corresponding phase change as $V_{\text{ds}}$ is increased. Note that $V_{\text{ds}} = 2.5$ mV approximates the thermomechanical/thermoelectric noise floor of the measured system. Under such a low source–drain voltage, the peak resonance response [proportional to $V_{\text{ds}}^2$ as seen from (1)] and the background electrostatic field current modulation (proportional to $V_{\text{ds}}^2$) become comparable to the noise floor of the system. Contributing noise sources to the noise floor in the system, as discussed in [54], include Johnson noise from the resonator and the lock-in amplifier, $1/f$ noise, thermomechanical noise, adsorption–desorption noise, and defect motion noise. This figure reveals that with increasing $V_{\text{ds}}$, the bandwidth and center frequency of the hysteretic region increase in a consistent manner—a mechanism that can be advantageously leveraged in practical applications. The right panel depicts the extracted peak amplitude as a function of the source–drain voltage amplitude (subtracting the background amplitude) as obtained by sweeping the frequency.

Similar nonlinear behavior to that detailed in Fig. 6 (top row) is observed for the nonplanar vibrations as well. In this experimental analysis, the gate biases are fixed such that $V_{\text{back}} = 5$ V and $V_{\text{side}} = 0$ V, and the amplitude of the ac source–drain voltage is incremented. Fig. 6 (bottom row) shows the nonplanar response when $V_{\text{ds}}$ is increased. Generally speaking, all of the response characteristics noted in Fig. 6 (top row) remain qualitatively unchanged with this bias configuration.

To further characterize the nonlinear frequency response structure, the device’s back-gate bias is fixed at zero and the side-gate bias was incremented from $-5$ V to 5 V, with the upper and lower bifurcation (jump) frequencies being recorded at each step. Fig. 7 shows the results of this experimental analysis when (left) negative and (right) positive dc biases are applied. As evident, for small ac source–drain voltages, no hysteresis is observed. However, at modest source–drain voltages, hysteresis (nonlinearity) occurs. As the side-gate bias is increased, the apex of each bifurcation wedge shifts to lower frequencies, due to a capacitive softening effect. Simultaneously, the top of each wedge shifts towards higher frequencies, indicating an increased frequency bandwidth associated with hysteresis at higher ac source–drain voltages $V_{\text{ds}}$.

amplitude is approximately $V_{\text{ds}} = 5$ mV for $V_{\text{side}} = 5$ V for the devices considered here.

Similarly, Fig. 8 highlights the bifurcation structure associated with out-of-plane device motions when the side-gate bias is fixed at zero and the back-gate bias is incremented from $-5$ V to 5 V. Again, the qualitative characteristics observed for planar motions appear to remain in the case of nonplanar motion.

VI. CONCLUSION

To the best of the authors’ knowledge, this study represents the first demonstration of dual-gate, nonlinear nanoelectromechanical resonators based upon an SOI process flow. As the proposed devices can be seamlessly, reproducibly, and reliably fabricated and integrated with commercial CMOS technologies, this advancement will enable the design and development of future nanosystems, specifically those targeting sensing and signal processing applications.
A key characteristic of the nanoresonators detailed herein is their inherently nonlinear and tunable nature. The systems typically exhibit a Duffing-like frequency response characteristic when excited above the noise floor, and thus exhibit hysteresis with respect to the excitation frequency over a finite bandwidth. This behavior should not be seen as detrimental however, as it is highly tunable. Accordingly, it should enable the development of highly sensitive bifurcation-based mass sensors, narrow-band amplifiers, and highly selective tunable receivers [52].

ACKNOWLEDGMENT
The authors would like to thank Pros. A. Raman and Y. Chen for their collaboration and useful discussions.

REFERENCES


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