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Control of Current Saturation and Threshold Voltage Shift in Indium Oxide Nanowire Transistors with Femtosecond Laser Annealing

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Flexible and/or transparent electronics have attracted significant interest due to their potential applications including see-through, lightweight, and conformable products.1–5 In particular, nanowire transistors (NWTs) may be better suited for future display products requiring transparent electronic switches because NWTs offer higher carrier mobility than those of thin-film transistors (TFTs), as well as the low-temperature processes that are compatible with optical transparency requirements.2–6 High-performance NWTs typically use ZnO, SnO2, and In2O3 semiconducting oxide nanowires, or aligned/random networked single-walled carbon nanotubes.1,2,4,7 Many reports have suggested that NWTs have higher performance and more stable transistor characteristics compared with amorphous silicon and polysilicon TFTs, especially on field effect mobility (μeff) and subthreshold slope (SS).8–11 Despite these excellent properties (high performance, high sensitivity, and high efficiency), however, there are still many issues to be resolved before NWTs can find practical digital and analogue applications. One issue is to place nanowires at the desired places of the wafer/board to form designed patterns. To manufacture integrated nanowire-circuits, it would be crucial to develop the technology to control the amount and shape of the nanowire in the course of its arrangement as well as to enhance the characteristics of nanowire elements. Another issue is to achieve highly saturated transistor current and robust semiconductor characteristics, such as uniform and controllable threshold voltages (Vth) and SS. Even though many unpassivated NWTs have been demonstrated, source-drain currents are not saturated but rather increase slightly linearly in most reports.3–4,7–12 Little research, to our knowledge, has been conducted to reduce such linear increase even though it is perhaps the biggest obstacle for the incorporation of NWTs in such transparent circuitry on low-temperature substrates, as current saturation is the key benefit of transistors. While high-temperature annealing or doping could be used to mitigate this problem in commercial thin-film transistors, elevated temperatures can change the properties of semiconducting nanowires, and there are difficulties in adjusting the doping level uniformly. Furthermore, these methods are in most cases incompatible with flexible device panels.

ABSTRACT Transistors based on various types of nonsilicon nanowires have shown great potential for a variety of applications, especially for those that require transparency and low-temperature substrates. However, critical requirements for circuit functionality, such as saturated source-drain current and matched threshold voltages of individual nanowire transistors in a way that is compatible with low temperature substrates, have not been achieved. Here we show that femtosecond laser pulses can anneal individual transistors based on In2O3 nanowires, improve the saturation of the source-drain current, and permanently shift the threshold voltage to the positive direction. We applied this technique and successfully shifted the switching threshold voltages of NMOS-based inverters and improved their noise margin, in both depletion and enhancement modes. Our demonstration provides a method to trim the parameters of individual nanowire transistors, and suggests potential for large-scale integration of nanowire-based circuit blocks and systems.

KEYWORDS: threshold voltage shift • In2O3 • nanowires • femtosecond laser • annealing • transistors
Several micrometers, does not annealing, which is performed on a length scale of even on plastic panels because instantaneous laser Furthermore, this annealing process could be possible avoiding damaging or sputtering them away (Figure 1a).

The gate electrode made from 110 nm thick patterned abusting of transparent glass substrate (corning glass), transparent NWT with the bottom gate structure, consisting of transparent glass substrate (corning glass), a buffer layer of 100 nm thick silicon dioxide, a gate electrode made from 110 nm thick patterned indium—tin oxide (ITO), a 20 nm thick Al2O3 gate insulator through atomic layer deposition (ALD), a single-crystal semiconducting In2O3 nanowire as the active channel, and 110 nm thick ITO for source/drain (S/D) electrodes. In2O3 nanowires were synthesized through a laser ablation method (band gap 6 g ≈ 3.6 eV, and diameter D ≈ 20 nm). They are transparent to visible light, and are suitable for transparent and flexible TFTs. Meanwhile, ITO is a promising candidate as transparent conductors for gate, source, and drain electrodes in TFTs. High-κ Al2O3 gate dielectric showed excellent insulating properties, with an electrical breakdown field of >8 MV/cm and a dielectric constant of ~9. Figure 1b shows the field emission scanning electron microscope (FE-SEM) image of several NWT devices including all transparent components. The lengths of single In2O3 nanowire (~20 nm diameter) addressed between S/D electrodes were ~3 μm to avoid the complications of the short channel effects. Figure 1a also illustrates the femtosecond laser annealing process. The unique aspect of our annealing process was that laser pulses were only focused on and scanned along the S/D contact regions using its particular property of localized energy input (beam spot diameter ~1.22 μm). The pulse wavelengths were centered at 800 nm, which has energy below the band gap of In2O3. Therefore we expected the effect to be likely different from the annealing using excimer lasers, which has a photon energy above the band gap of the nanowire.

The most prominent effects of laser annealing were the improvement of the current saturation and the positive shift of the threshold voltage Vth, Figure 2a shows the drain current versus drain-to-source voltage (I ds –V ds) characteristics for a representative NWT with V th ranges from −1.5 to 4 V in 0.5 V steps before (black open square) and after (red open circle) laser annealing at 0.43 J/cm²/pulse. The I th =V ds curves of as-fabricated devices deviated significantly from the expected response of a long-channel transistor even when V ds values were in the saturation region (V th > V th − V ds), and exhibited significant drain conductance or low output resistance (r d). The annealed devices, on the other hand, appeared to have induced V th shifts to the positive direction, which resulted in smaller saturation current at the same gate voltage. However, the drain currents showed significantly higher output resistance. We first identify the threshold voltages before and after the femtosecond laser annealing. The linear-scale drain current versus gate-source voltage (I th –V th) of the fully transparent single In2O3 NWT at V th = 0.1, 0.5, and V th = 4.0 V before (square) and after (circle) laser annealing is shown in Figure 2b. The V th can be extrapolated from the slope of the drain current increase and the values were around −2.9 V at V th = 0.1 V and around −2.7 V at V th = 0.5 V for as-fabricated devices. However, the V th values shifted along positive direction.

Figure 1. Schematic and scanning-electron micrograph of an In2O3-based NWT. (a) The cross-sectional schematic of a fully transparent, bottom gated nanowire transistor. The femtosecond laser pulses focus on the ITO source and drain area and scans along the edge of the source and drain pads. Laser pulses do not scan across the channel of the transistor, or the exposed portion of the nanowire. (b) Top-view scanning-electron micrograph of a fully transparent NWT. ITO was used for gate, source, and drain. The inset shows a single In2O3 nanowire (D/L = 20 nm/3 μm) addressed between source and drain.
to $V_{th} \approx 0.2$ and 0.5 V, respectively, after the laser annealing. Data from other $V_{ds}$ values showed similar results and we estimate the threshold voltage to be around $-2.8$ V for as-fabricated NWT and around 0.4 V for annealed NWT. The apparent reduction in source-drain current after the laser annealing can thus be explained by the positive shift of the threshold voltage.

To compare the output resistance, we plotted the $I_{ds}$-$V_{ds}$ characteristics at $V_{gs} = -2.5$ V for the as-fabricated device, and at $V_{gs} = 1$ V for the annealed device (Figure 2c). The saturation currents were similar, as the $V_{gs} - V_{th}$ were similar (0.3 V for as-fabricated and 0.6 V for annealed NWT). For $V_{gs} > 1.5$ V, which is appreciably higher than $V_{gs} - V_{th}$, the device should be in saturation state. However, the as-fabricated device clearly showed a weak saturation, or small output resistance, while the annealed device showed strong saturation. We applied linear regression to calculate the output resistance of the transistor using $I_{ds}$-$V_{ds}$ data in the range of $1.5 \text{ V} < V_{ds} < 5 \text{ V}$. The output resistance for the as-fabricated transistor was 37 MΩ, while for the annealed sample it was 200 MΩ, showing a 5.4-fold increase. Similar increase of output resistance (3–7-fold) was observed at other saturation current values. Strong saturation is very important for almost all circuit applications requiring transistors and we believe our method is the first to achieve such a goal with extremely low thermal budget, and without surface modification. Temporary $V_{th}$ shifts have been reported for In$_2$O$_3$ NWTs after UV light exposure. However, such exposure shifts the threshold to the negative direction and the device returns to its previous operation state shortly. The effect of femtosecond laser annealing appears to be permanent, and is stable in air. When we remeasured nanowire transistors after a few days and after several weeks, we observed negligible variations.

This permanent change of $V_{th}$ suggests that the postmetallization S/D annealing with a femtosecond laser could also be a tuning method to adjust the $V_{th}$ values of individual nanowires. To illustrate this potential, two different values of annealing power were sequentially applied to the same nanowire transistor and we observed a positive $V_{th}$ shift after each annealing. We first measured the $I_{ds}$-$V_{gs}$ at $V_{ds} = 0.5$ V of another representative NWT before laser annealing, and found the $V_{th}$ to be $-1$ V, and then applied femtosecond laser annealing at 0.14 J/cm$^2$/pulse. A $V_{th}$ shift to the positive direction by 0.5 V was observed. We then performed a second annealing on the same device, with the energy of 0.43 J/cm$^2$/pulse. A further shift toward the positive direction by 2.25 V was shown in Figure 2d. The additional power (in our case 0.43 J/cm$^2$/pulse) was essential because when we tried to apply the same annealing power, a negligible $V_{th}$ shift was observed. Figure 2d shows the log-scale $I_{ds}$-$V_{gs}$ characteristics of
an In2O3 NWT at $V_{ds} = 0.5$ V for different annealing conditions: before applying femtosecond laser (black open square, $V_{th} = -1$ V, $I_{on}/I_{off} \approx 1.19 \times 10^{3}$, $SS = 2.2$ V/dec, and $\mu_{eff} = 1.12 \times 10^{2}$ cm$^{2}$/V·s); after femtosecond laser annealing at pulse energy of 0.14 J/cm$^2$ (red open circle, $V_{th} = -0.5$ V, $I_{on}/I_{off} \approx 1.76 \times 10^{4}$, $SS = 2.2$ V/dec, and $\mu_{eff} = 1.47 \times 10^{2}$ cm$^{2}$/V·s); and after an additional femtosecond laser annealing at 0.43 J/cm$^2$ pulse (blue open diamond, $V_{th} = 1.75$ V, $I_{on}/I_{off} \approx 2.23 \times 10^{6}$, $SS = 2.2$ V/dec, $\mu_{eff} = 1.77 \times 10^{2}$ cm$^{2}$/V·s), respectively. After each femtosecond laser annealing, the $I_{on}/I_{off}$ and $\mu_{eff}$ both improved slightly. In all calculations, the field-effect mobility [$\mu = \frac{dI_{ds}}{dV_{gs}} \times \frac{L^{2}}{C_{g} \times V_{ds}}$] was calculated by using the cylinder-on-plate (COP) capacitance model [$C_{g} = \frac{2\pi \epsilon_{0} \epsilon_{r} L}{\ln(1 + t_{off}/t)}$]. Therefore, femtosecond laser annealing apparently has not only improved current saturation (by increasing output resistance by 3–7-fold) but also adjusted threshold voltages of individual In2O3 nanowire transistors. Such effects might provide a solution to one of the long-standing problems in large scale integration of devices made from NWTs: individual trimming of NWT characteristics to match the requirements of functional devices, such as inverters, current mirrors, and amplifiers.

As an application for our capability of adjusting the $V_{th}$ values of individual NWTs, we fabricated a fully transparent inverter with both transistors made from In2O3 nanowires. An inverter is one of the fundamental building blocks of logic circuits, and its switching threshold (or trip) voltage is preferred to be located at the middle of the supply voltage, which requires the proper positioning of the $V_{th}$ values of both transistors. Moreover, high and early saturation of the transistors are also desirable to improve the noise margin by maintaining the gain in the transition region. Femtosecond laser annealing introduced here appears to be an ideal method to improve the inverter characteristics. Figure 3a shows the two types of inverters we have fabricated, one with depletion mode load (left) and the other with enhanced mode load (right). The two types of inverters are the possible candidates when there is a fixed at 0, see Figure 3a. When the input is low ("0") and transistor $M_{2}$ is off, $M_{1}$ keeps driving the output high until $V_{ds}$ of $M_{1}$ drops to zero, which means that $V_{OUT}$ is the same as the supply voltage. When the input state changes to high ("1"), $M_{2}$ starts to discharge output quickly. This can be explained by the relative magnitudes of $V_{gs} - V_{th}$ for $M_{2}$ and for $M_{1}, V_{gs} - V_{th} \approx 0 = V_{th}$, since $V_{gs1}$ for $M_{1}$ is always 0. When $V_{gs2} - V_{th} = V_{IN} - V_{IN2}$ for $M_{2}$ is larger than $-V_{th1}$ of $M_{1}$, the current is limited by $M_{2}$; and $V_{ds2}$ of $M_{2}$ quickly reduces to near zero to match the small current set by $M_{1}$. This ensures a fast switching from high to low. Therefore the trip voltage is mostly determined by the $V_{th}$ of $M_{2}$ and $r_{o}$ of $M_{1}$ and $M_{2}$ and could be smaller (1.5 V) than half of the supply voltage, 2 V, as shown in Figure 3d. To achieve enhanced noise margin, the trip voltage is preferred to be shifted to close to 2 V. $NM_{H}$ was around 1.8 V, $NM_{L}$ was 0.8 V, and trip voltage was 1.5 V before femtosecond laser annealing, which was smaller than half of the supply voltage and therefore reduced the low voltage input noise immunity. However, through femtosecond laser annealing, trip voltage was changed to 2.2 V, $NM_{H}$ to around 1 V, and $NM_{L}$ to around 1.5 V, which achieved a better balance between $NM_{H}$ and $NM_{L}$. Moreover, the function of $M_{1}$ should remain complementary to that of $M_{2}$, so the threshold voltage of $M_{1}$ had to be maintained negative while that of $M_{2}$ is shifted along the positive direction. This requires local tuning of the pull-down transistor ($M_{2}$) without significantly affecting the pull-up transistor ($M_{1}$). Our femtosecond laser annealing meets those requirements and can be applied selectively to the pull-down transistor to shift the switching voltage of inverter to be in the middle of the supply rail. The voltage transfer characteristics in Figure 3d show that enhanced noise margin was achieved by shifting the trip point of inverter from 1.5 to 2.2 V. Moreover, the hysteresis of the inverter device was modest over the bias region before and after administering the annealing. Thus, it might be possible to use this technique to control the switching threshold voltage of an inverter, which is important to achieve a high noise margin for many circuit applications.
The operating principle of enhancement mode load transistor is different compared to depletion mode load inverter. Figure 3e shows that output voltage was not completely zero even when the input was driven high. Also, the transition from high to low was not as sharp as that of the depletion mode. These were primarily due to the static current through $M_3$ and $M_4$ when $M_4$ was turned on. Unlike the depletion mode, the $V_{gs3} - V_{th3}$ increases when $V_{OUT}$ drops, which increases the static current. At this time, the output voltage was determined by the on resistance ($R_{on}$) values of $M_3$ and $M_4$ as Ohm’s law is applicable. Thus, the ratio of pull-up and pull-down transistor was important in this case. In practice, this ratio can be achieved by adjusting the channel length. In addition, high $R_{on}$ of $M_3$ was required to obtain a sharper transfer from high to low state. The starting of transition from high to low is at a small negative voltage, as $V_{th}$ of $M_3$ exists in the slightly negative area. Therefore, the value of $NM_L$ was around 0.3 V before administering femtosecond laser annealing, which is a compromised operation. The femtosecond laser annealing produced a selective positive shift of $V_{th}$ for $M_4$. As a result, the value of $NM_L$ increased to around 1.2 V.

Meanwhile, $NM_H$ decreased from around 0.9 to 0.3 V, due to the positive threshold voltage shift. However, the total noise margin, $NM_L + NM_H$, increased from 1.2 to 1.5 V. Therefore, femtosecond laser annealing improved noise immunity by increasing the total noise margin, $NM_L + NM_H$. Figure 3e shows the effect of femtosecond laser annealing on an enhancement mode inverter: the trip voltage was shifted to the positive direction toward half of the supply voltage, and the total noise margin was improved. The hysteresis of this inverter was more prominent than that of the depletion mode, and we are investigating the causes and ways to mitigate them.

Finally, our inverter is highly transparent. Figure 4 shows the optical transmission spectra through the fully transparent NMOS inverters using In$_2$O$_3$ nanowires on a glass substrate in the 350–1250 nm wavelength range. The optical transmission value was around 82%. Note that the optical transmission value of corning glass substrate is around 92%. The NWT array regions were 1.0 $\times$ 0.5 in. (the glass substrate was 1.5 $\times$ 1.0 in.) and contained around 1500 NWT device patterns; and the entire substrate was coated with the Al$_2$O$_3$ gate insulator. The source/drain regions and the gate
laser annealing is expected to be mainly thermal, possibly forming an improved single-crystalline In$_2$O$_3$ nanowire structure. The short pulse duration may result in ITO photophysical bond breaking instead of classical melting,\(^2\) consequently forming ITO spikes into the nanowire channel to improve the contact-channel interface, modifying the Schottky barrier height and the effective doping in the nearby semiconductor region. Further investigation of the mechanism behind such annealing effects is interesting and ongoing. This study provides insights into the contact-dominated transistor properties, in terms of the effects on output resistance and $V_{th}$.

Combined with the excimer laser annealing,\(^1\) which shifts the threshold voltage to the negative direction by increasing the number of oxygen vacancies, one could envision full trimming capability of the threshold voltages of NWTs and maintaining high current saturation, thus opening the possibility of constructing sophisticated circuit blocks or other functional devices made from NWTs, and significantly advance our knowledge on flexible, and transparent electronics on low-temperature substrates. Controlling the threshold voltages of nanowires is of central importance to any practical integrated circuits. The semiconductor industry enjoys highly uniform doping and high-precision manufacturing (i.e., critical dimension control) to achieve uniform threshold voltages. While manufacturing of non-Si nanowire based transistors will certainly improve with novel techniques, it is unlikely that they will match the level of control in CMOS technologies, therefore the femtosecond laser tuning of individual NWT presented here would be very important in manufacturing NWTs if large circuit blocks are to function as designed. We note that there could be other ways to alter the transistor characteristics, such as surface passivation and chemical modifications. Femtosecond laser annealing appears to be noninvasive, and still preserves the essentialism behind such annealing effects is interesting and ongoing. This study provides insights into the contact-dominated transistor properties, in terms of the effects on output resistance and $V_{th}$.

Femtosecond Laser Anneal and I–V Measurement. The laser annealing source was a Ti:Sapphire laser operating at 800 nm. The laser pulse duration was 50 fs and the repetition rate was 1 kHz. Laser transmitted power varied from 1.67 $\mu$W (average energy fluence rate of 0.14 J/cm$^2$/pulse) to 5 $\mu$W (average energy fluence rate of 0.43 J/cm$^2$/pulse). The transmission spectra of normal incident linearly polarized light were collected with a Lambda 950 spectrophotometer (Perkin-Elmer). Electrical characterizations was performed with a semiconductor parameter analyzer (HP 4156A).

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