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Bipolar Integrated Circuits in 4H-SiC

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Abstract—Due to its wide band gap, 4H-SiC is potentially capable of sustained operation at temperatures well above 600 °C, but current devices are limited to lower temperatures by the stability of the metallization and passivation layers. SiC bipolar transistors are capable of operation at temperatures above 300 °C, as they do not have an oxide layer under high electric field and hence do not suffer from oxide reliability issues. In this paper, we describe bipolar digital integrated circuits on semi-insulating 4H-SiC that operate over a wide range of supply voltage and temperature, demonstrating the potential of SiC for high-temperature small-scale integrated-circuit applications.

Index Terms—High-temperature integrated circuits (ICs), silicon carbide (SiC), SiC ICs, smart power, transistor–transistor logic (TTL).

I. INTRODUCTION

SILICON CARBIDE (SiC) is a wide-band-gap semiconductor that offers significant performance advantages in applications requiring high voltages and/or high temperatures. 4H-SiC has a band gap of 3.25 eV, which is three times larger than that of silicon. The wider band gap gives SiC an avalanche breakdown field that is about five times larger than that of silicon, making it ideal for power-switching devices [1]–[3]. The wider band gap also results in an intrinsic temperature well above 600 °C, allowing high-temperature operation [4], [5]. The thermal conductivity of SiC is twice as high as silicon, enabling SiC devices to dissipate more internally generated heat [2]. SiC has an electron saturation velocity that is about twice as high as that of silicon [6], [7], whereas the electron mobility in 4H-SiC is about 60% that of silicon.

Generally, SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) cannot be reliably operated at temperatures above about 200 °C, due to issues with oxide reliability [8], although some recent work have extended the operational temperature of SiC MOSFETs and logic circuits using such MOSFETs to beyond 200 °C [9]–[11]. Since bipolar transistors (bipolar junction transistors, BJTs) do not utilize a gate oxide that is stressed by high electric fields, they are not subject to the same temperature restrictions as MOSFETs. This makes BJTs more suitable for high-temperature applications. In spite of all the aforementioned advantages, SiC BJTs suffer from degradation in electrical performance over time at both room and high temperatures [12]. This is caused by the development of stacking faults in the low-doped collector regions [12], [13] and/or the increase in the surface recombination in the base–emitter region [14]. However, recent work has demonstrated progress in the long-term operational stability of SiC BJT [15].

The first bipolar digital integrated circuits (ICs) in 4H-SiC were simple transistor–transistor logic (TTL) gates operating on a 15-V supply voltage, with propagation delays of more than 100 ns at room temperature [16]. In this paper, we report an improved and optimized design with propagation delays of only 9.8 ns at room temperature. All circuits operate over a wide range of supply voltage and at temperatures ranging from room temperature to over 300 °C.

II. SIMULATION AND DESIGN

Fig. 1 shows the structure and dimensions of the BJTs (without the metal interconnect levels) used for simulation purposes. Dimensions and the doping of the fabricated device slightly differ from the simulated structure.

Fig. 1. Structure, dimensions, and doping of the BJT used for simulation purposes. Dimensions and the doping of the fabricated device slightly differ from the simulated structure.

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Fig. 2. SPICE fitting of $I_C$–$V_{CE}$ for a 100-$\mu$m BJT for $I_B = 1$ mA.

Fig. 3. SPICE fitting of (a) $I_C$–$V_{BE}$ and (b) $I_B$–$V_{BE}$ for a 100-$\mu$m BJT.

Circuit designs are optimized using SPICE [19]. To simulate circuits in SPICE, an appropriate model for the BJT is needed. SPICE model parameters are initially generated by treating MEDICI simulations as “experimental data” and fitting the SPICE model to the MEDICI “data.” Comparisons of SPICE and MEDICI models are shown in Figs. 2 and 3. In Fig. 3, the agreement is poor at low $I_C$ and $I_B$ values. This is, in part, due to the inability of SPICE to accurately model recombination current. For circuit design, this is not critical since, for low $I_B$ values, the BJT is essentially cut off. The complete set of fitted curves and final model parameters are given in [20].

Many different bipolar IC families have been developed in silicon. In this paper, we consider two particular families: 1) TTL and 2) Schottky TTL (STTL). For STTL, two different circuit configurations are examined. The first configuration is the conventional Schottky TTL circuit, whereas the second configuration, which is called “STTL as TTL” is essentially the standard TTL circuit with Schottky diodes across each transistor. The performance of each design is evaluated using a basic inverter gate with the following goals: 1) it must exhibit adequate noise margins when loaded by a fan-out of ten similar gates and 2) a chain of such gates must be optimized for minimum propagation delay. Optimization is complicated, because the circuit configuration that gives the best dc characteristics may not be the fastest. Hence, both dc and transient performance are simultaneously evaluated. The SPICE circuit simulator is used to optimize the inverter design in all technologies. The basic power supply voltage $V_{CC}$ is chosen as 15 V, compared with 5 V for silicon TTL, due to the higher forward diode drop in wide-band-gap semiconductors.

Fig. 4 shows the circuit diagram of the TTL inverter with resistor and transistor values optimized for a fan-out of ten (FO-10), best dc noise margins, and lowest propagation delay. The length of all transistors, except the output transistor, is set at 25 $\mu$m. The output transistor is made 125 $\mu$m long to support a fan-out of ten. When the values of the resistors are adjusted, the areas of all transistors are scaled by the same ratio to maintain the same current density. The biggest drawback of this approach is degradation in noise margins, particularly logic-low noise margin at higher fan-outs. The solution is to make the output transistor larger than other transistors. This allows us to reduce resistor values to decrease the propagation delay without degrading the dc performance of the circuit.

Fig. 5 shows the circuit configuration of an optimized STTL inverter circuit. For the “STTL as TTL” design, the values of the resistors are carried over from the TTL design. Fig. 6 shows the voltage transfer characteristic (VTC) of the optimized TTL and STTL FO-10 inverter circuits. The stable operating points are the lowest and highest intersection points of the normal and the inverted VTC curves.

Fig. 7 shows the simulated propagation delay of an FO-10 inverter for four different designs. The optimized TTL and Schottky TTL designs (with semi-insulating substrates) display comparable propagation delays. Because of the additional complexity in fabricating STTL circuits and the minimal performance improvement, it was decided to pursue the optimized TTL design. The expected propagation delay for this configuration is 2.98 ns.
III. FABRICATION

All devices and circuits are fabricated on 50-mm wafers with n+/p/n-/n+ epilayers (0.65 μm − 1.2 × 10^{19} cm^{-3}/1.1 μm − 1 × 10^{17} cm^{-3}/0.54 μm − 8 × 10^{15} cm^{-3}/1 μm − 1 × 10^{19} cm^{-3}) on semi-insulating 4H-SiC substrates.

To characterize the performance of SiC TTL designs, additional gates and more complex ICs are fabricated, including a half-adder, an 11-stage ring oscillator, a string of ten inverters in series, and a D-type flip-flop.

Starting with the epitaxial wafer, Ti/Ni (10 nm/100 nm) is deposited as a masking material, and 0.7–0.78 μm of SiC is selectively removed by reactive-ion etching (RIE) in SF$_6$ to form the emitter fingers. For the p+ base contact, Ti/Au (10 nm/600 nm) is evaporated and patterned to form an implant mask, and Al is implanted at 650 °C at a dose of 1.05 × 10^{15} cm^{-2}. Following the implant, a graphite cap is formed on the sample to prevent roughening of the surface during the implant anneal, and the dopants are activated by annealing at 1600 °C for 20 min in argon. To form the base mesa, Ti/Ni (10 nm/150 nm) is deposited and patterned as an etch mask, and Al is implanted at 650 °C at a dose of 1.05 × 10^{15} cm^{-2}.

Following the implant, a graphite cap is formed on the sample to prevent roughening of the surface during the implant anneal, and the dopants are activated by annealing at 1600 °C for 20 min in argon. To form the base mesa, Ti/Ni (10 nm/150 nm) is deposited and patterned as an etch mask, and Al is implanted at 650 °C at a dose of 1.05 × 10^{15} cm^{-2}. Following the implant, a graphite cap is formed on the sample to prevent roughening of the surface during the implant anneal, and the dopants are activated by annealing at 1600 °C for 20 min in argon. To form the base mesa, Ti/Ni (10 nm/150 nm) is deposited and patterned as an etch mask, and Al is implanted at 650 °C at a dose of 1.05 × 10^{15} cm^{-2}.

To minimize surface recombination, several hundred angstroms of metal–oxide–semiconductor-quality oxide is grown by pyrogenic oxidation at 1150 °C for 3.5 h, followed by a two-hour anneal in NO at 1175 °C [21]. Using photoresist as a masking material, contact windows are opened in the oxide using RIE and buffered hydrofluoric acid (BHF). This is followed by deposition of contact metals (70-nm Ni for n-type and 34-nm/167-nm Ti/Al for p-type), using e-beam evaporation. The contacts are then annealed at 1000 °C for 2 min in vacuum.

A first intermediate dielectric (ILD), which is 0.5 μm thick, is formed by low-temperature oxidation (LTO). Next, windows are opened in the ILD to deposit top metal. Fifteen-nanometer Ti and 250 nm of Al are sputtered to form the first layer of metal interconnect. A second ILD is then deposited by LTO. In order to connect the first layer of interconnect to the second, vias are opened using RIE and wet etching, using photoresist as an etch mask. Finally, Ti/Au (15 nm/250 nm) is sputtered to form the second-level interconnect. Fig. 8 shows scanning electron microscope (SEM) images of some of the completed devices and circuits.

IV. RESULTS AND DISCUSSION

The dc characteristics of the transistors and circuits are measured using an HP-4156 semiconductor parameter analyzer. The transient response of circuits is characterized using an Agilent-33220A waveform generator and a Tektronix-TDS5032B digital phosphor oscilloscope with a Tektronix P6245 low-capacitance (< 1 pF) field-effect-transistor probe. All measurements are obtained at wafer probe using a hot chuck with maximum temperature of 355 °C.
The sheet resistivities $\rho_s$ of the emitter, collector, and base epilayers, which was obtained using transmission-line-method measurements, are 250, 216, and 21300 $\Omega$, respectively. The resistivities $\rho_{cn}$ of the emitter, collector, and base contacts are $2.35 \times 10^{-5}$, $2.06 \times 10^{-5}$, and $1.8 \times 10^{-3}$ $\Omega \cdot cm^2$, respectively.

Fig. 9 shows the dc current–voltage characteristics of the fabricated 25- and 125-$\mu$m BJTs, and Fig. 10 displays the Gummel plots for the same transistors. A peak dc current gain of 5.6 is observed for the 25-$\mu$m BJT, and a peak gain of 4.7 is observed for the 125-$\mu$m BJT. These results are much lower than the value (~42) predicted by MEDICI simulations. The two transistors have similar current levels due to the similar current gains.

Current gain depends on a number of factors, including the doping and thickness of the base and the emitter, minority carrier lifetime in these regions, and surface recombination at the top of the base and sidewalls of the emitter. It is highly sensitive to surface recombination velocity, and the actual value may differ from the value assumed in the simulations. Surface recombination on the etched sidewalls at the emitter–base boundary plays a major role in determining the current gain, and its effects are well documented in the literature (specifically, current gain is inversely proportional to surface recombination).

The current gain may be limited by the quality of the SiC-SiO$_2$ interface. Recent studies have shown that passivation by dry oxidation in an N$_2$O ambient gives rise to high current gain in a BJT due to reduced surface recombination [22]. As calculated from the Gummel plots, the ideality factors for the base currents in our devices are $\sim 2.9$ for the 25-$\mu$m BJT and $\sim 2.2$ for the 125-$\mu$m BJT; such high ideality factors strongly suggest that the base current is dominated by recombination.

Another possible explanation for the low current gain is recombination in the implanted p$^+$ base contact regions [18]. In the simulations, the electron and hole lifetimes were assumed to be 0.26 and 0.3 $\mu$s in all regions of the device. In the fabricated BJT, the lifetimes in the p$^+$ implanted region will likely be much lower due to lattice damage caused by ion implantation. To investigate this, additional simulations were performed with dimensions, dopings, and contact resistances.
set to those measured in the fabricated BJT. It was noticed that, when the lifetime in the p+ implant region is reduced to 1.5 ns, the current gain decreases to ~6. This suggests that base contact recombination alone may account for the low gain in the fabricated devices.

The low current gain may also be exacerbated by the “emitter size effect.” This effect is caused by edge recombination that becomes dominant when the emitter area-to-periphery ratio decreases. Many studies have shown that, as the emitter width decreases, the current gain also decreases [23]–[25]. Hence, for narrow emitter widths, it becomes much more important to improve the interface between SiC and SiO$_2$. The width of the emitter in our BJTs is 7 μm, which is narrow enough for this effect to play a key role in limiting the current gain.

Fig. 11 shows the VTC at room temperature and different supply voltages for both FO-1 and FO-10 inverters. For both inverters, $V_{OH}$ almost linearly increases with $V_{CC}$, whereas $V_{OL}$ only slightly increases. The inset in Fig. 11 shows the variation in noise margins with changing power supply voltage for both the inverters. As the power supply voltage is increased, the output-high noise margin $NM_H$ almost linearly increases with $V_{CC}$, whereas the output-low noise margin $NM_L$ slightly decreases. For the FO-1 inverter, $NM_H$ increases from 3.7 to 8.3 V, and $NM_L$ decreases from 5.8 to 5.5 V, as $V_{CC}$ goes from 15 to 20 V. For the FO-10 inverter, $NM_H$ increases from 1.8 to 6 V, and $NM_L$ decreases from 3.3 to 1.3 V, as $V_{CC}$ goes from 15 V to 20 V. As apparent from the figure, both inverters exhibit adequate noise margins over the entire range of power supply voltages and are in good agreement with the simulated results.

All individual gates and demonstration ICs operate as expected. Fig. 12 illustrates the logical functionality of two such ICs, i.e., the half-adder and D flip-flop.

Device and circuit performance are evaluated at two elevated temperatures, i.e., 150 °C and 355 °C. In the case of BJT, for a fixed base current, the current gain decreases with increasing temperature. The measured peak current gain for the 25-μm transistor is 5.6 at 23 °C, 4.5 at 150 °C, and 3.8 at 355 °C. For the 125-μm transistor, the peak gain is 4.7 at 23 °C, 3.8 at 150 °C, and 2.8 at 355 °C. The decrease in gain is expected since SiC n-p-n BJTs have a negative temperature coefficient of current gain, which is caused by an increase in the ionization of aluminum acceptors in the base and reduced emitter injection efficiency [26], [27].

Fig. 13 displays the variation in noise margins for both inverters as a function of power supply voltage and temperature. For a given $V_{CC}$, both the output-high voltage and output-low voltage increase with temperature. The increase in output-high voltage leads to an increase in $NM_H$, whereas the increase in output-low voltage leads to a decrease in $NM_L$. Fig. 14 demonstrates that the inverters still exhibit adequate noise margins, even at high temperatures, with the lowest noise margin being the $NM_L$ of the F-10 inverter at 355 °C.

Propagation delay is measured using the 11-stage ring oscillator circuit. The ring oscillator consists of an odd number of inverters (11 in this case) in a circular chain, where the output of the last inverter is fed back in to the first inverter. Fig. 14 shows the output characteristic of the ring oscillator at $V_{CC} = 20$ V at three temperatures. At room temperature, the ring oscillator exhibits high and low logic levels of about 14 and 0.4 V, respectively (13.6-V logic swing). The rise and fall times are determined to be 26 and 23 ns, respectively. The
The delay almost linearly increases with temperature (9.8 ns at 23 °C, 10.3 ns at 150 °C, and 11.7 ns at 355 °C), and the oscillation is 19% slower at 355 °C than at room temperature. As stated earlier, current gain determines the speed of charge removal from the base, and since the current gain decreases with temperature, it is expected that the delay will increase.

In spite of the low current gain, these delays are comparable to those of silicon TTL circuits (~10 ns) and are an order of magnitude lower than our first 4H-SiC bipolar ICs [16]. The ring oscillator waveforms remain robust at high temperatures, demonstrating the potential of SiC bipolar ICs for small-scale high-temperature application.

V. CONCLUSION

In this paper, we have described the design and fabrication of second-generation 4H-SiC bipolar ICs and characterized their operation as a function of temperature and power supply voltage. All devices and circuits are functional over a range of supply voltages and temperature, in spite of low current gains. We attribute the low current gain to a high surface recombination and short minority carrier lifetime in the implanted p+ base contact regions, in combination with narrow emitter fingers (emitter size effect). Propagation delays are an order of magnitude lower than the best previous results and compare well with those of silicon TTL. Further investigations are required to establish the long-term stability and reliability of this technology.

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