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Analysis of Electron Mobility in Inversion-Mode Al$_2$O$_3$/In$_x$Ga$_{1-x}$As MOSFETs

Weike Wang, Student Member, IEEE, James C. M. Hwang, Fellow, IEEE, Yi Xuan, Member, IEEE, and Peide D. Ye, Senior Member, IEEE

Abstract—The electron mobility in Al$_2$O$_3$/In$_x$Ga$_{1-x}$As (x = 0.53, 0.65, or 0.75) metal–oxide–semiconductor field-effect transistors was analyzed for scattering by oxide charge, as well as interface charge and roughness, and compared with measured transfer characteristics from depletion to inversion. The analysis showed that, under strong inversion, the electron mobility was mainly limited by interface roughness. The extracted interface roughness from the measured data was two to seven times that of the interface between a high-k dielectric and Si, assuming the correlation lengths were comparable. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.

Index Terms—Charge-carrier mobility, gallium compounds, indium compounds, metal–oxide–semiconductor field-effect transistors (MOSFETs), semiconductor device modeling.

I. INTRODUCTION

THE SUCCESS OF complementary metal–oxide–semiconductor technology is largely based on relentless shrinking of metal–oxide–semiconductor field-effect transistors (MOSFETs) according to Moore’s law. As the shrinkage approaches the physical limit of silicon, alternative channel materials such as high-mobility III–V semiconductors have received increasing attention. However, high bulk mobility does not necessarily lead to high surface mobility in an inversion-mode MOSFET. With the recent mapping of interface traps across the bandgap of InGaAs [1] and demonstration of high-performance InGaAs MOSFETs [2]–[15], their current–voltage characteristics can now be analyzed to determine the difference between surface and bulk mobility. This should complement studies that were based on the capacitance–voltage characteristics of metal–oxide–semiconductor diodes and compared with measured transfer characteristics from depletion to inversion. The analysis of inversion charge and roughness, and compared with measured transfer characteristics from depletion to inversion. The analysis showed that, under strong inversion, the electron mobility was mainly limited by interface roughness. The extracted interface roughness from the measured data was two to seven times that of the interface between a high-k dielectric and Si, assuming the correlation lengths were comparable. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.

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II. DEVICE STRUCTURE AND CHARACTERIZATION

Fig. 1 illustrates the structure of In$_x$Ga$_{1-x}$As MOSFETs used in this paper. A 500-nm layer of In$_{0.53}$Ga$_{0.47}$As p-doped to $4 \times 10^{17}$ cm$^{-3}$, a 300-nm layer of In$_{0.53}$Ga$_{0.47}$As p-doped to $1 \times 10^{17}$ cm$^{-3}$, and a 15- to 20-nm layer of In$_x$Ga$_{1-x}$As (x = 0.53, 0.65, or 0.75) p-doped to $1 \times 10^{17}$ cm$^{-3}$ were sequentially grown on p$^+$-doped InP substrates by molecular beam epitaxy. The In$_{0.53}$Ga$_{0.47}$As layer is lattice matched to InP, whereas the In$_{0.75}$Ga$_{0.25}$As layer is at the limit of pseudomorphic growth. An 8- to 10-nm layer of Al$_2$O$_3$ with a dielectric constant $k_{OX}$ of 9 was then formed on top of In$_x$Ga$_{1-x}$As by atomic layer deposition as the gate oxide. The gate was metalized with evaporated Ni and Au. Except for the extraction of source–drain parasitic resistance, current–voltage transfer characteristics were measured under a drain–source voltage $V_{DS}$ of 50 mV on MOSFETs with a gate length L of 4 µm and a gate width W of 100 µm. The low drain–source voltage ensured linear characteristics; the long gate length minimized short-channel effects. Several MOSFETs of the same In mole fraction were measured, and the typical characteristics are shown in Fig. 2. It can be seen that, with increasing In mole fraction, the ON-state current and transconductance improve, but the OFF-state leakage degrades. Detailed fabrication process and device performance can be found in [9]. All measurements were performed on-wafer by using an Agilent 4156C precision semiconductor parameter analyzer and a Cascade Summit 12000 probe station with a microchamber ambient enclosure and ±0.1 °C temperature control.

III. ANALYSIS OF INVERSION CHARGE

Despite the high performance of the present InGaAs MOSFETs, their interface trap density is rather high (as will be shown later), and their inversion charge density cannot be
accurately measured. Therefore, instead of extracting from the measured current–voltage characteristics the electron mobility as a function of the inversion charge density, we derive the mobility versus charge density characteristics and reduce them to a few simple parameters to be extracted from the measured current–voltage characteristics, as detailed in this section.

The electrostatic characteristics of the 2-D electron gas in a MOSFET inversion layer can be described by the following coupled Schrödinger and Poisson equations:

\[ \frac{d^2 \psi_I(z)}{dz^2} + \frac{2m^*}{\hbar^2} [E_I + q\varphi(z)] \psi_I(z) = 0 \]  
\[ \frac{d^2 \varphi(z)}{dz^2} = -\frac{q}{\varepsilon_S} [N_A + n(z) - p(z)] \]

where \( \psi_I(z) \) is the normalized wave function of an electron in the \( I \)th subband, \( m^* \) is the effective mass for the electron motion in the \( z \)-direction perpendicular to the oxide–semiconductor interface, \( \hbar \) is the reduced Planck’s constant, \( E_I \) is the energy level of the \( I \)th subband, \( q \) is the electron charge, \( \varphi(z) \) is the electrostatic potential, \( \varepsilon_S \) is the semiconductor permittivity, \( N_A \) is the ionized acceptor concentration, and \( n(z) \) and \( p(z) \) are the electron and hole concentrations, respectively. Equations (1) and (2) can be individually but consistently solved by assuming the electric field to be constant or the potential well to be triangular near the interface [16]. For the present InGaAs MOSFETs, Fig. 3(a) shows the lowest two subbands, i.e., \( E_1 \) and \( E_2 \), and their associated wave functions in the \( \Gamma \) valley under strong inversion. (In the range of inversion charge density explored in this paper, the occupation of satellite valleys is negligible [17].) Fig. 3(b) shows the depth distribution of charge densities summed over all subbands under strong inversion. Fig. 3(c) shows inversion charge density \( Q_N \) as a function of surface potential \( \varphi_S \), which is the potential on the semiconductor surface with respect to that in the semiconductor bulk. For comparison, the calculated charge densities of a silicon MOSFET with \( N_A = 1 \times 10^{17} \) cm\(^{-3}\) and a 10-nm \( \text{Al}_2\text{O}_3\) gate oxide are also included. It can be seen that, under strong inversion, the Si MOSFET has a higher charge density than the InGaAs MOSFETs mainly due to a higher density of states in the conduction band. Table I lists the parameter values [18] used in the calculation.
TABLE I

<table>
<thead>
<tr>
<th>Channel</th>
<th>Si</th>
<th>In$<em>{0.6}$Ga$</em>{0.4}$As</th>
<th>In$<em>{0.55}$Ga$</em>{0.45}$As</th>
<th>In$<em>{0.75}$Ga$</em>{0.25}$As</th>
</tr>
</thead>
<tbody>
<tr>
<td>$q_0$ (V)</td>
<td>5.1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$k_{ox}$</td>
<td>9.0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C$_{ox}$ (F/cm$^2$)</td>
<td>$8.0 \times 10^{-6}$</td>
<td>$1.0 \times 10^{-6}$</td>
<td>$0.8 \times 10^{-6}$</td>
<td></td>
</tr>
<tr>
<td>$k_s$</td>
<td>11.7</td>
<td>13.9</td>
<td>14.2</td>
<td>14.4</td>
</tr>
<tr>
<td>$m^*$ $(m_0)$</td>
<td>0.19</td>
<td>0.041</td>
<td>0.036</td>
<td>0.032</td>
</tr>
<tr>
<td>$m_0^*$ $(m_0)$</td>
<td>0.98</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\chi$ (V)</td>
<td>4.05</td>
<td>4.51</td>
<td>4.61</td>
<td>4.69</td>
</tr>
<tr>
<td>$E_C$ (eV)</td>
<td>1.12</td>
<td>0.74</td>
<td>0.62</td>
<td>0.53</td>
</tr>
<tr>
<td>$E_F-\rho$ (eV)</td>
<td>$-0.50$</td>
<td>$-0.24$</td>
<td>$-0.12$</td>
<td>$-0.04$</td>
</tr>
<tr>
<td>$E_{IT}$-E$_C$ (eV)</td>
<td>$-0.99$</td>
<td>$-0.63$</td>
<td>$-0.51$</td>
<td>$-0.42$</td>
</tr>
<tr>
<td>$Q_I$ (q/cm$^2$)</td>
<td>$7.4 \times 10^{11}$</td>
<td>$5.0 \times 10^{11}$</td>
<td>$7.7 \times 10^{11}$</td>
<td></td>
</tr>
<tr>
<td>$\rho_{ox}$ (V)</td>
<td>0.06</td>
<td>$-0.04$</td>
<td>$-0.02$</td>
<td>$-0.02$</td>
</tr>
<tr>
<td>$D_{IT}$ (cm$^{-2}$V$^{-1}$)</td>
<td>$4.0 \times 10^{11}$</td>
<td>$1.0 \times 10^{13}$</td>
<td>$5.7 \times 10^{12}$</td>
<td>$1.1 \times 10^{13}$</td>
</tr>
</tbody>
</table>

*relative permittivity of semiconductor  
*electron rest mass  
*electron transverse mass  
*electron longitudinal mass

Gate–source voltage $V_{GS}$ is related to $\varphi_S$ by

$$V_{GS} = \varphi_{MS} + \varphi_S - (Q_B + Q_N + Q_{IT} + Q_T)/C_{OX}$$  \hspace{1cm} (3)

where $\varphi_{MS}$ is the difference between gate metal and semiconductor work functions, $Q_B$ is the depletion charge density in the bulk of the semiconductor, $Q_{IT}$ is the interface charge density, $Q_T$ is the bulk oxide charge density assumed to be concentrated near the oxide–semiconductor interface, and $C_{OX}$ is the oxide capacitance. To evaluate $V_{GS}$ according to (3), $\varphi_{MS}$ was calculated by

$$\varphi_{MS} = \varphi_M - \chi - (E_C - E_F)/q$$  \hspace{1cm} (4)

where $\varphi_M$ is the metal work function, $\chi$ is the electron affinity, $E_C$ is the conduction band minimum, and $E_F$ is the Fermi level in the semiconductor bulk. These parameter values were also included in Table I. $Q_B$ and $Q_N$ were obtained by solving (1) and (2), as previously described.

To calculate interface charge density $Q_{IT}$, interface trap density $D_{IT}$ and charge neutral level $E_0$ [19] are needed. Fig. 4 shows the interface trap density between Al$_2$O$_3$/In$_{0.55}$Ga$_{0.45}$As and Al$_2$O$_3$/In$_{0.75}$Ga$_{0.25}$As MOSFETs measured by the charge-pumping method across the bandgap. The trap energy is relative to conduction band minimum $E_C$. (Dashed curves) Gaussian fit. (Solid lines) $D_{IT}$ levels extrapolated from $D_{IT}$ values at charge neutral levels $E_0$ into the conduction band.

Fig. 4. Interface trap densities $D_{IT}$ in (△) Al$_2$O$_3$/In$_{0.55}$Ga$_{0.45}$As, (◦) In$_{0.65}$Ga$_{0.35}$As, and (□) In$_{0.75}$Ga$_{0.25}$As MOSFETs measured by the charge-pumping method across the bandgap. The trap energy is relative to conduction band minimum $E_C$. (Dashed curves) Gaussian fit. (Solid lines) $D_{IT}$ levels extrapolated from $D_{IT}$ values at charge neutral levels $E_0$ into the conduction band.

IV. ANALYSIS OF ELECTRON MOBILITY

In addition to the inversion charge, low-field electron mobility $\mu$ is another important parameter critical to the transfer characteristics of the $n$-channel MOSFET. Consider the different scattering mechanisms that limit electron mobility, it can be expressed as [20]

$$\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{1}{\mu_R} + \frac{1}{\mu_C}$$  \hspace{1cm} (6)

where $\mu_0$ is the electron mobility in the conduction band, $\mu_R$ is the electron mobility in the bulk of the semiconductor, and $\mu_C$ is the electron mobility in the oxide. Fig. 5 shows the calculated interface charge density $Q_{IT}$ according to

$$Q_{IT} = \int_{E_0}^{E_F} D_{IT}(E) dE$$  \hspace{1cm} (5)

where $E_F$ is the surface Fermi level. The agreement with the experimental data is reasonable.

Fixed oxide charge density $Q_T$ is obtained by fitting the transfer characteristics, as discussed in Section IV. $Q_T$ mainly shifts the current–voltage characteristics along the voltage axis, whereas $Q_{IT}$ also changes its slopes.
where \( \mu_0 \) is the semiconductor bulk mobility accounting for the scattering of bulk and remote phonons, as well as ionized impurities, without considering the screening by the inversion charge, \( \mu_R \) is the interface roughness mobility, and \( \mu_C \) is the Coulomb scattering mobility due to both oxide charge \( Q_{IT} \) and interface charge \( Q_{IT} \).

The InGaAs bulk mobility has been measured in uniform slabs [21] and only needs to be fine-tuned to fit the subthreshold characteristics of the present InGaAs MOSFETs. Table I shows that the measured and fitted values, i.e., \( \mu_0' \) and \( \mu_0 \), respectively, are on the same order of magnitude.

In comparison, the interface roughness mobility needs to be derived by calculating the matrix element of the scattering potential before converting to the scattering rate or the relaxation time through the Fermi golden rule. The perturbation potentials for interface roughness scattering \( V_R \) and Coulomb scattering \( V_C \) [23]

\[
V_R = \frac{1}{4\pi} \sum I \frac{\Delta Q_I}{|\vec{r} - \vec{r}'|} \tag{7}
\]

\[
V_C = qE(z)\Delta(x, y) \tag{8}
\]

respectively, where \( \Delta Q_I \) is the charge of the scattering center, \( \bar{\varepsilon} \) is the average permittivity, \( \vec{r}' \) is the position of the electron in the inversion layer, \( \vec{r} \) is the position of the scattering center, \( E(z) \) is the electric field, and \( \Delta(x, y) \) is the interface roughness, which is assumed to be Gaussian.

Thus, the interface roughness mobility can be expressed as [23]

\[
\mu_R = (9\sqrt{\pi h}/4m^*E_{EFF})(\lambda/\Delta^2) \tag{9}
\]

where \( \lambda \) is the correlation length, \( \Delta \) is the root-mean-square average of \( \Delta(x, y) \), and \( E_{EFF} \) is the effective electric field at the interface according to

\[
E_{EFF} = (Q_B + Q_N/2)/\varepsilon_S. \tag{10}
\]

Since \( Q_B \) and \( Q_N \) can be calculated, as shown in Section III, \( E_{EFF} \) is known, which leaves \( \lambda/\Delta^2 \) as the only fitting parameter for \( \mu_R \).

The Coulomb scattering mobility with screening by the inversion charge for the \( I \)th subband can be expressed in (11) [20], shown at the bottom of the page, where

\[
\bar{\varepsilon} = (\varepsilon_{OX} + \varepsilon_S)/2 \tag{12}
\]

\[
\eta_I = E_I/k_BT \tag{13}
\]

\[
\bar{\varepsilon} = -3\left((12qm^*/h^2\varepsilon_S)[Q_B + (11/32)Q_N]\right)^{-1/3} \tag{14}
\]

\[
a = (2/3h)\sqrt{2m^*k_BT} \tag{15}
\]

and \( k_B \) is Boltzmann’s constant. Therefore, according to [20]

\[
\mu_C = \frac{\sum I \mu_C(E_I)D(E_I)f(E_I)E_I}{\sum I D(E_I)f(E_I)E_I} \tag{16}
\]

where \( D(E_I) \) is the density of states in the semiconductor, and \( f(E_I) \) is the Fermi–Dirac distribution function. Despite the high interface charge density, the Coulomb scattering mobility in the present InGaAs MOSFETs is calculated to be on the order of \( 10^4 \) cm²/Vs or higher and, hence, can only affect the total electron mobility under weak inversion. This is probably because, in the present InGaAs MOSFETs, the inverted electrons are farther away from the oxide than those in a Si MOSFET (see Fig. 3). In addition, under strong inversion, the Coulomb scattering is screened by the inversion charge.

As a summary of the aforementioned mobility analysis, Fig. 6 shows the calculated \( \mu_0, \mu_R, \mu_C, \) and \( \mu \) for the present InGaAs MOSFETs at room temperature. It can be seen that, under strong inversion, the total electron mobility decreases with increasing inversion charge and is mainly limited by the interface roughness mobility, as the bulk mobility is rather high in the present InGaAs MOSFETs with \( N_A = 1 \times 10^{17} \text{ cm}^{-3} \). Even with order-of-magnitude scaling of gate length and doping concentration, the bulk mobility will still be high enough so that, under strong inversion, the total mobility will be mainly limited by interface roughness, unless the interface roughness is significantly improved. By contrast, with higher channel doping and generally lower bulk mobility, the total electron mobility in typical Si MOSFETs is limited by the bulk mobility.

As the interface roughness mobility is not sensitive to temperature, the total electron mobility of the InGaAs MOSFETs exhibits negligible temperature dependence, as shown in Fig. 7. Such temperature insensitivity agrees with the experiment data of In
t_{0.53}Ga_{0.47}As MOSFETs over a much wider temperature range [24]. This confirms that, in the present cases, phonon scattering plays a minor role in determining the electron mobility, particularly when remote phonons are screened by the metal gate [25]–[27].

For compact modeling, the total electron mobility of the present InGaAs MOSFETs under moderate-to-strong inversion can be fitted to a simple power law \( E_{EFF}^{-0.7} \), as shown in Fig. 8. Although it is interesting to extrapolate the power law to 1 MV/cm under which most modern Si MOSFETs operate, it may not be valid because, under such a high field, the electron wave function will move closer to the semiconductor surface and even penetrate into the oxide to degrade the electron mobility faster than what the power law predicts. Unfortunately, high-field tests are not possible because the present InGaAs MOSFETs cannot be biased to higher gate voltages than those shown in Fig. 2. For comparison, the Si universal mobility [28] has also been included in Fig. 8.
Fig. 6. Calculated semiconductor bulk mobility $\mu_0$ (---), interface roughness mobility $\mu_R$ (--), Coulomb scattering mobility $\mu_C$ (••), and total electron mobility $\mu$ (−−−) for (a) In$_{0.75}$Ga$_{0.25}$As, (b) In$_{0.65}$Ga$_{0.35}$As, and (c) In$_{0.53}$Ga$_{0.47}$As MOSFETs at room temperature. In all cases, $\mu$ is mainly limited by $\mu_R$ under strong inversion.

V. EXPERIMENTAL VERIFICATION AND DISCUSSION

The transfer characteristics can be modeled by

$$I_{DS}(V_{GS}) = \left\{ R_{DS} + \left[ \frac{W\mu(V_{GS})Q_N(V_{GS})}{L} \right]^{-1} \right\}^{-1} V_{DS}$$

where $I_{DS}$ is the drain–source current, and $R_{DS}$ is the drain–source series parasitic resistance. The values of $R_{DS}$ were extracted from the measured transfer characteristics of devices with different gate lengths and then optimized to give the best overall fit. $Q_N$ and $\mu$ have been calculated in Sections III and IV, respectively, with $\mu_0$ and $\lambda/\Delta^2$ as fitting parameters.

The optimized values were listed in Table I. Fig. 2 compares in both linear and logarithmic scales the modeled and measured transfer characteristics of the present InGaAs MOSFETs with $V_{DS} = 50$ mV at room temperature and $-50$ °C, respectively. Excellent agreement was achieved from subthreshold to strong inversion.

Table I shows that the extracted interface roughness parameter $\lambda/\Delta^2$ for the present InGaAs MOSFETs is significantly smaller than that of the Si MOSFET, suggesting that the Al$_2$O$_3$/InGaAs interface is rougher than the SiO$_2$/Si interface. The interface roughness values of Si MOSFETs have been characterized through measurements of carrier mobility [22], [29], [30], atomic force microscopy [31], high-resolution transmission electron microscopy [32], and X-ray reflectivity [33]. For the SiO$_2$/Si interface, $\lambda = 0.6$–2.5 nm and $\Delta = 0.2$–0.5 nm. For the interface between a high-$k$ dielectric and Si, $\lambda$ is usually assumed to be the same, but $\Delta$ is slightly larger at 0.3–0.6 nm. Assuming that $\lambda$ is also the same for the Al$_2$O$_3$/InGaAs interface, the extracted $\lambda/\Delta^2$ implies that $\Delta = 1.2$–2.2 nm, which is approximately two to seven times that of the high-$k$/Si interface. Table I also shows that the interface is significantly rougher when the In mole fraction $x \approx 0.5$, which is consistent with poorer transfer characteristics of the In$_{0.53}$Ga$_{0.47}$As MOSFET. However, given the limited sample size, uniformity, and reproducibility, more statistics are needed.
before a firm correlation between the interface roughness and the In mole fraction can be established. For the same reason, no firm correlation between interface roughness and interface trap density can be established at the moment. This paper will have been more complete had the interface roughness of InGaAs MOSFETs been characterized through measurements of atomic force microscopy, high-resolution transmission electron microscopy, or X-ray reflectivity as in the case of Si MOSFETs mentioned earlier.

Fig. 4 shows that, for the present InGaAs MOSFETs with high In mole fractions, although the interface trap density is on the order of $10^{13}$ cm$^{-2}$ eV$^{-1}$ midgap, it rapidly decreases toward the conduction band. Since charge neural level $E_0$ for high In mole fractions is very close to the conduction band (see Table I), inversion-mode operation with good ON-state performance is achievable, whereas the OFF-state performance is still limited by the high interface trap density below $E_0$. Furthermore, although the ON-state performance appears to significantly improve with increasing In mole fraction, since the mobility under strong inversion is mainly limited by the interface roughness, the improved ON-state performance cannot be solely attributed to lighter effective mass or higher bulk mobility with increasing In mole fraction. According to (9), the interface roughness mobility is inversely proportional to the effective mass, and the approximately 20% lighter effective mass in In$_{0.75}$Ga$_{0.25}$As than that in In$_{0.53}$Ga$_{0.47}$As is insufficient to cause the mobility in In$_{0.75}$Ga$_{0.25}$As to be approximately three times that in In$_{0.53}$Ga$_{0.47}$As. Therefore, the better ON-state performance with increasing In mole fraction of the present InGaAs MOSFETs is mainly due to better interface roughness.

In Section III, the inversion charge was calculated by assuming a simple triangular well (see Fig. 3). In reality, the potential well in In$_{0.65}$Ga$_{0.35}$As and In$_{0.75}$Ga$_{0.25}$As MOSFETs contains an additional step between the channel and buffer layers, as shown in Fig. 9. However, it is shown in Fig. 9 that the solution of inversion charge density $Q_N$ for the stepped well is very close to that of the triangular well. This validates the approximation by the triangular well.

VI. Conclusion

Unlike in Si MOSFETs, the electron mobility in InGaAs MOSFETs under strong inversion was found to be mainly limited by the interface roughness. By extracting the mobility from the measured transfer characteristics, the roughness of the Al$_2$O$_3$/InGaAs interface was determined to be two to seven times of that of the SiO$_2$/Si interface. Therefore, to fully benefit from the high bulk mobility of InGaAs, its interface roughness with the gate oxide needs to be further improved.

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References


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