GaSb Inversion-Mode PMOSFETs With Atomic-Layer-Deposited Al2O3 as Gate Dielectric

Min Xu  
Birck Nanotechnology Center, Purdue University

Runsheng Wang  
Birck Nanotechnology Center, Purdue University

Peide D. Ye  
Birck Nanotechnology Center, Purdue University, yep@purdue.edu

Follow this and additional works at: http://docs.lib.purdue.edu/nanopub

Part of the Nanoscience and Nanotechnology Commons

Xu, Min; Wang, Runsheng; and Ye, Peide D., "GaSb Inversion-Mode PMOSFETs With Atomic-Layer-Deposited Al2O3 as Gate Dielectric" (2011). Birck and NCN Publications. Paper 989.  
http://dx.doi.org/10.1109/LED.2011.2143689

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.
GaSb Inversion-Mode PMOSFETs With Atomic-Layer-Deposited Al₂O₃ as Gate Dielectric

Min Xu, Runsheng Wang, Student Member, IEEE, and Peide D. Ye, Senior Member, IEEE

Abstract—GaSb inversion-mode PMOSFETs with atomic-layer-deposited (ALD) Al₂O₃ as gate dielectric are demonstrated. A 0.75-µm-gate-length device has a maximum drain current of 70 mA/mm, a transconductance of 26 mS/mm, and a hole inversion mobility of 200 cm²/V s. The OFF-state performance is improved by reducing the ALD growth temperature from 300 °C to 200 °C. The measured interface trap distribution shows a low interface trap density of 2 × 10¹²/cm²·eV near the valence band edge. However, it increases to 1 – 4 × 10¹³/cm²·eV near the conduction band edge, leading to a drain current on-off ratio of 265 and a subthreshold swing of ~600 mV/decade. GaSb, similar to Ge, is a promising channel material for PMOSFETs due to its high bulk hole mobility, high density of states at the valence band edge, and, most importantly, its unique interface trap distribution and trap neutral level alignment.

Index Terms—Atomic layer deposition, GaSb, high-k, MOSFET.

I. INTRODUCTION

COMPLEMENTARY metal–oxide–semiconductor (CMOS) devices based on Si have been scaled close to their physical limit. To further increase the device performance, III–V semiconductor materials have attracted interest because of their higher electron mobility and saturation velocity. Although significant progress has been made on high-k/III–V NMOSFETs [1]–[3] and Schottky-gate p-channel quantum well transistors [4], [5], there is less work on III–V PMOSFETs [6]. In this letter, we address the fundamental advantages of using GaSb as the p-channel material in a potential full III–V CMOS technology [7], [8]. The validity of this approach is supported by the experimental results on atomic-layer-deposited (ALD) Al₂O₃/GaSb PMOSFETs.

GaSb has a bandgap of 0.73 eV and is near lattice matched to InAs. The hole mobility of GaSb is ~ 1000 cm²/V·s, which is much higher than most other III–V materials [9]. However, the drain current (I_DS) in an inversion-mode MOSFET is not only determined by the mobility and saturation velocity but also by the inversion charge density. The effective density of states in the valence band (Nᵥ) for GaSb is as high as 1.8 × 10¹⁹/cm³ [10], which is also favorable for realizing high-performance GaSb PMOSFETs. The trap neutral level (E₀) position and interface trap distribution play a significant role in the device performance if the oxide/semiconductor interface is nonideal. According to the defect-induced gap-state model developed by Hasegawa and Ohno [11], the empirical model by the authors [12], and the defective interface model by Robertson [13], the E₀ for GaSb should be located around 0.1 eV above the valence band edge (Eᵥ). This particular property makes it easy to realize strong hole inversion.

II. DEVICE FABRICATION

Two-inch n-type GaSb (100) substrates with a doping concentration of 5.5 × 10¹⁷ cm⁻³ were used for MOSFET fabrication. After degreasing by acetone, methanol, and isopropanol, 30-nm Al₂O₃ was deposited at 300 °C in an ASM F-120 ALD chamber as an encapsulation layer using trimethyl aluminum and water as precursors. Source and drain regions were selectively implanted with a Si dose of 2 × 10¹⁴ cm⁻² at 50 keV through the 30-nm Al₂O₃ encapsulation layer [14]. Dopant activation was achieved by a 30-s rapid thermal anneal (RTA) at 650 °C (Process-I samples) or at 600 °C (Process-II and Process-III samples). The encapsulation layer was then removed by buffered oxide etch. The surface was then treated with HCl:H₂O = 1:1 for 30 s to etch away the native oxide and subsequently treated with NH₃OH for 60 s to remove elemental Sb. Following those treatments, 8-nm Al₂O₃ gate dielectrics were regrown by ALD at 300 °C (Process-I and Process-II samples) or 200 °C (Process-III samples). After 600 °C postdeposition anneal (PDA) for 30 s in N₂ ambient, the source and drain ohmic contacts were made by electron beam evaporation of a combination of Pt/Ti/Pt/Au. The gate electrode was defined by electron beam evaporation of Ni/Au. Also, an n-type GaSb substrate with a doping concentration of 5.5 × 10¹⁷ cm⁻³ and a p-type GaSb substrate with a doping concentration of 1.1 × 10¹⁸ cm⁻³ were used for MOSCAPs with 8-nm Al₂O₃ films grown at 300 °C and a 600 °C PDA.

III. RESULTS AND DISCUSSION

Fig. 1(a) shows the schematic cross section of a GaSb inversion-mode PMOSFET with the gate aligned in the (110) direction. Transfer-length-method structures are used to study the implantation/activation. Due to the relatively high substrate doping concentration (5.5 × 10¹⁷ cm⁻³), a high Si implantation dose (2 × 10¹⁴ cm⁻²) was used, requiring a high activation temperature to activate the dopants and recover lattice damage.
The sheet resistance is 390 Ω/sq. for 650 °C activation and 480 Ω/sq. for 600 °C activation, respectively. The source/drain contact resistance (RSH or RDH) is 6.85 Ω · mm for 650 °C and 15.1 Ω · mm for 600 °C activation, respectively, determined from PMOSFETs with different gate lengths. Fig. 1(b) shows the dc output characteristic of a 0.75-μm-gate-length GaSb PMOSFET with Process I. A maximum IDS of 70 mA/mm is obtained at a gate bias of −4 V and a drain bias of −3 V. From the device transfer characteristic, a maximum transconductance gm of ~26 mS/mm is obtained. Note that the IDS and gm achieved here are much larger than those from the previous works on inversion-mode GaAs PMOSFETs [15], [16]. The IDS is larger than the value reported on GaAs p-channel MOS-HFET (IDS ~ 50 mA/mm and gm ~ 50 mS/mm with LG = 0.6 μm) by Passlack et al. [6], while the gm is lower mainly due to the large source/drain contact resistance and the interface traps described as follows. The gate leakage current is below 1 × 10⁻³ A/cm² at −4.0 V gate bias, which is more than six orders of magnitude smaller than the drain on-current.

Fig. 2(a) summarizes all measured drain currents IDS for three different processed samples versus LG at VS = −3.0 V and VS = VT (2/3) · VDS. The drain on-current (ION) is linearly inversely proportional to LG, as expected, and starts to saturate at submicrometer gate length. The ION for Process I is slightly larger than those for Process II and Process III at the same LG due to a higher RTA temperature, thus better ohmic contacts. By the linear extrapolation at VDS = −0.05 V, the VT values of 2-μm-gate-length devices are determined to be −0.5 V for Process I, −0.75 V for Process II, and −1.7 V for Process III. The threshold voltage (VT) for Process III is shifted more negative due to low-temperature ALD dielectric formation, which leads to the reduction of the negative fixed charges in the dielectric [17]. Fig. 2(b) compares the transfer characteristics of 2-μm-gate-length devices for three different processes at VDS = −3 V. The leakage floor of ID at VGS > 0 is mainly determined by the reverse-biased pn-junction leakage current ISUB [1]. The leakage floor of IS at VGS > 0 is mainly due to the high DIT in the bandgap (Process I or II) which impedes further modulation of the channel charges at OFF state. The low values of ID and IS at VGS > 0 for Process III indicate the improvement in both junction leakage and the interface quality. From Fig. 2(b), the values of IS/ID are determined to be 24 and 100 for Process I, 107 and 289 for Process II, and 265 and 454 for Process III from ID and IS, respectively. The inset of Fig. 2(b) shows the saturation drain current for each process and clearly indicates the better OFF-state performance of Process III for GaSb MOSFETs.

Fig. 3(a) shows the temperature-dependent C-V measurements in accumulation [18] on an Al₂O₃/p-GaSb MOSCAP. The frequencies range from 5 to 464 kHz with temperature from 300 K down to 35 K. The very small frequency dispersion at all temperatures in the accumulation capacitance indicates true accumulation and good interface properties near the valence band edge. The room-temperature minority carrier (electron) or trap response at positive bias is suppressed at 77 K or 35 K. Note that, even at temperature as low as 35 K, the accumulation capacitance does not decrease significantly, in great contrast to GaAs [18]. This results from the high Nᵥ for GaSb. This allows the channel to get sufficiently high hole density with less E₊ movement.

Fig. 3(b) shows the DIT distribution across the whole GaSb bandgap. The DIT value near EV is 2 × 10¹² /cm² · eV determined by the measured low-f and high-f C-V method shown in Fig. 3(a). The temperature-dependent conductance method is also employed to quantitatively map the DIT distribution inside the bandgap and near Eᵥ for majority carriers in n-type GaSb MOSCAPs. It is found that the DIT for GaSb, similar to Ge without good passivation, increases rapidly to 1 – 4 × 10¹³ /cm² · eV in the bandgap and 1 – 2 × 10¹³ /cm² · eV near Eᵥ. Better DIT inside the bandgap for Process III is also consistent with the better OFF-state performance of PMOSFETs with Process III, as shown in Fig. 2(b). The determined DIT distribution at the Al₂O₃/GaSb interface clearly explains why strong inversion and reasonable drain current can be obtained on GaSb PMOSFETs. GaSb has a similar band alignment to the trap neutral level E₀ as Ge [12], [13], [19]. The previously demonstrated GaSb PMOSFET and DIT distribution further


