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http://dx.doi.org/10.1063/1.3622306

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Citation: Appl. Phys. Lett. 99, 052108 (2011); doi: 10.1063/1.3622306
View online: http://dx.doi.org/10.1063/1.3622306
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v99/i5
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Atomic-layer-deposited Al$_2$O$_3$ on Bi$_2$Te$_3$ for topological insulator field-effect transistors

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(Received 22 April 2011; accepted 5 July 2011; published online 4 August 2011)

We report dual-gate modulation of topological insulator field-effect transistors (TI FETs) made on Bi$_2$Te$_3$ thin flakes with integration of atomic-layer-deposited (ALD) Al$_2$O$_3$ high-k dielectric. Atomic force microscopy study shows that ALD Al$_2$O$_3$ is uniformly grown on this layer-structured channel material. Electrical characterization reveals that the right selection of ALD precursors and the related surface chemistry play a critical role in device performance of Bi$_2$Te$_3$ based TI FETs. We realize both top-gate and bottom-gate control on these devices, and the highest modulation rate of 76.1% is achieved by using simultaneous dual gate control. © 2011 American Institute of Physics. [doi:10.1063/1.3622306]

Three dimensional topological insulator (TI) materials, such as Bi$_2$Te$_3$, Bi$_2$Se$_3$, and Sb$_2$Te$_3$, have recently attracted much attention due to their unique physical properties. These structures are layered like graphene but appear to behave like insulators having a band gap in the material bulk. However, these materials show metallic behavior on their surfaces. The surface states of TIs consist of an odd number of massless Dirac cones, around which the linear dispersion of the electron spectrum is such that the carriers reach extremely high surface carrier mobilities up to 9000-10 000 cm$^2$/Vs. Moreover, these surfaces, protected by time reversal symmetry, result in a non-scattering carrier transport regime, making TIs rather promising for future nanoelectronics applications with ultralow power dissipation.

In order to realize practical TI field-effect transistors (FETs), it is important to study the integration of gate dielectrics on these materials so that the channel current can be controlled by the top-gate. In some early studies of Bi$_2$Te$_3$ based TI devices, where a heavily doped silicon back gate was used, no modulation was observed within a back-gate voltage sweep from −50 V to 50 V at room temperature. The highest modulation obtained is around 20% measured at 50 V to 50 V at room temperature. The highest modulation obtained is around 20% measured at 50 V to 50 V at room temperature. For Bi$_2$Se$_3$, which has a larger bandgap of 0.3 eV than 0.14 eV of Bi$_2$Te$_3$, minuscule gate modulation was reported using top-gate control at room temperature, while much larger modulation was achieved by the back-gate sweeps. Although these are inspiring results to observe the field effect by using a global back-gate, this cannot satisfy the requirement for real device applications, which requires individual device top-gate control and room temperature operation. Therefore, the realization of highly efficient top-gate modulation for Bi$_2$Te$_3$ and other TI materials at room temperature is urgently needed.

In this letter, we demonstrate Al$_2$O$_3$ growth by atomic-layer deposition (ALD) with two different precursors on Bi$_2$Te$_3$ top surfaces. The uniformity of the surface morphology after the ALD Al$_2$O$_3$ deposition is also studied. Electrical characterization has shown a strong modulation of Bi$_2$Te$_3$ based TI FETs with both top-gate and back-gate controls. Bi$_2$Te$_3$ thin flakes were peeled off from bulk ingots by standard 3M scotch tape techniques and were then transferred to a highly doped silicon wafer with 300 nm thick SiO$_2$. The thickness of these ultrathin flakes is less than 50 nm. Ten nanometer Al$_2$O$_3$ high-k dielectric layers were deposited by an ASM F-120 ALD system at 200°C by using tri-methyl-aluminum (TMA) and H$_2$O or TMA and O$_3$ as precursors. The pulse time is 0.8 s TMA and 1.2 s H$_2$O, or 1 s TMA and 1 s O$_3$, and the purge time is 6 s N$_2$ for each precursor. Source/drain regions were defined by optical lithography. Al$_2$O$_3$ was etched away using buffered oxide etch (BOE) at these source/drain regions, followed by e-beam evaporation of a 20 nm/40 nm Cr/Au metal and lift-off process for ohmic contacts. A 10 nm/50 nm Cr/Au layer was finally deposited as the top-gate. Final device structure is shown in Figure 1(a), which is similar to a traditional metal-oxide-semiconductor FET, but with two conducting surfaces and one conducting bulk channel in the channel region.

The crystal structure of Bi$_2$Te$_3$ has been shown to be similar to graphene, with stacking layers bonded by the Van der Waals force. The lattice constant for hexagonal Bi$_2$Te$_3$ is 0.4384 nm for the a-axis and 3.045 nm for the c-axis. Each layer of Bi$_2$Te$_3$, a quintuple layer with the thickness of ~1 nm, consists of the five layer sequence Te-Bi-Te-Bi-Te. Three quintuple layers form one unit cell. On the top and bottom Te layers, there are no dangling bonds at the surface. This may lead one to suspect that it is not possible to deposit ALD Al$_2$O$_3$ directly on these flakes because there would be no chemical absorption due to the absence of dangling bonds at surface, as generally seen in the case of graphene. Early studies also revealed that ALD Al$_2$O$_3$ fails to be deposited on graphene surfaces but would only cluster and grow on graphene edges and ultimately form nanoribbons. However, our results show that this problem does not occur for Bi$_2$Te$_3$. A Veeco Dimension 3100 AFM was used to study the flake surface and the layer edges after Al$_2$O$_3$ deposition. The pristine Bi$_2$Te$_3$ surface was studied after peeling and being transferred to SiO$_2$/Si substrates. We notice the surface is not as smooth as the graphene surface. This might be attributed to the fact that Bi$_2$Te$_3$ is not as highly air-stable as...
graphene; oxygen and water molecules in air can slightly oxidize the Te-terminated surface. This oxidation facilitates the following ALD process by creating nucleation spots for precursor absorption. The smallest step observed is \( \sim 1 \text{ nm} \) corresponding to the thickness of one quintuple layer. Most of terraces have the heights of single or multiple unit cells.

Figure 1(b) shows the surface morphology of Bi\(_2\)Te\(_3\) surface after 20 cycles of ALD growth using TMA and H\(_2\)O, corresponding to \( \sim 1.8 \text{ nm} \) Al\(_2\)O\(_3\) deposition. In the graphene case, the surface of graphene remained intact while Al\(_2\)O\(_3\) nanoribbons are clearly formed at the graphene edges.\(^{17}\) No Al\(_2\)O\(_3\) nanoribbons or clusters can be observed at the Bi\(_2\)Te\(_3\) layer edges. Figure 1(c) shows that ALD Al\(_2\)O\(_3\) is conformal and uniformly coated on a series of steps of the peeled Bi\(_2\)Te\(_3\) surface with the relative step height remaining similar before ALD.

Electrical characterization was performed after device fabrication using a Keithley 4200. Two devices, one using TMA/H\(_2\)O (Device 1) and another using TMA/O\(_3\) (Device 2) as precursors for Al\(_2\)O\(_3\) are studied here. The typical geometric features are 2 \( \mu \text{m} \) in gate length and 1 \( \mu \text{m} \) in gate width. The channel resistance, including the contact resistance, for Devices 1 and 2 are 32 k\( \Omega \) and 25 k\( \Omega \), respectively, indicating that the flake thicknesses are similar. Linear I-V characteristics indicate a good ohmic contact to the Bi\(_2\)Te\(_3\) flakes. Figures 2 shows independent top-gate and back-gate modulation for both devices with another gate floating. The top-gate and back-gate leakage currents are less than \( 10^{-10} \text{ A} \). We do not observe an electron-hole or ambipolar transition because the strong stoichiometric doping of Bi\(_2\)Te\(_3\) makes it an n-type material with an estimated doping concentration of \( \sim 10^{19} \text{ cm}^{-3} \).

For Device 1, a maximum of 45.6% modulation is reached through back-gate control, where the back-gate voltage is swept from \(-50 \text{ V}\) to \(50 \text{ V}\). We calculate the transconductance (\( g_m \)) to be 9.8 nS. Comparatively, the top gate \( g_m \) is measured 60 nS at its maximum, six times larger than the back-gate \( g_m \) due to the thinner top dielectric thickness and higher k value. Though we get an improved value for transconductance by top-gate control, the improvement is not as high as we expect considering the oxide thickness and dielectric constant for both SiO\(_2\) as back-gate oxide and Al\(_2\)O\(_3\) for top-gate oxide. The top-gate \( g_m \) should be around 60 times larger than back-gate \( g_m \) if we don’t consider top-gate partial coverage of the channel and roughly estimate the practical dielectric constant of Al\(_2\)O\(_3\) to be \( \sim 7.8 \), twice that of SiO\(_2\). The stark contrast between predicted and measured values indicates non-ideal Al\(_2\)O\(_3\)/Bi\(_2\)Te\(_3\) interfaces, which is consistent with the discussions above. Also, from the extrinsic transconductances, we can estimate the low limit of the effective electron mobility with top-gate control to be \( \sim 1.69 \text{ cm}^2/\text{Vs} \) and with back-gate control to be \( \sim 17.0 \text{ cm}^2/\text{Vs} \). This effective mobility contains two parts, the surface state mobility and the bulk mobility. The results indicate that the low mobility bulk channel is the dominant conducting channel and the high mobility surface channels are degraded by the poor interfaces, in
particular, the top interface. Poor interface conditions easily result in a strong degradation of field-effect modulation efficiency as demonstrated in ALD high-k/III-V MOSFETs.\textsuperscript{19} Compared to III-V MOSFETs, such interface degradation in Bi\textsubscript{2}Te\textsubscript{3} could impose more serious problems in device performance due to its unique carrier transport properties. It has been stated in previous studies that the conductance of those topological insulators is composed of two parts: the bulk conductance and the surface conductance, including the top surface conductance and bottom surface conductance.\textsuperscript{10} The two surface conducting channels are of interests due to its high mobility and non-scattering carrier transport. Considering the large intrinsic carrier density in its bulk, the top surface is more sensitive to the top gate control than the bottom surface, so the two surfaces do not play symmetric roles under gate bias. The bottom surface has a better interface condition with the back SiO\textsubscript{2} dielectric as it has been left intact during the bias. The bottom surface has a better interface condition with high carrier mobility and velocity. Any formation of top-channel material for device applications is its surface channel for device applications based on top-gate dielectric on semiconductors cannot be as important as on TI since the conducting channel is on the surface.

In conclusion, we have investigated ALD high-k oxide formation on Bi\textsubscript{2}Te\textsubscript{3} as a top-gate dielectric. AFM studies reveal the feasibility of direct ALD of high-k dielectrics on this layered material. Electrical characterization shows a pronounced modulation by both top-gate and back-gate with the highest modulation of 76.1% achieved with simultaneous dual gate control. However, at this point, the top-gate modulation is not as effective as the back-gate modulation at the same electrical field due to the degraded interface between the ALD dielectric and the TI. Further studies on protecting the TI surface during ALD dielectric formation are on-going.\textsuperscript{21–23}

The authors would like to thank X. Xu, C. Liu, G. Q. Xu, Y.P. Chen, A.T. Neal, and N. Conrad for valuable discussions and E. Milligan, W.J. Qian, J.F. Tian, and M. Xu for technical assistance. The work is supported by DARPA/MESO program.

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\textsuperscript{1}M. Z. Hasan and C. L. Kane, Rev. Mod. Phys. \textbf{82}, 3045 (2010).
\textsuperscript{5}L. Fu and C. L. Kane, Phys. Rev. B \textbf{76}, 045302 (2007).
\textsuperscript{6}D. X. Qu, Y. S. Hor, J. Xiong, R. J. Cava, and N. P. Ong, Science \textbf{329}, 5993 (2010).
\textsuperscript{8}D. Teweldebrhan, V. Goyal, and A.A. Balandin, Nano Lett. \textbf{10}, 1209 (2010).