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Performance Comparisons of III-V and strained-Si in Planar FETs and Non-planar FinFETs at Ultra-short Gate Length (12nm)

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Abstract*— The exponential miniaturization of Si CMOS technology has been a key to the electronics revolution. However, the downscaling of the gate length becomes the biggest challenge to maintain higher speed, lower power, and better electrostatic integrity for each following generation. Both industry and academia have been studying new device architectures and materials to address this challenge. In preparation for the 12nm technology node, this paper assesses the performance of the $In_{0.75}Ga_{0.25}As$ of III-V semiconductor compounds and strained-Si channel nano-scale transistors with identical dimensions. The impact of the channel material property and device architecture on the ultimate performance of ballistic transistors is theoretically analyzed. 2-D and 3-D real-space ballistic quantum transport models are employed with band structure non-parabolicity. The simulation results indicate three conclusions: 1) the $In_{0.75}Ga_{0.25}As$ FETs do not outperform strained-Si FETs, 2) triple-gate FinFETs surely represent the best architecture for sub-15nm gate contacts, independently from the material choice, and 3) The simulations results further show that the overall device performance is very strongly influenced by the source and drain resistances.

***Index Terms*— III-V vs. Si, InGaAs, strained-Si, single-gate, double-gate, triple-gate, MOSFETs, FinFETs, real-space effective mass simulations**

I. Introduction

Novel materials and device architectures are required that will outperform conventional Si-based FETs at ultra-scaled dimensions to keep improving the performance of nano-scale transistors [1-16]. In particular, it has been demonstrated that InGaAs FETs can exhibit performance superior to Si FETs because of their very high electron mobility. This may enable high speed and low power logic applications beyond Si-CMOS technology [2, 4, 8-10, 14-19]. However, due to recent innovations in strain engineering, which have boosted its electron and hole mobilities, Si is still the most popular material and is widely used as the CMOS channel material in industry [6, 20-21].

A significant challenge associated with the downscaling of transistors is the poor electrostatic control of a single-gate contact over the channel of ultra-scaled devices calling short channel effects (SCE). Multi-gate architectures [2-3, 8, 11, 22-24], as recently introduced by Intel for the 22nm technology node [25], can help suppress SCE, even at short gate lengths, deliver near-ideal sub-threshold slopes, and reduce drain induced barrier lowering (*DIBL*) [2-3].

In preparation for the 12nm technology node, this paper investigates the performance of single-/double-gate planar ultrathin-body (UTB) FETs and triple-gate FinFETs employing $In_{0.75}Ga_{0.25}As$ as a channel material and compares them to strained-Si channel FETs. The high-κ gate dielectric, HfO_2, is used as an insulator to circumvent the gate leakage current caused by tunneling across the gate oxide [8, 10, 16, 26].

Since fabricating III-V and Si nano-scale transistors with identical dimensions and electrical properties is very difficult, time consuming, and expensive, the performance of all the devices considered in this work are simulated using a state-of-art computer aided design tool [16-17, 26-30] and not extracted from an experimental setup. Numerical device simulations provide a comprehensive way to capture the electrical behavior of different devices with different materials and structures for performance assessment as long as the same set of approximations is used in all cases.

The theoretical modeling of two-dimensional (2-D) and three-dimensional (3-D) nano-scale transistors demands a proper treatment of quantum effects such as the energy level quantization caused by strong quantum confinement of electrons and band structure non-parabolicity. To address these issues, a multi-dimensional quantum transport solver based on a self-consistent solution of the Schrödinger and Poisson equations in the real-space effective mass approximation [18] with a tight-binding extraction of the effective mass values is used to simulate III-V and strained-Si devices in planar and non-planar architectures [17, 27]. With this simulation approach, the *I-V* characteristics of realistic III-V high electron mobility transistors could be accurately reproduced [16-18]. Electron-phonon scattering [28], surface roughness [29], alloy disorder [30], and tunneling gate leakage [26] can in principle be included in the simulations. However, they are not included due to high computation cost in real-space

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modeling and all the FETs are simulated in the ballistic limit of transport.

This paper is organized as follows. Section II describes the single-/double-gate planar UTB FETs and triple-gate FinFET structures, and introduces the simulation approach. The performance of devices employing $In_{0.75}Ga_{0.25}As$ and strained-Si channels are compared and analyzed in Section III. Finally, Section IV summarizes the main findings of this paper and concludes it.

II. Device Description And Simulation Approach

The device schematics of the single-/double-gate UTB FETs and triple-gate FinFETs modeled in this work are shown in Fig 1. An $In_{0.75}Ga_{0.25}As$ layer on an $In_{0.52}Al_{0.48}As$ buffer is used as the channel material for III-V FETs [14-16]. The source and drain regions are n-doped with a donor concentration N_D=5×10^{19} cm^{-3} and a length of 20nm. Transport occurs along the <100> crystal axis. A 1% uniaxial stress is applied to the <110>-oriented Si channels with a SiO_2 substrate. Strain is used to achieve a higher electron velocity resulting from a reduction of the effective mass (m^*) parallel to the stress direction [6, 20-21]. The source and drain regions of the Si transistors are n-doped with a donor concentration N_D=1×10^{20} cm^{-3} and a length of 20nm.

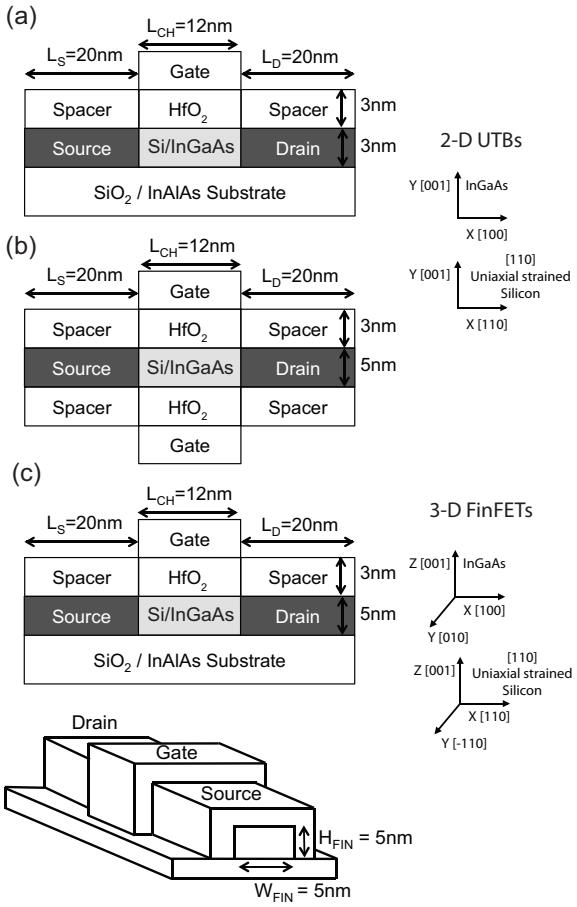

Fig. 1. Schematics of the simulated devices (a) Single-gate planar UTB FET (b) Double-gate planar UTB FET (c) 2-D and 3-D schematics of triple-gate FinFET.

All architectures use an HfO_2 high-κ gate stack with a relative dielectric constant ε_R = 20, a thickness t_{OX}=3nm, and a conduction band gap offset ΔE_C = 2.3 eV and 2.48 eV for $In_{0.75}Ga_{0.25}As$ and Si, respectively [31-32]. This corresponds to an equivalent oxide thickness EOT of 0.585nm, consistent with the ITRS specifications for the 12nm technology node [1]. The source and drain regions are covered by spacers made of a low dielectric material (ε_R = 5) to reduce the electric fields coupling to the gate.

The simulated III-V and Si UTB FET and FinFET devices have the same geometry and gate stacks, but different channel materials and doping concentrations. The OFF-current of all the devices is set to 0.1 μA/μm by varying the work function of the metal gate contact.

To reduce the computational burden, the device structures are simulated in two steps. First, only the intrinsic domain, as illustrated in Fig. 1, is considered. Then, the source (R_S= 80 Ω-μm) and drain (R_D= 80 Ω-μm) series resistances taken from the ITRS are added in a post-processing step to the intrinsic *I-V* characteristics. This procedure was described previously in Ref. [16].

The real-space quantum transport solver OMEN is used to simulate the 2-D and 3-D FETs in Fig. 1 in the ballistic transport regime. The Schrödinger and Poisson equations are solved self-consistently using the effective mass approximations and a finite difference grid. To account for the strong non-parabolicity of III-V materials, the effective masses of the $In_{0.75}Ga_{0.25}As$ based transistors are extracted from a $sp^3d^5s^*$ tight-binding (TB) band structure calculation including spin-orbit coupling [14-16].

Architecture	Channel Material	m_X	m_Y	m_Z	Degeneracy
Single-gate	$In_{0.75}Ga_{0.25}As$	0.066	0.0159	0.066	1
UTB FETs	[110] 1% Uniaxial	0.16	0.9	0.22	2
2-D	Strained Silicon	0.5	0.19	0.31	4
Double-gate	$In_{0.75}Ga_{0.25}As$	0.059	0.0109	0.059	1
UTB FETs	[110] 1% Uniaxial	0.16	0.9	0.22	2
2-D	Strained Silicon	0.5	0.19	0.31	4
Triple-gate	$In_{0.75}Ga_{0.25}As$	0.0706	0.0769	0.0769	1
FinFETs	[110] 1% Uniaxial	0.16	0.22	0.9	2
3-D	Strained Silicon	0.5	0.31	0.19	4

Table 1. Transport and confinement effective masses and subband degeneracy for the $In_{0.75}Ga_{0.25}As$ and strained-Si planar UTB FETs and triple-gate non-planar FinFETs.

The transport effective masses (m_t) for the $In_{0.75}Ga_{0.25}As$ transistors are obtained by fitting the curvature of the lowest tight-binding conduction band with a parabola. The confinement effective masses (m_c) are chosen so that the energy difference between the two lowest tight-binding conduction bands is correctly reproduced by the effective mass model. The layers around the $In_{0.75}Ga_{0.25}As$ channel are taken into account when the effective masses are extracted from the tight-binding band structure so that the electron wave function can deeply penetrated into them, resulting into a larger transport effective masses. This method delivers

structure-dependent effective masses which are quite different from their bulk value, yet are in good agreement with experimental data [16].

There are two sets of effective masses for the stained-Si devices with transport along the <110> crystal axis covering the six-fold-degenerate valleys of Si. First, there is a group of four-fold-degenerate valleys with the same transport and confinement effective masses extracted as in Ref. [33-34]. Since the corresponding energy quantization levels are relatively high in energy, strain is not considered for these bands. The second group of two-fold-degenerate valleys requires more attention because by applying a uniaxial tensile stress strain strongly influences the value of their transverse effective masses strongly decreases, leading to better transport properties. The effective masses in this case were taken from Ref. [20] and were verified using the Vienna Ab-initio Simulation Package (VASP) [35]. All the effective masses used in this work are summarized in Table 1.

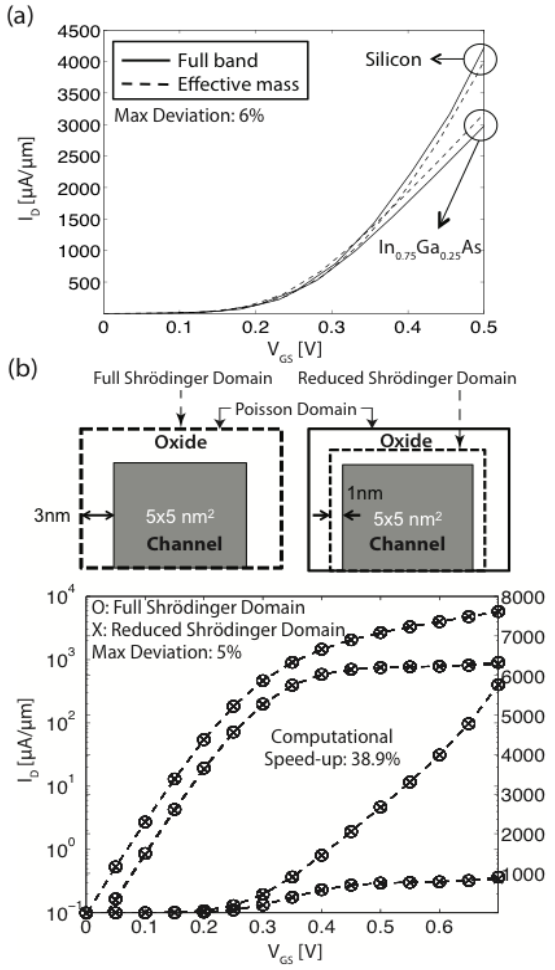

Fig. 2. (a) Basis reduction: comparison of the full-band (solid lines) and effective mass (dashed lines) I_D-V_{GS} characteristics at V_{DS}=0.7 V (b) Domain reduction: comparison of I_D-V_{GS} characteristics of the strained-Si FinFET at V_{DS}=0.05 V and V_{DS}=0.7 V simulated using the entire Fin cross section (crosses) and reduced spatial domain that captures the wave function leakage (circles).

Full-band atomistic simulations are too computationally expensive to be applied to the complete full *I-V* characteristics of large 3-D device structures as shown in Fig. 1. However, to verify that our method that extracts effective masses from tight-binding band structures works well, the intrinsic I_D-V_{GS} of the $In_{0.75}Ga_{0.25}As$ and strained-Si 3-D FinFETs are simulated in the effective mass approximation and compared to the atomistic tight-binding model [27] at a single V_{DS}=0.7 V. The results in Fig. 2 (a) show that both methods exhibit identical trends with values of drain current very close to each other when I_D < 3000 μA/μm. This corresponds to the domain of interest and demonstrates that a simulation approach based on the effective mass approximation can be used when it is well-calibrated against a full band model. We note here again that the effective masses used for such agreement are significantly different from the bulk values and heavily influenced by device geometry and confinement details. The use of un-calibrated bulk-based effective masses would yield significantly different results and would not enable a realistic comparison between the Si and InGaAs material systems.

Apart from the band structure model, another severely limiting factor in the simulation of 3-D FinFETs is the size of their cross-section which increases the solution time for the Schrödinger equation in real-space. While the entire cross section needs to be included to solve the Poisson equation, the simulation domain of the Schrödinger equation can indeed be reduced. The electron wave function does not extend all along the surrounding dielectric layers, and the Schrödinger domain can therefore be restricted to 1nm around the $In_{0.75}Ga_{0.25}As$ and Si channel. This is illustrated in Fig. 2 (b). The I_D-V_{GS} transfer characteristics of the strained-Si FinFET at V_{DS}=0.05 V and 0.7 V are shown in Fig. 2 (b) in logarithmic and linear scale. A maximum deviation between the full and the reduced Schrödinger domain solutions of 5% is observed. Consequently, by reducing the simulation domain for the Schrödinger equation, the simulation time for the whole I_D-V_{GS} characteristics consistent of 16 bias points decreases about 39% from 90 hours to 55 hours on 256 cores on 2.5GHz quad core AMD 2380 processors [36].

III. Results And Discussion

Based on the methodology presented in Section II we have simulated the III-V and strained-Si UTB FETs and FinFETs shown in Fig. 1. From the resulting transfer I_D-V_{GS} and output I_D-V_{DS} characteristics, some key technology parameters such as, *SS*, *DIBL*, ON-current (I_{ON}), ballistic injection velocity (V_{INJ}), and inversion charge density (N_{INV}) were extracted for each device.

As explained earlier, the source and drain contact regions extending beyond the intrinsic device are excluded from the quantum transport simulation. These extrinsic source and drain regions are characterized by two series resistances (R_S and R_D) included as a post-processing step where the intrinsic $V^*_{GS,in} = V_{GS,ext} - I_D R_S$ and $V^*_{DS,in} = V_{DS,ext} - I_D (R_S + R_D)$ account for the correction. For example, the simulated ON-current of $In_{0.75}Ga_{0.25}As$ triple-gate FinFET is extracted at $V_{GS} = V_{DS} = 0.7$ V and amounts to I_{ON}/W= 2490 μA/μm, but the intrinsic biases are $V_{GS,in}$ = 0.5 V, $V_{DS,in}$ = 0.3 V with

R_S = 80 Ω-μm = R_D = 80 Ω-μm. This method has been applied previously and showed good agreement with experimental data [16-18]. Note that drain current of the triple-gate FinFET is normalized by the Fin-height of H_{Fin} = 5nm [37].

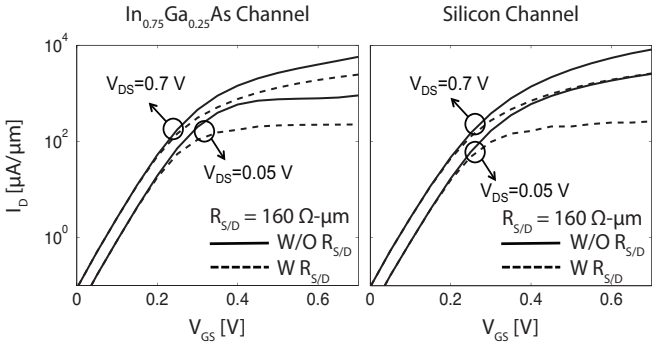

Fig. 3. Intrinsic (solid lines) and extrinsic (dashed lines) I_D-V_{GS} characteristics of triple-gate FinFETs for (a) $In_{0.75}Ga_{0.25}As$ and (b) strained-Si channels.

Fig. 3 shows the intrinsic I_D-V_{GS} and the post-processed I_D-V_{GS} transfer characteristics of the $In_{0.75}Ga_{0.25}As$ and strained-Si triple-gate FinFETs at V_{DS}=0.05 V and V_{DS}=0.7 V. The source and drain series resistances have a negligible effect on the OFF-state, but they significantly reduce the drain current in the ON-state, by more than 50% in both FETs: the ON-current of the $In_{0.75}Ga_{0.25}As$ triple-gate FET decreases from 5768 μA/μm to 2490 μA/μm after the post-processing. It is clear that the extrinsic source and drain contact regions dominate the overall performance of both device types. Hence, careful and low resistance of contact designs may turn out to be even more important than the optimization of the central device in future device architectures, regardless of the channel material.

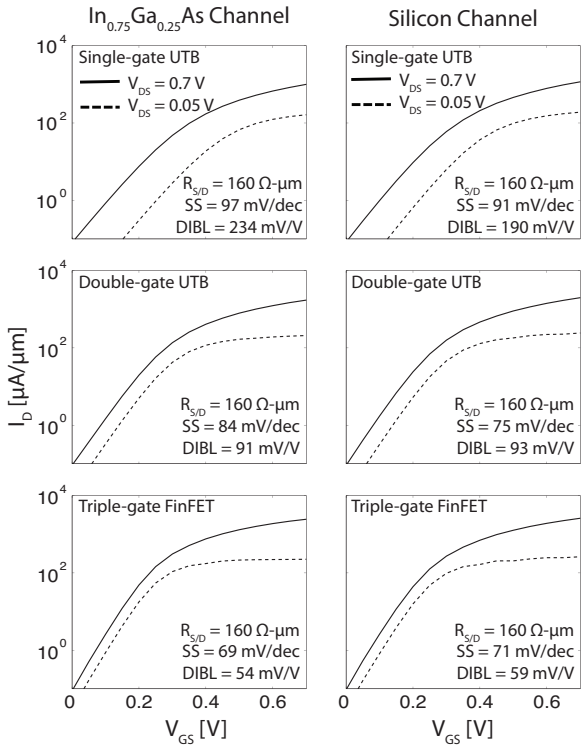

Fig. 4. I_D-V_{GS} characteristics for the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs for two given drain voltage V_{DS} = 0.05 V and V_{DS} = 0.7 V with different gate voltages V_{GS} from 0.0 to 0.7 V (steps of 0.05 V) in semi-log scale.

Figures 4 and 5 show the ballistic transfer and output characteristics of the simulated devices after the inclusion of the series resistances. All the performance parameters (*SS*, *DIBL*, I_{ON}, V_{INJ} and N_{INV}) are extracted from *I-V* characteristics shown in Fig. 4 and Fig. 5. The values are reported in Table 2, where the effect of the contact series resistances are taken into account. The power supply voltage for each device is set to 0.7 V to meet the ITRS ON-current requirements for III-V and Si devices [1, 9], and the metal gate work functions are tuned to obtain the same OFF current (I_{OFF}=0.1 μA/μm). Note that for the single-gate transistors a body thickness (T_{body}) of 3nm is needed, because severe SCE are observed with T_{body}=5nm.

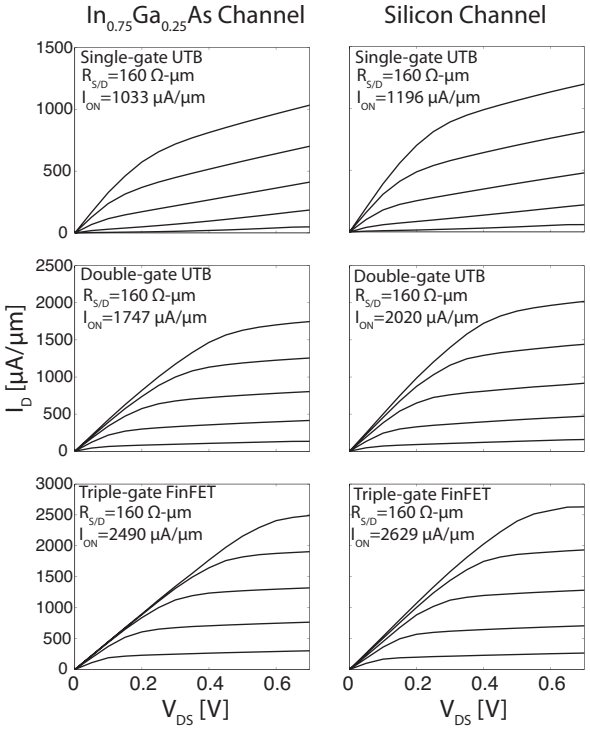

Fig. 5. I_D-V_{DS} characteristics of the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs at six different gate voltages V_{GS} = 0.0 V, 0.3 V, 0.4 V, 0.5 V, 0.6 V and 0.7 V.

For example, the $In_{0.75}Ga_{0.25}As$ based single-gate FET shows a *SS* of 148 mV/decade and *DIBL* of 441 mV/V when T_{body}=5nm while these values are reduced to 97 mV/decade and 234 mV/V when T_{body}=3nm. Also, to maintain a full substrate depletion in the single-gate structure the body thickness should be about 1/3 of the gate length. In the case of double-gate and triple-gate transistors the same body thickness (T_{body}=5nm) is employed for comparison under the same conditions. From the extracted performance parameters, the impact of the channel material property and device architecture on the ultimate performance of ballistic transistors is examined theoretically.

Most III-V compound semiconductors such as $In_{0.75}Ga_{0.25}As$ (E_G = 0.53 eV, m^* = 0.032m_0, ε_R = 14.4), InAs (E_G = 0.36 eV, m^* = 0.023m_0, ε_R = 15.15), and InSb (E_G =

Structure	Single-gate		Double-gate		Triple-gate	
Material	InGaAs	Si	InGaAs	Si	InGaAs	Si
SS [mV/dec]	97	91	84	75	69	71
DIBL [mV/V]	234	190	91	93	54	59
I_{ON} [μA/μm]	1033	1196	1747	2020	2490	2629
V_{INJ} [cm/s]	3.3×10^{7}	1.1×10^{7}	4.5×10^{7}	9.5×10^{6}	4.7×10^{7}	1.1×10^{7}
N_{INV} [/cm^2]	1.5×10^{12}	5.7×10^{12}	2.1×10^{12}	1.1×10^{13}	3.7×10^{12}	1.8×10^{13}

Table 2. Device performance parameters for the $In_{0.75}Ga_{0.25}As$ and strained-Si in sinlge-/double-gate planar FET and triple-gate FinFET configuration. The power supply voltage (V_{DD}) for each device is set to 0.7 V, and the OFF current (I_{OFF}) is set to 0.1 μA/μm. *SS* is observed for the saturated value of V_{GS}.

0.18 eV, $m^* = 0.014m_0$, $\varepsilon_R = 16.8$) have a significantly lower band gap (E_G), smaller electron effective mass (m^*), as well as higher relative dielectric constant (ε) than Si. These properties make devices employing III-Vs more prone to SCE compared to Si. Multi-gate architectures become important to reduce SCE in ultra-scaled devices especially for III-Vs.

As shown in Table 2, SCE are significantly suppressed in terms of *SS* and *DIBL* in multi-gate structures while single-gate structures can not achieve decent performance parameters, even with a 3nm of body thickness: planar double-gate structures lead to a *SS* improvement of about 13% for the $In_{0.75}Ga_{0.25}As$ FET and 18% for the strained-Si FET as compared to the single-gate devices. The *SS* of the triple-gate FinFET is improved by about 29% for the $In_{0.75}Ga_{0.25}As$ FET and about 22% for the strained-Si FET as compared to their single-gate planar counterparts.

More impressive results are the improvements of *DIBL* when going from planar single-gate to planar double-gate structures and non-planar triple-gate FinFETs: for the $In_{0.75}Ga_{0.25}As$ FET, *DIBL* decreases from 234 mV/V (single-gate) to 91 mV/V (double-gate) and further down to 54 mV/V when used as a FinFET. In strained-Si, the same trend can be observed, *DIBL* is reduced from 190 mV/V to 93 mV/V for the double-gate structures and finally down to 59 mV/V for the triple-gate FinFET. From these results, it can be concluded that only multi-gate structures, and especially triple-gate FinFETs provide a good enough electrostatic channel control and minimize the short channel effects as the transistor gate lengths are scaled down below the 15nm technology node.

The observed trends in DIBL of Fig 6. (a) can be explained by invoking the concept of the geometric screening length for fully depleted (FD) SOI MOSFETs from D. J. Frank et al. [38]. The geometric screening length (λ [nm]) is used as a measure of SCE inherent to a device structure [11, 21, 39]. It describes the electrostatic controllability of the depletion region in the channel. The SCE are proportional to the geometric screening length. A shorter geometric screening length reduces the influence of the drain contact on the channel region and suppresses SCE. In addition, an increased number of gates with the same dimension of body thickness (T_{Body}) and oxide thickness (T_{OX}) reduce the geometric screening length, as shown in Equation (1) [11, 19], where the subscript of each λ represents the number of gates.

$$\lambda_1 = \sqrt{\frac{\varepsilon_{Body}}{\varepsilon_{OX}} T_{Body} T_{OX}}, \quad \lambda_2 = \sqrt{\frac{\varepsilon_{Body}}{2\varepsilon_{OX}} T_{Body} T_{OX}}, \quad \lambda_3 = \sqrt{\frac{\varepsilon_{Body}}{3\varepsilon_{OX}} T_{Body} T_{OX}} \quad (1)$$

Fig. 6 (b) illustrates the behavior of the geometric screening length in the $In_{0.75}Ga_{0.25}As$ FET and strained-Si single-, double-, and triple-gate devices. As it can be seen, the non-planar triple-gate FinFET exhibit the lowest geometric screening length and best electrostatic control among all three architectures in terms of *SS* and *DIBL*. The behavior of the geometric screening length also captures the higher improvement rate of SCE in the $In_{0.75}Ga_{0.25}As$ transistors as the number of gates increases. Indeed, the difference between the geometric screening length of the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs ($\Delta\lambda_{\text{number of gates}} = |\lambda_{\text{InGaAs}} - \lambda_{\text{Silicon}}|$) decreases as the number of gates increases showing that III-V FETs see a larger benefit from multi-gate structures than Si FETs.

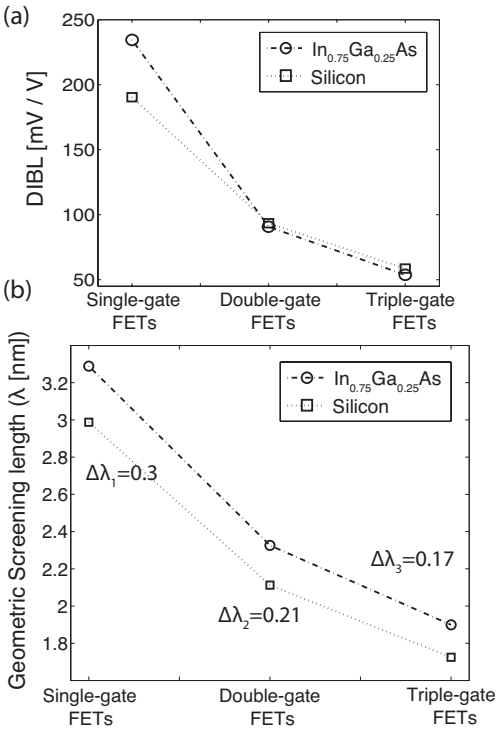

Fig. 6. (a) DIBL (b) Geometric screening length (λ) of the $In_{0.75}Ga_{0.25}As$ and strained-Si planar and non-planar FETs.

Beside the electrostatic control, the properties of the channel materials strongly influence the performance of different FETs. The injection velocity at the top-of-the-barrier (ToB), V_{INJ}, provides a remarkable insight into the transport properties of a given transistor design [40]. Fig. 7 summarizes the method to extract this metric from quantum transport simulations. The $In_{0.75}Ga_{0.25}As$ transistors benefit from a significantly smaller transport effective mass compared to strained-Si, as summarized in Table 1, resulting in a ballistic injection velocity at the top-of-the-potential barrier 3 to 4.7 times higher than strained-Si, depending on the device architecture.

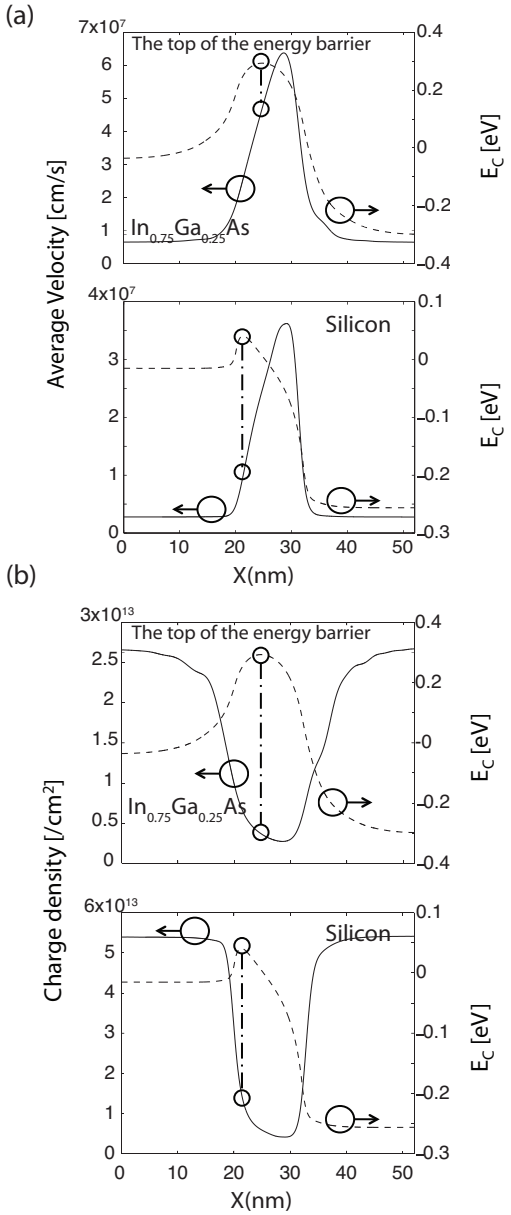

Fig. 7. (a) Ballistic injection velocity in the $In_{0.75}Ga_{0.25}As$ and strained-Si double-/triple-gate FinFETs extracted at the top of the energy barrier (b) ON-state carrier density in the $In_{0.75}Ga_{0.25}As$ and Si double-/triple-gate FinFETs extracted at the top of the energy barrier.

However, due to the low effective mass, III-V FETs suffer from a lower density-of-states (*DOS*), which generally reduces the effective gate capacitance and the maximum achievable inversion charge density (N_{INV}). Under the same bias condition, the strained-Si transistors exhibit a 3.8 to 5.2 times higher inversion charge density at the ToB compared to the $In_{0.75}Ga_{0.25}As$ transistors. The increase of the inversion charge at the ToB overwhelm the benefit of a high injection velocity since the drain current can be expressed as $I_D = q\, V_{INJ}\, N_{INV}$, where q is the elementary charge. Therefore, the strained-Si FETs have slightly higher ballistic ON-currents than the $In_{0.75}Ga_{0.25}As$ FETs, as shown in Table 2.

The inversion charge and injection velocity are not only affected by material properties, but also by the device architecture. In Table 2, an increase of the injection velocity and inversion charge density can be observed in multi-gate architectures which deliver higher current drives than single-gate devices. Hence, the ON-current of the double-gate structures is improved by about 1.7 times in both the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs as compared to the single-gate structures. The ON-current of the triple-gate FinFET increases about 2.4 times in the $In_{0.75}Ga_{0.25}As$ FET and 2.2 times in the strained-Si FET again compared to the single-gate architectures.

The $In_{0.75}Ga_{0.25}As$ FETs see a higher performance improvement than the strained-Si in devices as the number of gates increases, because the III-V materials are more sensitive to SCE and take advantage of the better electrostatic control provided by the multi-gate architecture. As a consequence, this is a key finding of our paper, Table 2 demonstrates that the $In_{0.75}Ga_{0.25}As$ and strained-Si triple-gate FinFETs exhibit almost identical performance metrics: a low *SS* and *DIBL* as well as a large ballistic ON-current.

However, it should be emphasized that the ballisticity of ultra-short III-V and strained-Si nano-transistors is currently unknown and difficult to estimate. So far, Si-based FETs have always operated at about 50% of their ballistic limit, mainly due to surface roughness scattering at the $Si\text{-}SiO_X$ interface [41]. This number has not changed much for many successive technology generations. In addition, recent results of Si and III-V transistor simulation prove that electron-phonon scattering plays a more important role in Si than in III-V [42], because many more subbands are available in Si than in III-V for electrons to scatter out of the original state.

In contrary, specific III-V FETs seem to operate very close to their ballistic limit [16, 18, 39] since surface roughness scattering is extremely small in these devices. Especially, growing a high-κ layer directly on the top of a III-V channel might significantly increase surface roughness and remote Coulomb impurity scattering in these transistors and deteriorate their ballisticity. There are number of proposed processing techniques such as interfacial passivation layer (IPL) and atomic layer deposition (ALD) to address the interfacial chemistry on III-V compound semiconductors [2, 10, 43]. In effect, their insulator layer is often made of another III-V material with a larger band gap or a wide band gap III-V material / high-κ gate stack so that the channel-insulator interface is very smooth. Such

insulator layers work well for relatively large EOT, but it is not clear yet what will happen when the EOT must be reduced below 1nm.

It should also be noted that simulation results are based on the same low series resistance assumed in the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs simulation. The contacts of FETs based on III-V semiconductors are often characterized by higher series resistance compared to Si [8, 16, 18, 39, 46]. However, some studies indicate that the contact resistance of n-type InGaAs can be significantly reduced by using innovative processing techniques [44, 45]. Experimentally, the contacts of III-V semiconductors have always been characterized by much larger series resistances than those of Si due to structural reasons [8-9, 16, 18, 39, 46]. The analysis presented here emphasizes the need to optimize the extrinsic part of the device by incorporating such novel processing techniques in order to reduce the contact resistance and improve the performance of III-V FETs. [8, 44, 45, 46].

Since the exact ballisticity of the $In_{0.75}Ga_{0.25}As$ and strained-Si FETs as well as the achievable contact series resistances are uncertain yet, it is difficult to determine what will be the best material for nano-scale transistors. However, numerical device simulations are required to provide performance projections according to the ITRS specifications without complicated fabrication processes of multiple device prototypes. The simulation results indicate that at 12nm gate length, $In_{0.75}Ga_{0.25}As$ FETs deliver very similar performance as strained-Si FETs. The contact resistances dominate the behavior of both device types. Triple-gate FinFETs surely represent the best architecture for sub-15nm gate contacts, independently from the choice of the channel material.

IV. Conclusion and Outlook

This paper assesses the performance of the $In_{0.75}Ga_{0.25}As$ and strained-Si channel nano-scale transistors in single-/double-gate planar FETs and non-planar triple-gate FinFETs configurations in preparation for the 12nm technology node. The device structure, doping concentration, OFF-current, and normalization conditions are defined according to the ITRS specifications and with the help of Intel Corporation. The impact of the channel material property and device architecture on the ultimate performance of ballistic transistors is theoretically analyzed.

The simulation results indicate that III-V FETs do not outperform Si FETs in the ballistic regime, but deliver very similar performance. However, III-V is still one of the most promising candidates, because they could operate closer to their ballistic limit than Si FETs under certain circumstances and therefore provide higher ON-current due to less performance degradation from electron-phonon and surface scatterings. Ultra-short III-V FETs need multi-gate structures to overcome the weakness of SCE caused by their narrow band gap, small electron effective mass, and high relative dielectric constant. Multi-gate architectures represent a very consistent way to reduce *SS* and *DIBL* while increasing the ON-current. Also, to keep improving the performance of both III-V and Si FETs in the future technology nodes, their source and drain regions should be optimized to minimize their contact series resistance, since the overall device performance will be dominated by the contact resistance.

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