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Effects of (NH₄)₂S passivation on the off-state performance of 3-dimensional InGaAs metal-oxide-semiconductor field-effect transistors

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Planar and 3-dimensional (3D) buried-channel InGaAs metal-oxide-semiconductor field-effect transistors (MOSFETs) have been experimentally demonstrated at deep-submicron gate lengths. The effect of (NH₄)₂S passivation with different concentrations (20%, 10%, or 5%) on the off-state performance of these devices has been systematically studied. 10% (NH₄)₂S treatment is found to yield the optimized high-k/InP barrier layer interface property, resulting in a minimum subthreshold swing (SS) lower than 100 mV/dec. Moreover, the 3D device structure greatly improves the off-state performance and facilitates enhancement-mode operation. A scaling metrics study has been carried out for 10% (NH₄)₂S treated 3D devices with gate lengths down to 100 nm. With the optimized interface passivation, 3D III-V MOSFETs are very promising for future high-speed low-power logic applications.

Recently, surface-channel and buried-channel III-V metal-oxide-semiconductor field-effect transistors (MOSFETs) have been extensively studied for beyond 14 nm logic applications. Thanks to the continuous progress on improving high-k/III-V interfaces, inversion-mode InGaAs MOSFETs with high drive current have been realized with various gate stacks.1–5 On the other hand, buried-channel InGaAs MOSFETs with GaAs/AlGaAs, InAlAs, or InP barrier6–9 and quantum-well FETs (QWFETs) with thin InP barrier10 have been shown to offer higher transconductance (g_m), higher effective mobility, and lower subthreshold swing (SS) compared to surface-channel III-V MOSFETs. Furthermore, non-planar structure has recently been introduced to III-V device fabrication to suppress short channel effects (SCEs) at deep-submicron gate lengths. Much better off-state performance has been obtained on InGaAs FinFETs (Refs. 11 and 12) and multi-gate QWFETs (Ref. 13). Therefore, a 3-dimensional (3D) buried-channel InGaAs MOSFET is promising candidate for ultimately scaled III-V device technology. (NH₄)₂S passivation is a common pre-gate treatment to improve the interface quality of III-V MOSFETs. O’Connor et al. recently reported a systematic Al₂O₃/InGaAs interface study with different (NH₄)₂S passivation conditions.14 Superior capacitance-voltage (CV) characteristics have been achieved on 10% (NH₄)₂S treated samples. However, the impact of different sulfur passivation conditions on the interface property of InGaAs MOSFETs at the device level is lacking. In a buried-channel InGaAs MOSFET, although the oxide/semiconductor interface is not directly located at the high mobility channel, the high-k/barrier layer interface is of great importance to achieve good off-state performance of the device and, therefore, it can also be a good test vehicle for optimization of the sulfur passivation.

In this letter, we fabricated planar and 3D buried-channel InGaAs MOSFETs and systematically study the effect of (NH₄)₂S passivation with different concentrations (20%, 10%, or 5%) on the off-state performance of the devices. It is found that 10% (NH₄)₂S passivated devices show the best interface property, yielding a lower SS and drain-induced barrier lowering (DIBL). The positive threshold voltage (V_T) shift of the 20% and 5% (NH₄)₂S treated devices confirms that more acceptor traps remain unpassivated in these devices. Moreover, a detailed scaling metrics study of 3D buried-channel InGaAs MOSFETs treated with 10% (NH₄)₂S is also carried out for gate length (L_G) down to 100 nm. By implementing 3D structure, a SS lower than 100 mV/dec has been obtained and enhancement-mode operation is achieved.

MOSFET fabrication started with a 2 in. semi-insulating InP substrate. A 300 nm undoped In₀.₅₂Al₀.₄₈As buffer layer, 10 nm undoped In₀.₇Ga₀.₃As channel layer, 2 nm undoped InP barrier layer, and 20 nm N⁺ doped InGaAs layer were sequentially grown by molecular beam epitaxy. Device

![FIG. 1. (Color online) (a) Schematic diagram of planar and 3D buried-channel InGaAs MOSFETs in x-z plane, (b) Cross sectional view of 3D buried-channel InGaAs MOSFETs in y-z plane, and (c) Top-view SEM image of a finished 3D buried-channel InGaAs MOSFET with W_fin = 30 nm and L_G = 350 nm.](https://example.com/fig1.png)
isolation and gate recess etching were then performed using citric acid based solution. The gate lengths of the devices were varied from 0.5 μm down to 100 nm. For non-planar devices, a fin etching process was done using BCl3/Ar based reactive ion etching. The smallest fin width (WFin) defined was 30 nm and the fin height (HFin) was around 50 nm. After short buffered oxide etch (BOE) dip, the samples were soaked in (NH4)2 S (20%, 10%, or 5% diluted in H2O). The passivation time was fixed at 10 min for all three (NH4)2 S concentrations in this experiment. The passivation time of 10 min is optimized by the detailed Al2O3/InP capacitance-voltage interface studies. The air exposure after sulfur treatment was minimized. The samples were then loaded into an ASM F-120 atomic-layer deposition (ALD) reactor for 5 nm Al2O3 deposition at 300°C. Source/drain contacts were then formed by Au/Ge/Ni deposition and 350°C rapid thermal annealing process (RTA). Finally, Ni/Au was electron beam evaporated as gate metal. Since sulfur passivation was found to be unstable after thermal treatment higher than 400°C, no post deposition annealing (PDA) was performed after ALD gate dielectric deposition, and the thermal budget of the entire fabrication process was as low as 350°C. All patterns were defined by a Vistec UHR electron beam lithography system.

Figure 1(a) shows the schematic diagram of the planar and 3D buried-channel InGaAs MOSFETs fabricated in this work. Figure 1(b) shows the schematic cross section in y-z plane for 3D devices. A top view scanning electron microscopy (SEM) image of a finished device with parallel fin structures is shown in Figure 1(c). Figures 2(a) and 2(b) show the well-behaved output and transfer characteristics of a 3D buried-channel InGaAs MOSFET with Lg = 250 nm, WFin = 30 nm and passivated with 10% (NH4)2 S before gate oxide deposition. A saturation drain current of 380 μA/μm and gm of 557 μS/μm is obtained at Vds = 0.5 V. The threshold voltage (Vth) of the device is −0.05 V from linear extrapolation at Vds = 50 mV and −0.18 V using 1 μA/μm metric at Vds = 0.5 V. A SS of 120 mV/dec and DIBL of 99 mV/V are also achieved. Compared to deep-submicron surface-channel InGaAs MOSFETs, a higher gm is obtained at a lower drain voltage with the same gate oxide thickness, indicating the advantage of buried-channel devices for low-voltage operation.

To study the effect of different sulfur passivation conditions, the SS and Vth of planar and 3D devices with (NH4)2 S (20%, 10%, or 5%) passivation are shown in Figures 3(a) and 3(b), respectively. To minimize the influence from the SCE, Lg = 0.5 μm devices are investigated. First, the 10% (NH4)2 S treated devices show the lowest SS of 96 mV/dec, indicating a lower interface trap density (Dit) at the Al2O3/InP barrier layer interface. The upper limit of midgap Dit is estimated to be around 4.6 × 1012/eV·cm² for 10% (NH4)2 S treated surface. The reduction of Dit indicates the effective suppression of native oxides at high-k/InP interface by 10% (NH4)2 S passivation, being evident from the lack of In3⁺ states detected in Al2O3/InP (100) x-ray photoelectron spectroscopy (XPS) characterization. This is in good agreement with the previous XPS study on high-k/InGaAs interface, where lowest amount of surface oxides are present in 10% (NH4)2 S treated samples. However, SS values alone cannot distinguish between acceptor/donor traps. Second, 10% (NH4)2 S treated devices show lower Vth than 20% or 5% (NH4)2 S treated devices. This indicates that 20% and 5% (NH4)2 S treatment is less effective in passivating acceptor traps, resulting in a positive Vth shift. Moreover, the highest drain current is also obtained on 10% (NH4)2 S passivated devices at the same gate voltage overdrive (Vg−Vth). This again suggests that the unpassivated surface traps are mostly acceptor-like. These observations are consistent with the conclusion from previous interface study on surface-channel InGaAs MOSFETs, where simulation results show that acceptor-like traps degrade SS, Vth, and on-current. It is also noted that similar results have been found on Ge surface and interfaces, where unpassivated acceptor defects delays inversion in Ge nMOSFETs. Third, the DIBL of 10% (NH4)2 S passivated devices are also found to be the lowest. This may result from a better gate electrostatic control of the channel.
The benefits of 3D structures are confirmed with lower SS, channel InGaAs MOSFETs is also carried out and the layer interface. A scaling metrics study of the 3D buried-channel InGaAs MOSFETs passivated with 10% (NH₄)₂ S vs. LG of planar and 3D (WFin = 30nm) buried-channel InGaAs MOSFETs passivated with 10% (NH₄)₂ S. VT is determined by 1 μA/μm metric at Vds = 0.5 V.

due to the better gate oxide/barrier layer interface quality. Although not a direct effect of Dth, a lower DIBL is desired when device dimension scales down to deep-submicron regime. Finally, the 3D devices with WFin = 30nm show lower SS and increase in VT, compared to the planar devices. By introducing 3D structure, the devices can be switched off faster and enhancement-mode operation can be more easily achieved. In summary, 10% (NH₄)₂ S passivation is found to yield the best interface quality and optimum off-state performance for planar and 3D buried-channel InGaAs MOSFETs.

Furthermore, we investigate the scaling of the buried-channel InGaAs MOSFETs with 10% (NH₄)₂ S passivation and the gate lengths of the devices varied from 0.5 μm down to 100 nm. Figure 4(a) shows the SS and DIBL versus LG for non-planar devices with WFin = 30 nm, where SS is obtained at a drain voltage of 0.5 V. It is found that SS and DIBL gradually increase with LG shrinking due to the SCE. Further suppression of SCE can be achieved by reducing WFin and decreasing the equivalent oxide thickness, or implementing more advanced 3D structure such as gate-all-around structure.

Figure 4(b) shows the VT versus LG for planar and 3D devices with WFin = 30 nm. A 0.15 V to 0.25 V positive VT shift has been observed for 3D devices, making the device operation more approaching enhancement-mode. Moreover, 3D devices show better threshold roll-off property due to a better electrostatic control of the channel. These results highlight the importance of introducing advanced 3D structure into the fabrication of III-V MOSFETs at deep sub-micron gate lengths.

In conclusion, planar and 3D buried-channel InGaAs MOSFETs have been demonstrated with gate length down to 100 nm. The effects of sulfur passivation with different (NH₄)₂ S concentrations (20%, 10%, or 5%) on the off-state performance of the planar and 3D devices are systematically studied. It is found that 10% (NH₄)₂ S is the optimum sulfur passivation condition, resulting in a better Al₂O₃/InP barrier layer interface. A scaling metrics study of the 3D buried-channel InGaAs MOSFETs is also carried out and the benefits of 3D structures are confirmed with lower SS, DIBL, and higher VT, making 3D III-V MOSFETs very promising for beyond 14 nm logic applications. The optimized sulfur passivation technique is applicable to the fabrication of surface-channel InGaAs MOSFETs as well as bottom-up GaAs, InGaAs, and InAs nanowire FETs providing a simple solution to improve high-k/III-V interface quality.

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