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Performance Prediction of Ultrascaled SiGe/Si Core/Shell Electron and Hole Nanowire MOSFETs

Abhijeet Paul, Saumitra Mehrotra, Mathieu Luisier, and Gerhard Klimeck

***Abstract*—The performances of ultrascaled SiGe nanowire field-effect transistors (NWFETs) are investigated using an atomistic tight-binding model and a virtual crystal approximation to describe the Si and Ge atoms. It is first demonstrated that the band edges and the effective masses of both relaxed and strained SiGe bulk are accurately reproduced by our model. The band structure model is then coupled to a top-of-the-barrier quantum transport approach to simulate the output characteristics of ultrascaled n/p SiGe NWFETs and explore their viability for future high-performance CMOS applications. We predict a considerable improvement of SiGe nFETs and pFETs over their Si counterparts for SiGe/Si core/shell structures.**

***Index Terms*—Ballistic, MOSFETs, nanowire (NW), SiGe, tight binding (TB), top of the barrier (ToB), virtual crystal approximation (VCA).**

I. Introduction

HIGH-PERFORMANCE (HP) CMOS technology improvements are pursued by increasing the hole mobility through the use of SiGe by various experimental groups [1], [2]. Improvements in the process technology enabled the fabrication of high-Ge-concentration ultrascaled SiGe-channel nanowire field-effect transistors (NWFETs). These NWFETs can be divided into two categories: 1) SiGe/Si core/shell channels with SiO_2/high-κ as gate dielectrics [1], [2] (Type A) and 2) SiGe channels with high-κ (HfO_2 or ZrO_2) gate dielectrics (Type B), as shown in Fig. 1.

The performance analysis of SiGe NWFETs with nanoscale dimensions is only possible with a simulator that can simultaneously handle the material, the strain, the quantum confinement properties, and the electron–hole band coupling of the devices. This letter presents a general atomistic tight-binding (TB) electronic structure calculation method to solve such a system (Section II), validates the band structure model against the experimental bulk SiGe data (Section III-A), applies it to Type A and B SiGe n/p NWFETs for HP-CMOS applications (Section III-B), and finally provides the conclusions (Section IV).

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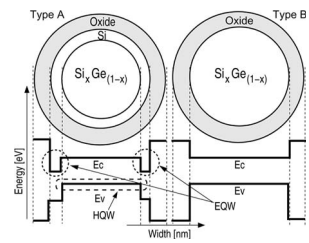

Fig. 1. Schematic of Type A and B SiGe NWFETs. Cross-sectional material variations are shown for the two structures. Shown below is the variation in the CB minimum (E_c) and the VB maximum (E_v) along the cross-section of the NWFETs. EQW (HQW) represent the electron (hole) quantum-well formed due to the bandedge mismatch at SiGe and Si interface.

II. Numerical Model and Approach

A. Band Structure Calculation in SiGe Alloys

The band structure of SiGe is based on a virtual crystal representation of the binary alloy (A_xB_{1-x}). Its TB coefficients are calculated as the weighted mean of the coefficients of the individual materials A and B [TB virtual crystal approximation (TB-VCA)]

$$E_\sigma^{AB} = x \cdot E_\sigma^A + (1-x) \cdot E_\sigma^B \quad (1)$$

$$V_{\sigma_1\sigma_2}^{AB} = x \cdot V_{\sigma_1\sigma_2}^A + (1-x) \cdot V_{\sigma_1\sigma_2}^B \quad (2)$$

where E_σ and $V_{\sigma_1\sigma_2}$ are the on-site energies for an orbital σ and the nearest neighbor coupling elements between two orbitals $\sigma_{1,2}$, respectively. Si and Ge atoms are replaced by fictitious SiGe atoms whose TB parameters are linearly interpolated between those of Si and Ge taken from [3].

Si and Ge have a lattice mismatch of 4.2%, which gives rise to a large strain field in SiGe systems. This effect is taken into account by first adjusting the coupling matrix elements $V_{\sigma_1\sigma_2}^A$ and $V_{\sigma_1\sigma_2}^B$ in (2) according to Harrison's scaling rule [3] and then by linearly interpolating them

$$V_{\sigma_1\sigma_2}^{AB,\text{strain}} = x \cdot V_{\sigma_1\sigma_2}^A \left(\frac{d_A}{d_{AB}}\right)^{\eta_A} + (1-x) \cdot V_{\sigma_1\sigma_2}^B \left(\frac{d_B}{d_{AB}}\right)^{\eta_B}. \quad (3)$$

In (3), the η's are taken from [3], and the average bond length d_{AB} is calculated using Vegard's law [4]

$$d_{AB} = x \cdot d_A + (1-x) \cdot d_B \quad (4)$$

where d_A and d_B are the individual bond lengths for materials A and B, respectively. The internal strain at the SiGe/Si (AB/A) interface is accounted by averaging the bond length at the interface (d_{int}) over two atomic monolayers

$$d_{\text{int}} = (d_{AB} + d_A)/2. \quad (5)$$

The scaling of the nearest neighbor coupling elements $V_{\sigma_1\sigma_2}$ leads to an energy shift (Δ_σ) of the diagonal elements E_σ $(E_\sigma \to E_\sigma + \Delta_\sigma)$ [5]. This is accounted for in (1) as

$$E_\sigma^{AB,\text{strain}} = x \cdot \left(E_\sigma^A + \Delta_\sigma^A\right) + (1-x) \cdot \left(E_\sigma^B + \Delta_\sigma^B\right). \quad (6)$$

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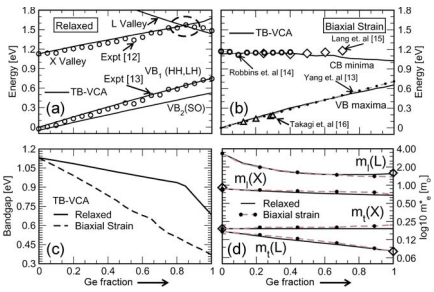

Fig. 2. (a) Comparison of bandedges for relaxed bulk SiGe. Experimental CB data (○) is from [11]. VB values obtained by subtracting the bandgap (Eg) values in [12] from our CB values. (b) Comparison of bandedges for biaxially strained SiGe bulk structure. CB experimental data from [13] (○) and [14] (◊) and VB data from [15] (4) and [12] (dotted line). (c) Bandgap variation in relaxed and biaxially strained SiGe bulk structure calculated using TB-VCA. (d) Electron effective masses in transverse $(m^*_{\rm te})$ and longitudinal $(m^*_{\rm le})$ directions for relaxed and biaxially strained SiGe bulk with varying Ge%. Experimental data (◇) in (d) are from [16].

A previous study [6] derived an approximate, atomic disorder dominated band structure of SiGe nanowires and showed that the standard VCA cannot reproduce the bandgaps of such systems. The improved VCA model presented here includes the nonlinear effects of bond deformation in Si and Ge as a function of bond length separately before the material is homogenized. The new TB-VCA model can reproduce critical design elements such as bandgaps and effective masses in close agreement with experimental data. It does, however, not include the atomistic disorder that could be captured with a full 3-D representation.

B. Self-Consistent Charge and Potential Calculation

The gating and the applied source-to-drain bias are included by self-consistently coupling the calculation of the charge and of the electrostatic potential of the NWFETs at one single location along the transport direction, the top of the barrier (ToB), also known as the "virtual source" [7]. The band structure of the SiGe NW is calculated at the ToB using the TB model. Forward and backward propagating states are populated according to the S and D Fermi levels as well as the gate potential $(V_{\rm GS})$. The resulting charge is self-consistently calculated with the electrostatic potential at the ToB on a 2-D finite element grid [8]. Any gate configuration is possible, from a single gate to a gate all around. It has been shown that the ToB approach is as accurate as computationally more intensive 3-D approaches [9] as long as the gate length (L_g) is longer than ∼5× the NW cross section width (W) and DIBL is not relevant [10].

III. Results and Discussion

A. Benchmarking Against Bulk Band Structure

The $E(k)$ dispersion along the principle Brillouin zone axes $(L \rightarrow \Gamma \rightarrow X \rightarrow U/K \rightarrow \Gamma)$ is calculated for relaxed and biaxially strained bulk SiGe structures with different Ge concentrations. Fig. 2(a) shows the relaxed CB and VB edges. The TB-VCA model agrees well with the available experimental data [11], [12] for all the Ge compositions. The crossover of the conduction band (CB) edge from the X valley to the L valley at around 85% Ge is correctly captured in the relaxed system [Fig. 2(a)].

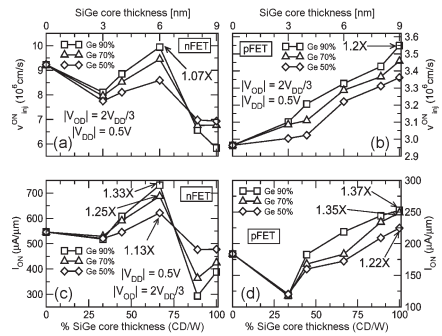

Fig. 3. $v^{\rm ON}_{\rm inj}$ for the (a) nFETs and (b) pFETs. $I_{\rm ON}$ is shown for the (c) nFETs and (d) pFETs. The device metrics, calculated at $V_{\rm OD} = 2V_{\rm DD}/3$ and $|V_{\rm DD}| = 0.5$ V, are plotted for ⟨100⟩ SiGe channel with 90%, 70%, and 50% Ge content and core thickness of 0, 3, 4, 6, 8, 9 nm (Type B).

Biaxially strained SiGe structures are obtained by growing SiGe on a thick silicon layer [2]. Pure Ge grown pseudomorphically on a (100) Si substrate produces a compressive strain of 4.2% due to lattice mismatch. Fig. 2(b) shows the band edge variation as a function of Ge% for compressively strained SiGe on (100) Si. The bandgap variation for relaxed and biaxially strained bulk SiGe is shown in Fig. 2(c). The strained CB varies only weakly with varying Ge%, resulting in a larger bandgap reduction compared to the relaxed system. The VB shift is similar in both systems. Biaxial compressive stress only weakly affects the electron transverse and longitudinal masses at the X and the L valley compared to the relaxed case [Fig. 2(d)].

B. Performance Analysis of SiGe NWFETs

SiGe/Si core/shell structures represent an attractive FET design due to their low-defect channel/gate-dielectric interface and improved performances for both n- and pFETs [1], [2] over their Si counterparts. Here, Type A and B NWFETs with n- and p-doped contacts and ⟨100⟩ oriented channels are considered. The total wire diameter (W) is set to 9 nm with a 1.5-nm gate oxide $(\mathrm{SiO_2}, \epsilon_r = 3.9)$. The core diameter (CD) is varied from 0 (pure Si), 3, 4, 6, 8 to 9 nm (no Si shell, Type B).

The performance comparison is done using a constant-overdrive-voltage $(V_{\rm OD} = 2V_{\rm DD}/3)$ method, as proposed in [17]. The ON-state gate bias $(V^{\rm ON}_{\rm GS})$ is defined as $V^{\rm ON}_{\rm GS} = V_{\rm Tlin} + V_{\rm OD}$, where $V_{\rm Tlin}$ is the linear threshold voltage of the FET. A $V_{\rm DD}$ of 0.5 V has been used in this work.

The ON-state drain current $I_{\rm ON}$ and the intrinsic device delay $\tau_D = C_g V^{\rm ON}_{\rm GS}/I_{\rm ON}$, where C_g is the gate capacitance, are two important metrics for performance comparison [17]. In 1-D ballistic FETs, $I_{\rm ON}$ and τ_D are a direct function of the virtual source carrier velocity $(v^{\rm ON}_{\rm inj})$

$$I_{\rm ON} = C_g \cdot V_{\rm OD} \cdot v^{\rm ON}_{\rm inj} \tag{7}$$

$$\tau_D = (C_g \cdot V_{\rm OD}) / \left(C_g \cdot V_{\rm OD} \cdot v^{\rm ON}_{\rm inj}\right). \tag{8}$$

SiGe Versus Si, $v^{\rm ON}_{\rm inj}$ Comparison: In nFETs $v^{\rm ON}_{\rm inj}$ improves by ∼1.07 × for 90% Ge and $CD/W = 2/3$ [Fig. 3(a)]. For a given CD, the CB edge mismatch increases with increasing Ge% in the core, hence forming a deeper electron quantum well (EQW) in the Si shell (Fig. 1). The inversion charge preferably stays in this Si EQW, where electron velocity $(v_{\rm inj})$ is higher than Ge [18]. As the CD increases, the EQW becomes thinner, and the inversion charge moves back to the slower SiGe core. This explains the oscillation in $v^{\rm ON}_{\rm inj}$ with shell thickness

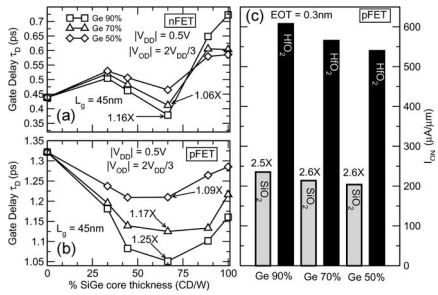

Fig. 4. Gate delay (τ_D) for different SiGe (a) nFETs and (b) pFETs. The fastest n-FET (90% Ge channel, $CD = 6$ nm) is $\sim$2$\times$ faster than the fastest pFET (90% Ge channel, $CD = 6$ nm). (c) $I_{\rm ON}$ in the 9 nm diameter SiGe channel pFETs improve by $\sim$2.5$\times$ after replacing SiO_2 by HfO_2.

reduction. Type B NWFETs show decreasing $v_{\rm inj}^{\rm ON}$ with increasing Ge%. In pFETs a higher Ge% and reduction in Si-shell thickness improve $v_{\rm inj}^{\rm ON} \sim 1.2\times$ compared to Si [Fig. 3(b)].

SiGe Versus Si, $I_{\rm ON}$ Comparison: In nFETs for 90% Ge with $CD/W \sim 2/3$, the $I_{\rm ON}$ improves by $\sim$1.33$\times$ [Fig. 3(c)] since the inversion charge is pushed inside the high velocity Si shell [18]. In nFETs, $I_{\rm ON}$ also shows an oscillatory nature for the same reason as $v_{\rm inj}^{\rm ON}$. The pFETs show improvement in $I_{\rm ON}$ with an increasing Ge% and CD [Fig. 3(d)]. This benefit can be attributed to the higher Ge% in the core (higher $v_{\rm inj}^{\rm ON}$) and very thin shell thickness (larger C_g). In pFETs, $I_{\rm ON}$ shows a dip when going from a pure Si channel to a SiGe channel [Fig. 3(d)], since the charge buildup is mostly inside the SiGe core (HQW, Fig. 1) which is buried under a thick Si shell, resulting in smaller C_g and hence smaller $I_{\rm ON}$ according to (7).

SiGe Versus Si, τ_D Comparison: The gate delay (τ_D) is determined by the interplay of the inversion charge buildup and its velocity in the channel. For nFETs, an improvement of $\sim$1.1$\times$ is observed for the 90% Ge core with $CD/W \sim 70\%$ [Fig. 4(a)]. In pFETs, the minimum τ_D is obtained for the devices with $CD/W \sim 66\%$ [Fig. 4(b)]. For pFETs, the maximum improvement is obtained for the 90% Ge core which has higher $v_{\rm inj}^{\rm ON}$. Thus, the core/shell structures can be designed to speed up both the n- and pFETs compared to their Si counterparts.

Comparison of SiGe n- and pFETs: The pFETs are $\sim$2$\times$ slower as compared to the nFETs ($\tau_n/\tau_p \sim 0.4/1.05$) [Fig. 4(a) and (b)]. The pFETs can be enhanced by improving the gate control on the channel. This can be achieved in two ways: 1) by reducing the Si-shell thickness and 2) by using a high-κ gate dielectric material. I_D–$V_{\rm GS}$ simulation for three Ge% (90, 70, and 50) channels with no Si shell and 1.5-nm-thick HfO_2 as gate dielectric (EOT $\sim$ 0.3 nm, $\epsilon_r \sim 21$) has been performed. $I_{\rm ON}$ improves as much as $\sim$2.5$\times$, bringing the pFET performance closer to the nFET, as shown in Fig. 4(c). However, this increases the fabrication complexity and the need for good NW/oxide interface quality [2].

IV. Conclusion

We have presented an improved experimentally benchmarked band structure model for both relaxed and strained SiGe structures. This model has been incorporated into a ToB transport model, and it has been used to study both n and p SiGe NWFETs. The design for 9-nm SiGe NWFETs is explained. The nFETs can be improved by $\sim$1.3$\times$ in $I_{\rm ON}$ and the pFETs by $\sim$1.37$\times$ compared to the Si FETs. Both n- and p-type SiGe FETs show an improvement of $\sim$1.2$\times$ over their Si counterparts in terms of gate delay for a high Ge% and an optimally thick Si shell. SiGe pFETs will require a thinner Si shell and a high-κ gate dielectric material to make them comparable to SiGe nFETs. Alloy and interface roughness scattering have been neglected in this study which are expected to reduce the channel currents.

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