

6-2010

Leakage-Reduction Design Concepts for Low-Power Vertical Tunneling Field-Effect Transistors

Samarth Agarwal

Purdue University - Main Campus

Gerhard Klimeck

Purdue University - Main Campus, gekco@purdue.edu

Mathieu Luisier

Purdue University - Main Campus

Follow this and additional works at: <http://docs.lib.purdue.edu/nanopub>



Part of the [Nanoscience and Nanotechnology Commons](#)

Agarwal, Samarth; Klimeck, Gerhard; and Luisier, Mathieu, "Leakage-Reduction Design Concepts for Low-Power Vertical Tunneling Field-Effect Transistors" (2010). *Birck and NCN Publications*. Paper 807.

<http://dx.doi.org/10.1109/LED.2010.2046011>

This document has been made available through Purdue e-Pubs, a service of the Purdue University Libraries. Please contact epubs@purdue.edu for additional information.

Leakage-Reduction Design Concepts for Low-Power Vertical Tunneling Field-Effect Transistors

Samarth Agarwal, Gerhard Klimeck, and Mathieu Luisier

Abstract—Using an atomistic full-band quantum transport solver, we investigate the performances of vertical band-to-band tunneling FETs (TFETs) whose operation is based on the enhancement of the gate-induced drain leakage mechanism of MOSFETs, and we compare them to lateral p-i-n devices. Although the vertical TFETs offer larger tunneling areas and therefore larger ON currents than their lateral counterparts, they suffer from lateral source-to-drain tunneling leakage away from the gate contact. We propose a design improvement to reduce the OFF current of the vertical TFETs, maintain large ON currents, and provide steep subthreshold slopes.

Index Terms—Band-to-band tunneling transistors, full-band and atomistic quantum transport, steep subthreshold.

I. INTRODUCTION

BAND-TO-BAND tunneling FETs (TFETs) are emerging as an attractive alternative to MOSFETs in reducing the power consumption of integrated circuits. While the subthreshold slope (SS) of conventional MOSFETs is fundamentally limited to 60 mV/dec at room temperature, in TFETs, the cold injection of valence band (VB) electrons from a source contact into the conduction band (CB) of a drain contact does not impose any lower limit on the SS . Although an SS lower than 60 mV/dec has been demonstrated for lateral TFETs based on carbon nanotube [1], silicon [2], and strained germanium [3] devices, all these approaches suffer from low-ON currents, typically a few microamperes per micrometer, when more than 1,000 $\mu\text{A}/\mu\text{m}$ is required [4].

Atomistic full-band transport simulations indicate that lateral p-i-n TFETs made of a homogeneous material are not capable of providing large enough ON currents, even with a low direct band gap such as InSb and a perfect electrostatic control of the channel as gate-all-around nanowires [5], [6]. The ON-current limitation of lateral TFETs originates from their small tunneling area limited to the device cross section. By switching the tunneling mechanism to a vertical approach characterized by an enhancement of the gate-induced drain

leakage present in MOSFETs, it is possible to increase the tunneling area of TFETs proportionally to their gate length and to obtain large ON currents. Such a vertical TFET design has been recently proposed [7]–[9] and named “green FET” (gFET) for its potential to reduce the supply voltage of transistors.

Using the atomistic simulation approach described in Section II, we show in this letter that the gFETs offer larger ON currents than lateral devices but suffer from lateral source-to-drain tunneling leakage away from the gate contact. This effect has never been analyzed before, although it increases the gFET OFF current by several orders of magnitude and makes any steep SS impossible. We therefore propose a design modification to suppress the source-to-drain tunneling leakage in vertical TFETs without affecting their ON current. We further demonstrate using an InAs device that very good performances can be obtained by optimizing the gFET structure.

II. SIMULATION APPROACH AND RESULTS

The InAs lateral and vertical TFETs considered in this letter are simulated using an atomistic full-band quantum transport solver based on the sp^3s^* nearest-neighbor tight-binding method and a wave function approach [5], [10]. Transport is treated in the ballistic limit, and electron-phonon scattering is not included. The InAs tight-binding parameters are taken from [11]. For computational reasons, spin-orbit coupling is neglected, which does not alter our conclusions [5]. Gate leakage currents are also neglected in this letter.

The tight-binding model accurately and simultaneously describes the CB and VB of most semiconductor materials, as well as the imaginary bands coupling them which is responsible for tunneling. Contrary to standard TFET simulators where tunneling is treated as a perturbation in the WKB approximation [12] and only exists in predefined regions, our approach is characterized by a global tunneling model (tunneling is present everywhere by default). Hence, it is not necessary to specify the regions where tunneling is expected to take place, and no crucial tunneling path is omitted.

TFETs are usually based on lateral band-to-band tunneling of electrons from a p^+ source into a n^+ drain, as shown in Fig. 1(a). An increase of the gate voltage pushes down the CB edge of the device channel below the VB edge of the source and opens a bias-dependent tunneling window at the source/channel interface, as shown in Fig. 1(b). The fact that the electrostatic control of the channel diminishes deep into the device body and does not go beyond a few nanometers puts a restriction on the cross-sectional area available for tunneling and on the highest achievable ON current.

Manuscript received February 10, 2010; revised March 10, 2010. Date of publication April 19, 2010; date of current version May 26, 2010. This work was supported in part by the National Science Foundation (NSF) under Grant EEC-0228390, which funds the Network for Computational Nanotechnology; by the NSF PetaApps Grant 0749140; by the Nanoelectronics Research Initiative through the Midwest Institute for Nanoelectronics Discovery; and by the NSF through the TeraGrid resources provided by the Texas Advanced Computer Center and the National Institute of Computational Sciences. The review of this letter was arranged by Editor J. Cai.

The authors are with the Network for Computational Nanotechnology and the Birck Nanotechnology Center, Purdue University, West Lafayette, IN 47907 USA (e-mail: samarth@purdue.edu; gekco@purdue.edu; mluisier@purdue.edu).

Digital Object Identifier 10.1109/LED.2010.2046011

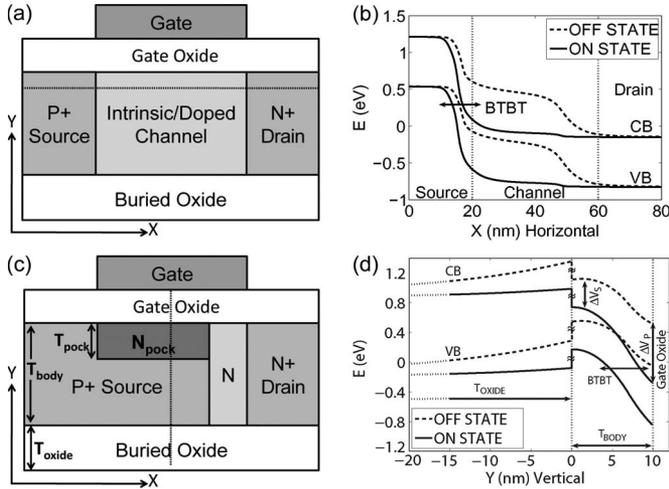


Fig. 1. (a) Lateral p-i-n single-gate TFET. (b) CB and VB edges of the p-i-n device in its (dashed lines) OFF- and (solid lines) ON-states along the horizontal dashed line in (a). (c) Single-gate gFET structure as proposed in [7]. (d) CB and VB edges of the gFET in its OFF- and ON-states along the vertical dashed line in (c). The buried oxide extends from -50 to 0 nm, but only the 20 nm close to the semiconductor channel is shown here.

The vertically tunneling gFET structure, as shown in Fig. 1(c), keeps the p^+ source and n^+ drain of the lateral device, but the source extends close to the drain contact, and both regions are separated only by a lightly n -doped layer. A thin and highly n -doped region called “pocket” is implanted just below the gate contact in the p^+ extended source. Tunneling occurs under the gate region, between the VB electrons of the p^+ extended source and the available confined CB states of the n^+ pocket, as shown in Fig. 1(d). A gate voltage increase moves down the CB edge of the pocket below the VB edge of the extended source and opens a vertical tunneling channel whose area is proportional to the gate length.

Fig. 2(a) compares the transfer characteristics I_d-V_{gs} at $V_{ds} = 0.5$ V of a single-gate InAs lateral p-i-n TFET and a single-gate InAs gFET. Both devices have the same gate length $L_g = 40$ nm, equivalent oxide thickness $EOT = 0.5$ nm, supply voltage $V_{DD} = 0.5$ V, and source and drain doping ($N_A = 2 \times 10^{19}$ cm $^{-3}$, $N_D = 2 \times 10^{19}$ cm $^{-3}$). The lateral device has a body thickness of 5 nm to maintain a good electrostatic control of the channel, while the gFET has $T_{body} = 10$ nm, $T_{pock} = 5$ nm, and $N_{pock} = 2 \times 10^{19}$ cm $^{-3}$, and the n doping of the 5 -nm layer between the source and the drain is 10^{18} cm $^{-3}$.

As expected, the ON current ($I_{ON} = I_d$ at $V_{gs} = V_{ds} = V_{DD}$) is much larger for the gFET ($180 \mu\text{A}/\mu\text{m}$) than for the p-i-n lateral TFET ($14 \mu\text{A}/\mu\text{m}$), but it is still well below the ITRS requirement. The spatial distribution of the gFET ON current is shown in Fig. 2(b). It can be observed that vertical band-to-band tunneling occurs between the extended source and the pocket, but the tunneling current is not homogeneously distributed, and two main channels (arrows) can be distinguished. This is due to the profiles of the CB and VB edges that vary along the x -axis, while they should ideally remain constant.

The detrimental characteristics of the gFET is its very high OFF current ($I_{OFF} = I_d$ at $V_{gs} = 0$ V and $V_{ds} = V_{DD}$) that has never been reported before [7]–[9], and whose spatial distribution is shown in Fig. 2(c). A lateral leakage current

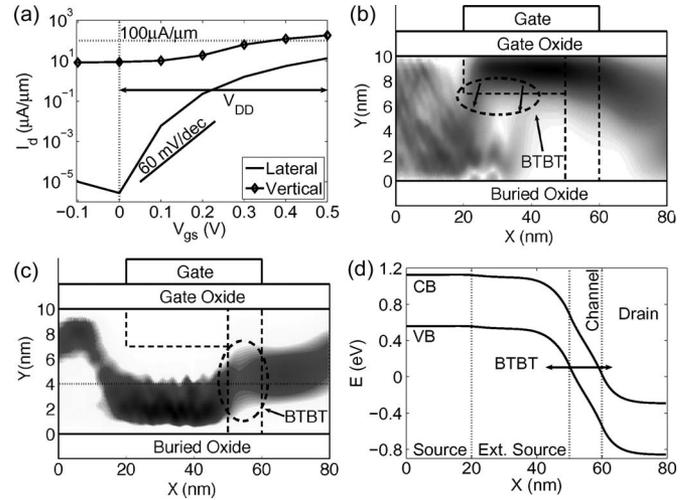


Fig. 2. (a) Transfer characteristics I_d-V_{gs} at $V_{ds} = 0.5$ V of (solid line) a lateral p-i-n TFET and (line with symbols) a vertical gFET, with $L_g = 40$ nm and $EOT = 0.5$ nm. (b) Spatial distribution of the gFET ON current. High-current-density regions appear darker. (c) Same with (b) but for the OFF current. For clarity, a different color scale is used. (d) CB and VB edges of the gFET OFF-state on the horizontal line below the n^+ pocket at $y = 4$ nm in (c).

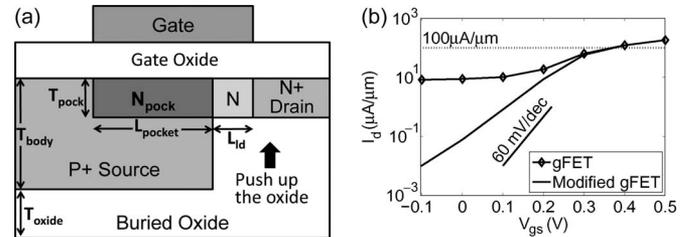


Fig. 3. (a) Modified gFET design. The buried oxide is raised to the height of the pocket in the drain and in the lightly doped channel region. (b) Comparison of the transfer characteristics I_d-V_{gs} at $V_{ds} = 0.5$ V for (line with symbols) the “conventional” and (solid line) the modified gFET design.

flowing between the n^+ pocket and the buried oxide can be identified. Fig. 2(d) describes the band diagram of the region where the OFF current flows. It looks like a lateral p-i-n structure that the gate cannot control due to its distance. VB electrons laterally tunnel from the extended source into the drain contact and increase I_{OFF} . The gFET, as shown in Fig. 1(c), is therefore unsuitable for low-power logic applications.

To address the large OFF-current issue, we propose a modification of the gFET design in Fig. 3(a). The spatial distribution of the OFF current in Fig. 2(c) shows that the VB electrons originating from the extended source are collected in a portion of the drain contact that is not active in the ON-state shown in Fig. 2(b). The buried oxide below the drain and the lightly n -doped channel are therefore pushed up to the height of the pocket in the drain and lightly n -doped channel such that it blocks any lateral tunneling current pathway. The transfer characteristics of the “original” and modified gFETs are compared in Fig. 3(b), demonstrating that I_{OFF} is reduced by several orders of magnitude without affecting I_{ON} .

The gFET ON current and SS must also be improved by optimizing the body thickness T_{body} , pocket length L_{pocket} , width T_{pock} , and doping N_{pock} in Fig. 3(a). Fig. 4(a) shows the effect of the pocket length L_{pocket} on the gFET I_d-V_{gs} .

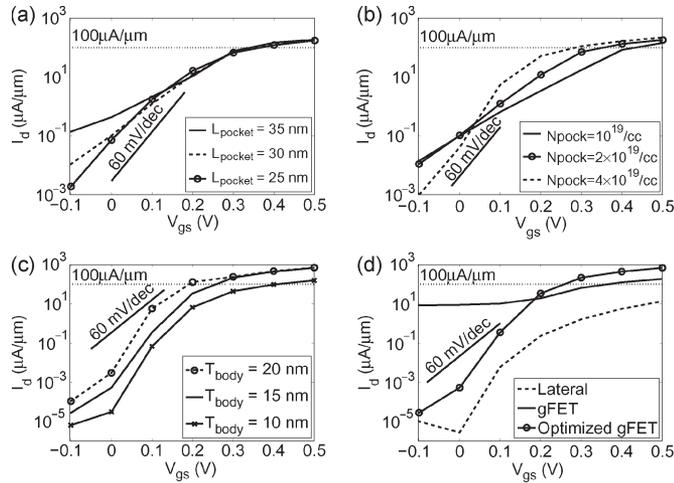


Fig. 4. Transfer characteristics I_d - V_{gs} of different gFET designs. (a) Variation of the pocket length L_{pocket} at a constant gate length $L_g = 40 \text{ nm}$. (b) Variation of the pocket doping N_{pock} . (c) Variation of the body thickness T_{body} . (d) Comparison of (line with circles) the optimized InAs gFET with (solid line) the original gFET design and (dashed line) the lateral p-i-n TFET.

A decrease in L_{pocket} and an increase in L_{ld} ($L_g = L_{\text{pocket}} + L_{\text{ld}}$ remains constant) lead to a further reduction of the gFET OFF current and of the SS . Although the raising of the buried oxide below the drain contact suppressed most of the source-to-drain leakage currents, some diagonal paths joining the extended source and the drain contact persisted. Increasing L_{ld} makes these tunneling paths longer and reduces I_{OFF} and SS . However, the tunneling ON current, which is roughly proportional to L_{pocket} , slightly decreases (about 10% reduction for L_{pocket} going from 35 to 25 nm).

Increasing the pocket doping N_{pock} , as described in Fig. 4(b), induces larger vertical electric fields so that the tunneling length between the p^+ extended source and the n^+ pocket becomes smaller, the current magnitude becomes larger, and the SS becomes steeper. Hence, SS reduces here from 118 mV/dec for $N_{\text{pock}} = 10^{19} \text{ cm}^{-3}$ to 47 mV/dec for $N_{\text{pock}} = 4 \times 10^{19} \text{ cm}^{-3}$, while I_{ON} increases from 143 to 220 $\mu\text{A}/\mu\text{m}$. Similarly, a reduction on T_{pock} improves I_{ON} and SS .

The influence of the body thickness is investigated in Fig. 4(c). As shown in Fig. 1(d), an increase of the gate voltage pushes down the bands not only close to the gate contact in the pocket region, as desired (energy shift labeled ΔV_p), but also deeper in the p^+ extended source (ΔV_s). Of course, $\Delta V_s < \Delta V_p$ since the gate control decreases as a function of the distance, but ideally, ΔV_s should be as small as possible to maximize the electric field between the pocket and the extended source and the tunneling current. Increasing T_{body} from 10 to 15 nm helps reduce ΔV_s and increase I_{ON} . A further increase to 20 nm does not improve I_{ON} .

Finally, Fig. 4(d) shows the best transfer characteristics I_d - V_{gs} at $V_{ds} = 0.5 \text{ V}$, which could be obtained by optimizing the InAs gFET structure ($T_{\text{body}} = 15 \text{ nm}$, $L_{\text{pocket}} = 25 \text{ nm}$, $T_{\text{pock}} = 3 \text{ nm}$, $N_{\text{pock}} = 4 \times 10^{19} \text{ cm}^{-3}$, and $L_g = 40 \text{ nm}$; all the other parameters remain the same). An intrinsic $I_{\text{ON}} = 667 \mu\text{A}/\mu\text{m}$ (no contact series resistance), $I_{\text{OFF}} = 1e-3 \mu\text{A}/\mu\text{m}$, and $SS = 36 \text{ mV/dec}$ are reported for the optimized gFET, which is much better than the original gFET design, and the lateral p-i-n TFET.

III. CONCLUSION

We have investigated InAs vertical TFETs known as gFETs and compared them to lateral p-i-n devices. Simulation results suggest that the gFET gives a significant gain in the ON current over the lateral tunneling geometries due to an increase of the tunneling area. The original gFET design is still unsuitable for low-power logic applications because of very high OFF currents caused by lateral source-to-drain tunneling. A structure modification and an optimization of the device parameters allow for a reduction of I_{OFF} by several orders of magnitudes, an increase of I_{ON} close to the ITRS requirement, and an SS below the 60-mV/dec limit of MOSFETs.

REFERENCES

- [1] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, p. 196 805, Nov. 2004.
- [2] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," *IEEE Electron Device Lett.*, vol. 28, no. 8, pp. 743–745, Aug. 2007.
- [3] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, "Double-gate strained-Ge heterostructure tunneling FET (TFET) with record high drive currents and $<60 \text{ mV/dec}$ subthreshold slope," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–3.
- [4] ITRS 2009. [Online]. Available: <http://www.itrs.net>
- [5] M. Luisier and G. Klimeck, "Atomistic full-band design study of InAs band-to-band tunneling field-effect transistors," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 602–604, Jun. 2009.
- [6] M. Luisier and G. Klimeck, "Performance comparisons of tunneling field-effect transistors made of InSb, Carbon, and GaSb-InAs broken gap heterostructures," in *IEDM Tech. Dig.*, Dec. 2009, Paper 37.6.
- [7] C. Hu, D. Chou, P. Patel, and A. Bowonder, "Green transistor—A VDD scaling path for future low power ICs," in *Proc. Int. Symp. VLSI-TSA*, Apr. 2008, pp. 14–15.
- [8] C. Hu, "Green transistor as a solution to the IC power crisis," in *Proc. 9th ICSICT*, Oct. 2008, pp. 16–20.
- [9] A. Bowonder, P. Patel, K. Jeon, J. Oh, P. Majhi, H.-H. Tseng, and C. Hu, "Low-voltage green transistor using ultra shallow junction and hetero-tunneling," in *Proc. Ext. Abstr. 8th IWJT*, 2008, pp. 93–96.
- [10] M. Luisier, A. Schenk, W. Fichtner, and G. Klimeck, "Atomistic simulation of nanowires in the $sp^3d^5s^*$ tight-binding formalism: From boundary conditions to strain calculations," *Phys. Rev. B, Condens. Matter*, vol. 74, no. 20, p. 205 323, Nov. 2006.
- [11] G. Klimeck, R. C. Bowen, T. B. Boykin, and T. A. Cwik, " sp^3s^* tight-binding parameters for transport simulations in compound semiconductors," *Superlattices Microstruct.*, vol. 27, no. 5/6, pp. 519–524, 2000.
- [12] G. D. Mahan, *Many Particle Physics*. New York: Plenum, 2000.